PIEZOELECTRIC MICRORESONATORS ON SI FOR INDUCTOR FREE EMBEDDED (ON-CHIP) POWER CONVERTERS IN PV POWERED AUTONOMOUS MICROSYSTEMS

by

Abu Saleh Mohammad Imtiaz

A dissertation submitted to the faculty of
The University of Utah
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

The University of Utah

December 2014

Copyright © Abu Saleh Mohammad Imtiaz 2014

All Rights Reserved

The University of Utah Graduate School

STATEMENT OF DISSERTATION APPROVAL

The dissertation of **Abu Saleh Mohammad Imtiaz**

has been approved by the following supervisory committee members:

Name	Role	Date Approved
Faisal Khan	, Chair	**8/13/2014**
Marc Bodson	, Member	**8/13/2014**
Hanseup Kim	, Member	**8/13/2014**
Michael Scarpulla	, Member	**8/13/2014**
Jeffrey Walling	, Member	**8/13/2014**
Shad Roundy	, Member	**8/13/2014**

and by **Gianluca Lazzi** , Chair/Dean of

the Department/College/School of **Electrical and Computer Engineering**

and by David B. Kieda, Dean of The Graduate School.

ABSTRACT

Microelectromechanical systems (MEMS) resonators on Si have the potential to replace the discrete passive components in a power converter. The main intention of this dissertation is to present a ring-shaped aluminum nitride (AlN) piezoelectric microresonator that can be used as an energy-transferring device to replace inductors/capacitors in low power resonant converters for biomedical applications in Autonomous Microsystems. The zero voltage switching (ZVS) condition for a series resonant converter incorporating the proposed MEMS resonator has been presented analytically and verified through experiment. This ZVS condition can be found in terms of the equivalent circuit parameters of the resonator. To the best of my knowledge, a ZVS model for thin film devices has not yet been reported in the literature. A CMOS-compatible fabrication process has been proposed and implemented. In addition, the fabricated devices have been characterized, and experimental results are included. The first contour mode AlN MEMS resonator with moderately low resonant frequency and motional resistance is reported in this dissertation with measured resonant frequency and motional resistance of 87.28 MHz and 36.728 Ω, respectively. The first part of this dissertation discusses the feasibility of a PV powered autonomous microsystem. The reliability, efficiency, and controllability of PV power systems can be increased by embedding the components of a typical power converter on the same Si substrate of a PV cell.

In order to achieve more insight of the macro or surface electronics, a novel fabrication process along with experimental results has been presented in this dissertation demonstrating the integration of PV cells and major components needed to build a power converter on the same substrate/wafer. Because of the cell level power conversion, PV panels constructed from these cells are likely to be immune to partial shading and hot-spot effects. The effect of light exposure on converter switches has been analyzed to understand the converter behavior at various illumination levels. Simulation and experimental results have been provided to support this analysis. In addition to the process-related challenges and issues, this work explains the justification of this integration by achieving higher reliability, portability, and complete modular construction for PV based energy harvesting units for autonomous microsystems.

To my parents; without them I would have been nothing.

TABLE OF CONTENTS

ABSTRACT………………………………………………………………………. iii

LIST OF TABLES ……………………………………………………………… viii

ACKNOWLEDGEMENTS………………………………………………………. ix

Chapters

1. INTRODUCTION…………………………………………………………….. 1

    1.1 Recent Trend in Power Supply Design……………………………….... 3
    1.2 Piezoelectric MEMS Resonator……………………………………….. 5
    1.3 Outline of Thesis…………………………………………………….. 6
    1.4 References………………………………………………….............. 8

2. MONOLITHICALLY EMBEDDED POWER CONVERTERS FOR PV POWER GENERATION……………………………………………………… 12

    2.1 Existing Microfabrication Processing for On-Chip Components: A Literature Review 14
        2.1.1 Silicon Processing for PV Fabrication…………………………. 14
        2.1.2 Silicon Processing for Circuit Components Fabrication……….. 15
        2.1.3 Si or SiC/GaN: Choice of Materials……………………………. 17
        2.1.4 Existing Monolithic Power Converter Solutions……………….. 19
    2.2 Fabrication………………………………………………………............. 19
    2.3 Justification of the Proposed Device Architecture…………………….. 20
    2.4 Simulation Results…………………………………………………….. 22
    2.5 References……………………………………………………………... 22

3. FEATURES AND CHALLENGES IN MONOLITHICALLY EMBEDDED POWER CONVERTERS FOR PV POWER GENERATION……………….. 31

    3.1 Recent High Reliable, High Efficiency Designs for PV Power Generation……………………………………………………………. 32
    3.2 Features of the Proposed Integration………………………………….. 35
        3.2.1 Cost Reduction………………………………………………. 35
        3.2.2 Partial Shedding……………………………………………... 37

3.2.3 Enhanced Reliability………………………………………… 38
3.3 Challenges of the Proposed Integration……………………………. 41
3.4 References……………………………………………………….. 43

4. CHARACTERIZATION OF MONOLITHICALLY EMBEDDED POWER CONVERTERS FOR PV POWER GENERATION…………………………… 49

4.1 Device Fabrication and Characterization……………………………… 50
4.2 Embedded Power Converter………………………………………... 52
4.3 Analysis of Light Generated Effects on the Power Switches (Simulation Results)…………………………………………………. 53
4.4 Analysis of Light Generated Effects on the Power Switches (Experimental Results) 56
4.5 References………………………………………………………... 56

5. PIEZOELECTRIC MEMS RESONATOR IN POWER CONVERSION……. 69

5.1 Characteristics of MEMS Resonator……………………………….. 71
5.2 Basic Principles of Contour Mode Piezoelectric Resonator…………... 73
5.3 Piezoelectric Devices in Power Conversion…………………………. 76
5.4 Merits of Utilization of MEMS Piezoelectric Devices in Power Converters………………………………………………………… 78
5.5 References……………………………………………………….. 79

6. FABRICATION AND CHARACTERIZATION OF CONTOUR MODE PIEZOELECTRIC AlN MEMS RESONATOR…………………………….. 93

6.1 Fabrication Process on SOI Wafer…………………………………... 94
6.2 Fabrication Process on Si Wafer……………………………………... 96
6.3 Device Characterization……………………………………………... 98
6.4 Appendix………………………………………………………… 104
6.5 References…………………………….................................... 105

7. FEASIBILITY ANALYSIS OF USING MEMS RESONATOR IN SERIES RESONANT CONVERTERS. ……………………………………………. 123

7.1 Inductorless ZVS Condition of MEMS Resonator Based Converter…. 124
7.2 Model Verification………………………………………………….. 133
7.3 Efficiency Analysis of MEMS Resonator Based Converter…………… 134
7.4 Performance Analysis of the Fabricated Device in Series Resonant Converter……………………………………………………………... 136
7.5 References……………………………………………………………. 138

8. CONCLUSIONS………………………………………………………… 156

LIST OF TABLES

2.1 Processing steps to integrate CMOS devices with PV cells…………………… 25

3.1 Cost breakdown of a typical PV power generating system…………………… 46

3.2 Cost breakdown of a typical AC module……………………………………… 46

3.3 Cost breakdown of the proposed system……………………………………… 46

3.4 Failure rate of different components used in power converters………………. 47

3.5 MTBF calculation of proposed embedded converter………………………… 48

3.6 MTBF calculation of the converter constructed from discrete components….. 48

5.1 Estimated comparison of the state of the art devices to MEMS resonator…… 92

6.1 Comparison of the electromechanical properties of three piezoelectric materials……………………………………………………………………… 107

6.2 Materials coefficient of AlN thin film……………………………….…… 107

6.3 Equivalent electrical circuit model parameters of the fabricated resonator corresponding to Fig. 5.1 in Chapter 5 using the data shown in Fig. 6.9a…… 108

6.4 Equivalent electrical circuit model parameters of the fabricated resonator corresponding to Fig. 5.1 in Chapter 5 using the data shown in Fig. 6.10a…. 108

7.1 Equivalent electrical circuit model parameters of the piezoceramic resonator corresponding to Fig. 5.1……………………………………………………. 154

7.2 Comparison of the PT based converters with the microresonator based converter in terms of efficiency and size of the piezoelectric device……………………….. 154

7.3 Comparison of the presented piezoelectric resonator-based converter with recently reported microinductor based converters…………………………………… 155

ACKNOWLEDGEMENTS

Through more than 25 years of schooling, I came across excellent mentors, colleagues, and friends. This journey would have been impossible without their help, suggestions, and guidance. I am grateful to all of them with all my heart.

Beginning graduate school in a completely different culture and environment was the most challenging task, and completing this task has only been possible due to the guidance of my advisor Professor Faisal Khan. His advice on both research as well as other aspects of my life has been priceless. The suggestions and encouragement that I received from him over the last 5 years have helped me to complete this dissertation. I would like to thank Professor Jeffrey Walling not just for being on my committee but also for the support and help he rendered to me during the last 2 years at the University of Utah. Many thanks to Professor Marc Bodson, Professor Hanseup Kim, Professor Mike Scarpulla, and Professor Shad Roundy for being on my committee and for offering valuable suggestions.

I would like to acknowledge the Electrical Power Research Institute (EPRI) and the University of Utah Nanofab Lab for their financial and technical support towards the research that I conducted in my dissertation. My deepest gratitude to Brian Baker at the University of Utah's Nanofab lab. My initial understanding of microfabrication process development came from him. I want to thank all the members of the power engineering and automation research lab for their help and support in various aspects.

Finally, I would like to acknowledge the continuous inspiration from my mother Habiba Begum and my father Md. Abdur Razzaque Bhuiya. Had it not been so, I would not have made it this far. Thank you so much for being an integral part of my journey so far.

CHAPTER 1

INTRODUCTION

The demand for miniaturized autonomous microsystems is increasing for different sensing and monitoring applications. In many applications it is necessary to measure sensor values and then control the actuators accordingly and to interact between different systems (sense/decide/act/communicate) [1]. Hence, autonomous Microsystems are active topics for research. Microbatteries are the conventional way of providing energy to these systems. Contemporary batteries can only supply little total energy (~1–3 J/mm^3) until they run out in 1–3 years. The fabrication of thin film microbatteries requires nonstandard materials and processes [2]. Furthermore, the replacement of these batteries after a certain period becomes another issue. Therefore, the topic of power harvesting is increasingly considered as a key point to the development of autonomous Microsystems [3]. Continuously operated electronic circuits were reported to draw power less than 1μW/mm^2, which can be lowered by running at a low duty cycle. Autonomous devices that are self-powered over their full lifetime by extracting energy from the ambient are crucial for applications such as intelligence, active security, or health monitoring purposes [4]. There are few technological challenges for the implementation of autonomous Microsystems. The biggest one is to harvest energy and increase the total efficiency of the system.

This efficiency is divided into the efficiency of the source itself limited by the physical principles and power electronic circuits' efficiency. These Microsystems incorporate energy sources and energy storage as well as energy management, sensing, and communications circuits. Solar energy harvesting is a potential energy source for autonomous Microsystems [5]. Energy management circuits are necessary to deliver maximum power to different loads in different lighting conditions. Integration of solar cell on a chip by "above-IC" complementary metal oxide semiconductor (CMOS) postprocessing has been reported in the literature [6], [7]. This integration should not compromise CMOS performance. However, extra processing steps are necessary. Interestingly, the fabrication process of a solar cell is mature and very much compatible with CMOS processes. Therefore, it is possible to integrate the power electronic circuit on the same die of a solar cell using the same fabrication process, and this can be used for powering the autonomous Microsystems.

In general, a switching power electronic converter/circuit contains power and control inputs and power output. The input raw power is processed according to the control input, and conditioned output power is produced. Efficiency is the key metric parameter while designing a power converter. Typical components of a power electronic converter include resistive elements, capacitive elements, magnetic devices (inductors and transformers), and semiconductor devices operated mainly in switched mode. Capacitors and magnetic devices are essential parts of a power converter because ideally they should not consume power. For the same reason, semiconductor devices are operated as switches—either ON with substantial current with a very small voltage drop or OFF with a substantial voltage drop but nearly zero current.

A periodic switching pattern creates rectangular voltage or current waveforms, which needed to be filtered to obtain a DC output. An RC filter is not an option due to losses, so an LC filter is used. One way to think about the roles of the passive reactive components is that they store energy on time scales similar to the switching period. Therefore, the energy that must be stored in the passive components is inversely proportional to frequency 0. Therefore, the increment of the switching frequency in order to reduce the size of passive components has played a key role in the advancement of power electronics.

1.1 Recent Trend in Power Supply Design

Consumers of electronic product have become accustomed to miniaturization and increased levels of functional integration in electronic devices. Cell phones are not simply a device with basic call capability with a monochrome display but a feature-rich computer with GPS, Internet connectivity, PDA functionality, cameras, music players, and high-resolution touch screens. The age old printed circuit board based power supply technology has been impacted by this continuous integration in recent times. A tremendous amount of research is going on to reduce the area and volume occupied by the power converters. Therefore, the converters can be designed for space-constrained and miniaturized applications. Integrating components may provide higher reliability. This can reduce assembly and inventory costs also.

Research advances in semiconductors, magnetics, capacitors, and packaging technologies are driving these integrated solutions of power converters. The following are the technology integration definitions by the Power Sources Manufacturers Association

(PSMA) [9]:

- Power Supply in Package (PSiP) – Separate ICs (switch drivers, controller) within the same package with external (off chip) inductors.
- Power IC: Switch drivers, switches, and control circuits on a single chip with external (off chip) inductors.
- Power Supply on a Chip (PwrSoC) – Switch drivers, switches, and control circuits on a single chip with integrated (on chip) inductors.

Fig. 1.1 shows the envisioned evolution of the power converter from discrete "power supply on printed circuit board (PCB)" solutions to the PwrSoC technology. PSiP and power ICs technologies are very similar technologies, where the later is suitable for only low power converters (<10 W). The integration of controllers and switch drivers is not feasible for high power converters because the chips are fabricated in different voltage processes (i.e., the controllers are fabricated on a low-voltage process, and the switch drivers are fabricated on a high voltage process). Therefore, PSiP is the suitable technology for higher power. Vicor manufactures many high power converters with PSiP technology.

Many companies such as Enpirion, Fuji, Micrel, National Semiconductor, and TI have been manufacturing products with PSiP and Power IC technology. Enpirion [10] and Micrel [11] copackaged the inductor in a plastic encapsulated package on the same lead frame as the adjacent PMIC. On the other hand, Fuji [12] and National Semiconductor [13] used ceramic ferrite inductor, which acts as a chip scale substrate on which the PMIC is mounted. 3-D stacked PSiP technology has been demonstrated by TI [14] . Few commercially available PSiP and power IC products are given [15]–[22].

Interestingly, there is no commercial product demonstrating the PwrSoC technology to date. This technology is still in the research phase. Only a few articles [23]–[29] have reported the true PwrSoC where the air core inductors are monolithically integrated with the power IC. The switching frequencies of these converters are greater than 50 MHz; thus the air core inductor is sufficient for the power conversion. Obviously, inductance density of air core is much lower than the conventional ferrite core transformer.

The main focus of research towards PwrSoC is on integrating the inductor. Many articles have been published on this integration and are well summarized in [30]–[31]. The performance of these inductors is analyzed in [32]–[33]. Different magnetic materials such as Co–Zr–Ta, Ni–Fe, etc., have been investigated for this purpose. In addition, a number of coil and winding geometries such as spiral, stripe, toroidal, solenoid, etc., have been investigated as well. In this regard, a completely different device such as a thin film piezoelectric resonator has been considered as a potential candidate in this dissertation as a replacement for on-chip inductors in power conversion applications.

1.2 Piezoelectric MEMS Resonator

Advances in MEMS design and fabrication enabled growth of piezoelectric resonators span a frequency range from 10s to 100s of MHz on a single substrate. A mechanical motion is produced in the piezoelectric layer when a RF signal is applied across the device. The fundamental resonance is observed when the thickness of the film is equivalent to half the wavelength of the RF signal. Therefore,

$$v = \sqrt{\frac{E}{p}} \tag{1.1}$$

and

$$f = \frac{v}{2d} \tag{1.2}$$

where E, p, d, and v are the elastic constant, density, thickness, and acoustic velocity of the film, and f is the resonant frequency of the resonator [34]. The quality factor of the microresonator is significantly higher than the discrete L-C resonators and ceramic resonators [35].

These resonators are attractive as an on-chip resonator for different reasons:

- Compatibility of thin film devices with silicon and silicon processes.
- The acoustic and electrical properties of piezoelectric material (such as AlN and ZnO) are very attractive.
- The plate capacitor of the device ensures good performance against electrostatic discharge (ESD) and electromagnetic interference (EMI) compared to discrete L-C resonators.

1.3 Outline of Thesis

The dissertation is organized in the following chapters.

In Chapter 2, a literature review on macroelectronics or surface electronics is given at the beginning, followed by a literature review on integrating discrete components such as inductors, capacitors, field effect transistors (FET) etc., on-chip is given. A literature review on existing embedded power converters is also given in Chapter 2. The proposed CMOS compatible process to integrate MOS switches, capacitors, and diodes on the same die of a PV cell in the same process run is described next. With an embedded

power-conditioning circuit, PV powered autonomous Microsystems can be constructed using the proposed process. Simulation results of the proposed process are included in Chapter 2 also.

In Chapter 3, the advantages of the embedded power converter for PV power generation is discussed. Challenges to address for the proposed integration are also described in that chapter.

The proposed process is implemented and the experimental results are shown in Chapter 4. The characteristics of different components are depicted first followed by the performance of an embedded power converter for PV power generation. Light generated effects on the FETs are included at the end of Chapter 4.

As described earlier, inductive components are mandatory to achieve dynamic voltage scaling, and this dynamic voltage scaling is an essential feature for a renewable energy harvesting system. A piezoelectric microresonator on Si is proposed in Chapter 5 to replace the on-chip inductor for power converters. Brief discussions about the operating principles and characteristics of the proposed MEMS resonator vibrating in contour mode are provided. A literature review on utilization of piezoelectric devices such as bulk piezoelectric transformers in power conversion is described in Chapter 5 also.

The detailed fabrication process of the contour mode piezoelectric AlN MEMS resonator on Si is described in Chapter 6. The fabricated devices have been characterized and the experimental results are provided in this chapter also.

The feasibility of using this MEMS device in a series-resonant converter is discussed in Chapter 7. Inductorless zero voltage switching (ZVS) in a resonant converter can be

achieved using this device, and a state space model for this ZVS condition is provided in Chapter 7 also with experimental validation. An analysis of the efficiency of the device in the same converter is performed as well. Finally, the superior electromagnetic interference (EMI) performance of the device is proved through experimental results at the end of Chapter 7.

Finally, Chapter 8 summarizes the work presented in this dissertation. Future directions of the MEMS resonator based embedded power converter research are also provided in the final chapter

1.4 References

[1] E. Mackensen *et al*., "Smart wireless autonomous microsystems (SWAMs) for sensor actuator networks," in *Proc. ISA/IEEE Sensors for Industry*, 2004, pp. 72–78,.

[2] W.C. West *et al*., "Lithium microbattery development at the jet propulsion laboratory," *IEEE Aerosp. Electron. Syst. Mag*., vol. 16, no. 8, pp. 31–33, Aug. 2001.

[3] M. Ferrari *et al*., "Modeling, fabrication and performance measurements of piezoelectric energy converter for power harvesting in autonomous microystems," *IEEE. Trans. Instrum. Meas*., vol. 55, no. 6, pp. 2096–2101, Dec. 2006.

[4] J. Penders *et al*., "Human++: from technology to emerging health monitoring concepts," in *Symp. Medical Devices Biosensors*, 2008, pp. 94–98.

[5] N. K. Pour *et al*., "A reconfigurable micro power solar energy harvester for ultra-low power autonomous microsystems," in *IEEE Int. Symp. Circuits Systems*, 2013, pp. 33–36.

[6] J. Lu *et al*., "Above CMOS a-Si and CIGS solar cells for powering autonomous microsystems," in *IEEE Int. Electron Device Meeting*, 2010, pp. 31–34.

[7] J. Lu *et al*., "Integration of solar cells on top of CMOS chips part 1: a-Si solar cells" IEEE Tran. Elec. Devices, vol. 58, no. 7, pp. 2014–2021, Jul. 2011.

[8] C. R. Sullivan, "Integrating magnetics for on-chip power: Challenges and opportunities," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2009, pp. 291–298.

[9] F. Waldron *et al*. “Technology roadmapping for power supply in package (PSiP) and power supply on chip (PwrSoC),” *IEEE Tran. Power Electron.*, Vol. 28, no. 9, pp. 4137–4145, Sept. 2013.

[10] Altera. (2014). *Enpirion product, EN5322Q* [Online]. Available: http://www.altera.com.

[11] Micrel. (2014). *Micrel product, MIC3385* [Online]. Available: http://www.micrel.com.

[12] Fuji. (2014). *Fuji product, FB6831* [Online]. Available: http://www.fujielectric.com.

[13] Texas Instruments. (2014). *National Semiconductor Product, LM3218* [Online]. Available: http://www.ti.com.

[14] Texas Instruments. (2014). *TI product, TPS82671* [Online]. Available: http://www.ti.com.

[15] Vishay. (2014). *Vishay product, FX5545G108* [Online]. Available: http://www.vishay.com.

[16] Bel Power. (2014). *Bel Power product, SRAH-12Fxx0* [Online]. Available: http://www.pwrsoc.com.

[17] Delta Electronics. (2014). *Delta Electronics product, IPM04S0A0S10FA* [Online]. Available: http://www.digikey.com.

[18] Linear Technology. (2014). *Linear Tech product, LTM4608* [Online]. Available: http://www.linear.com.

[19] Murata. (2014). *Murata product, MPD6S022 S* [Online]. Available: http://www.power.murata.com.

[20] Intersil. (2014). *Intersil product, ISL8201M* [Online]. Available: http://www.intersil.com.

[21] ROHM. (2014) *ROHM product, BP5275* [Online]. Available: http://www.rohm.com.

[22] Lineage Power. (2014) *Lineage Power product, PicoTLYnx* [Online]. Available: http://www.lineagepower.com.

[23] J. Wibben and R. Harjani, “A high-efficiency DC–DC converter using 2 nH integrated inductors,” *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 844–854, Apr. 2008.

[24] M.Wens and M. S. J. Steyaert, “A fully integrated CMOS 800-mW fourphase semiconstant ON/OFF time step-down converter,” *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 326–333, Feb. 2011.

[25] J. T. DiBene *et al*., “A 400 Amp fully integrated silicon voltage regulator with in-die magnetically coupled embedded inductors,” in *Proc. Applied Power Electronics Conf.*, 2010, pp. 1381–1390.

[26] H. Nakazawa *et al*., “Micro-DC/DC converter that integrates planar inductor on power IC,” *IEEE Trans. Magn.*, vol. 36, no. 5, pp. 3518–3520, Sep. 2000.

[27] M. Alimadadi *et al*, “A fully integrated 660 MHz low-swing energyrecycling DC–DC converter,” *IEEE Trans. Power Electron.*, vol. 42, no. 6, pp. 1475–1485, Jun. 2009.

[28] J. Ni *et al*., “Improved on-chip components for integrated DC–DC converters in 0.13 μm CMOS,” in *Proc. 35th European Solid-State Circuits Conf.*, 2009, pp. 448–451.

[29] S. Musunuri and P. L. Chapman, “Design of low power monolithic DC–DC buck converter with integrated inductor,” in *Proc. IEEE Power Electron Speccialists Conference*, 2005, pp. 1773–1779.

[30] D. S. Gardner *et al*., “Review of on chip inductor structures with magnetic films,” IEEE Trans. Magn., vol. 45, no. 10, pp. 4760–4766, Oct. 2009.

[31] C. O. Mathuna *et al*., “Review of integrated magnetic for power supply on chip (PwrSoC),” *IEEE Tran. Power Electron*., vol. 27, no. 11, pp. 4799–4816, Nov. 2012.

[32] R. Meere *et al*., “Size and performance tradeoffs in micro-inductors for high frequency DC-DC conversion,” *IEEE Tran. Power Electron*., vol. 45, no. 10, pp. 4234–4237, Oct. 2009.

[33] R. Meere *et al*. “Magnetic-core and air-core inductors on silicon: A performance comparison upto 100 MHz,” *IEEE Trans. Magn.*, vol. 47, no. 10, pp. 4429–4432, Oct. 2011.

[34] P. Osbond *et al*. “The influence of ZnO and elelctrode thickness on the performance of thin film bulkacoustic resonators,” in *Proc. IEEE Ultrasonics*, 1999, pp. 911–914.

[35] R. Ruby, “ A decade of FBAR success and what is needed for another successful decade,” in *Symp. Piezoelectricity, Acoustic Waves Device Application (SPAWDA)*, 2011, pp. 365–369.

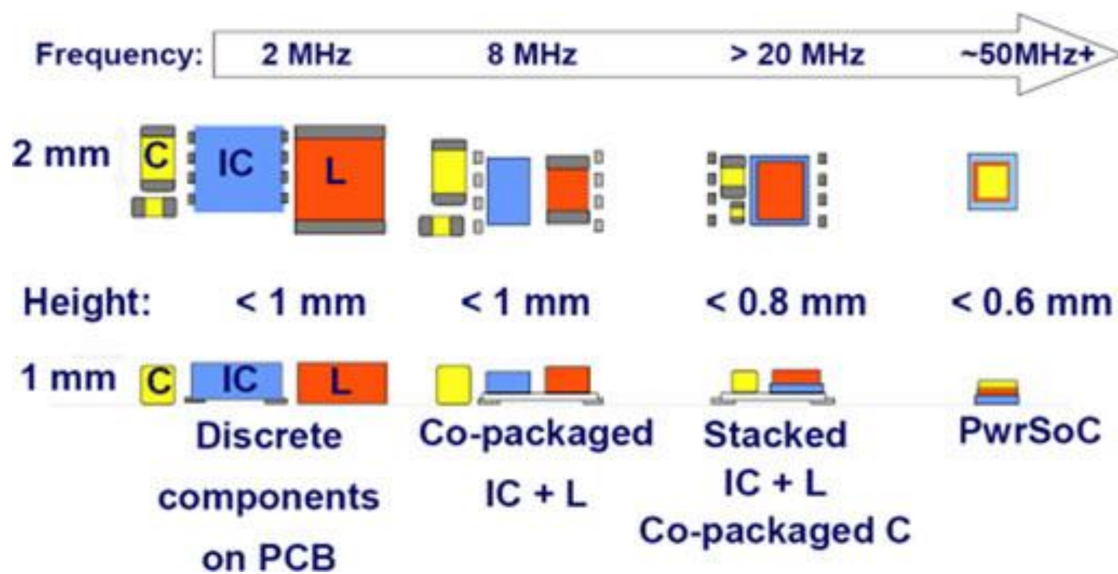


Fig. 1.1: Vision for evolution of PwrSoC technology (Courtesy of Mathuna et al. © 2012 IEEE) [31]

CHAPTER 2

MONOLITHICALLY EMBEDDED POWER CONVERTERS FOR PV POWER GENERATION

The use of large area electronics or macroelectronics is a relatively recent idea. However, significant work has been done to integrate the display driver circuitry on the same substrate with the display itself used in large screen TV monitors. Therefore, there exist many success stories in the literature in this regard [1]. On the other hand, electronic components such as power semiconductor switches, resistors, capacitors, inductors, and other passive elements have been used in the form of discrete components on printed circuit boards (PCB) for several decades. However, the amount of work to integrate these components on the wafer level using custom fabrication processes is insignificant. Therefore integration of components in this form can significantly reduce space and weight compared to standard printed circuit board approaches.

Conventional discrete electronic circuits may not be the most suitable for spreading the components over a large area in order to monitor and address the partial shading problems in a PV system. In addition, surface electronics could be used to address several major failures such as the partial shading, formation of hotspots, bypass diode failure, module cracking, and arcing. Poor interconnection is a key reason for many of these failures.

Other than power electronics, several other research areas such as X ray imaging, solid state lighting with integrated driver circuitry, intelligent smart grid, medical application such as “sensitive skins” [2], etc., require the use of planar electronics. Fabrication challenges in these areas have not been properly addressed using traditional Si CMOS microelectronics. Several other reports have been found on the Department of Defense’s (DOD) project of macroelectronics to improve the mission capability of unmanned aerial vehicles (UAVs). To address additional communication in UAV avionics, it needs to incorporate flexible plastics antennas with flexible active circuitry such as low-noise amplifiers (LNAs), RF switches, and digital control circuits.

Some of the macroelectronics projects of NASA include solar sails (kilometer wide light membrane of solar cells) with integrated sensors for health monitoring and reshaping the sail. Therefore it is beneficial to integrate sensors and control circuits with the membrane in order to reduce weight and achieve additional features. The idea of macroelectronics can be used with renewable energy sources by integrating the power converter circuit on the same wafer/substrate used to build the solar energy harvesting devices. Unfortunately, no previous work has been found in the literature on this application of macroelectronics. The concept of an on-die power conversion unit is becoming more prevalent in microprocessors. Although DC-DC converters have been monolithically fabricated for low-power applications, no attempts have been made to use them in the embedded fashion for PV power generation in critical applications such as in battlefield or scientific expedition. Recently, PV cells have been widely utilized to power wireless sensor network (WSNs) and autonomous microsystems for biomedical applications [3], [4]. Embedding PV cells in the substrate could be an efficient way for

generating power on chip. The limited power generated by the embedded PV cell could be sufficient for circuits designed especially for low-power operation leading to autonomous microsystem.

2.1 Existing Microfabrication Processing for On-Chip Components: A Literature Review

2.1.1 Silicon Processing for PV Fabrication

Today's PV production is dominated by Crystalline silicon (c-Si) based technologies [6]. Single crystal (SC-Si) technologies have several advantages such as i) an established technology base, ii) superior material quality, and iii) improved efficiency and stability over the two other conventional solutions (thin film and polycrystalline). For integration purposes, SC-Si technologies must be explored first. The individual components of grid tied inverters (MOSFETs, diodes, inductors, and capacitors) have already been fabricated on the c-Si wafer to implement power processing units inside microprocessors. Moreover, the efficiency of cells made from SC-Si is higher than that of all multi-crystalline and thin film solar cells (those have been developed so far) [6] by a significant amount, and solar cells with efficiency of 20%–26% on commercialized Czochralski (Cz) wafers have been reported.

The main disadvantage of SC-Si is the higher fabrication cost compared to multicrystalline and thin film solar cells [6], and this additional cost can be justified if the combination of the cell and the power processing unit could achieve an extended lifespan. Moreover, SC-Si based solar cells require the smallest footprint for a certain power level, and this is advantageous over other PV technologies when space issue is prevalent, such

as in a battlefield.

2.1.2 Silicon Processing for Circuit Components Fabrication

In general, a typical power converter may have six different kinds of active and passive components. These components are 1) capacitor, 2) power switch, 3) inductor, 4) diode, 5) resistor, and 6) any integrated circuits for gate driving and control. The following paragraphs explain how these components could be accommodated on Si using the same process.

2.1.2.1 Capacitors

There are many known techniques to form capacitance on Si. The electrolytic capacitor used at the DC bus of the inverter can be replaced by a metal-silicon capacitance with an internal SiO_2 layer. Using a conventional 0.35 µm CMOS foundry process, it is possible to grow polydiffusion capacitance of about 5 nF/mm^2 with an oxide thickness of 5–10 nm [7]. Making high aspect ratio pores in Si by deep reactive ion etching (DRIE), 30 nF/mm^2 capacitance can be realized with standard insulator (SiO_2/Si_3N_4) [8]. Moreover, insulators with high a dielectric constant (Al_2O_3) can produce very high capacitance (440 nF/ mm^2) while fabricating higher aspect ratio pores [9]. MIM (metal- insulator-metal) capacitance is promising to give the highest capacitance for the integration purposes (5–40 nF/ mm^2) [10], [11].

2.1.2.2 MOSFET

Commercially available power MOSFETs are trench MOSFETs. A detailed literature study reveals various techniques for trench MOSFET fabrication [12]–[14]. Reference [14] shows good process steps that can be easily integrated with the power diode.

2.1.2.3 Inductor

The idea of “power supply on chip” or “system on chip” for high power conversion is a relatively recent idea. However, no single on-chip power converter has been reported in literature yet offering high efficiency and adjustable conversion ratio [15] at the same time. Switched capacitor integrated voltage regulators (IVR) can provide high efficiencies at reasonable current densities; however, achieving dynamic conversion ratio is very challenging with switched capacitor IVRs [15], [16]. Switched inductors converters (such as a buck converter) can provide high efficiency and high current density, as well as offer a continuous range of conversion. The bottleneck of this switched inductor IVR is the integration of power inductors [17], [18] on silicon.

Very recently, on chip inductors having spiral geometry and fabricated without magnetic materials exhibit inductances ranging from 1–10 nH. The densities of these inductors are lower than 100 nH/mm^2, occupying a large substrate area. To fabricate a magnetic film that is compatible with standard CMOS processing technology is a challenging task. The magnetic material should have high temperature stability, a good deposition and etching technique, and compatibility with Si technology. Moreover, increasing inductance typically involves increasing the magnetic film thickness, which in turn results in increased eddy currents; therefore, the peak quality factor is reduced.

The high quality factor inductors seem to have lower inductance density too. Therefore, significant research is still in place to design on-chip inductors with a high quality factor and small footprint. Different magnetic materials such as Co–Zr–Ta, Ni–Fe, etc., have been investigated for this purpose. In addition, a number of coil and winding geometries such as spiral, stripe, toroidal, solenoid, etc., have been investigated as well.

2.1.3 Si or SiC/GaN: Choice of Materials

Some of the favorable features of the wide band gap materials such as GaN and SiC are order of magnitude higher electrical field and three to five times higher thermal conductivity, higher breakdown voltage, higher doping density, and carrier lifetime. These properties contribute to the following reasoning: high Si–C bond strength facilitates towards higher breakdown voltage; due to high bandgap, higher temperature is needed to transfer carriers from valance to conduction band giving high-temperature withstanding capability. In addition, reduced carrier lifetime leads to faster switching capability [21].

However, the mass development of these devices is still limited by difficulties in crystal growth and material properties. The SiC wafers suffer from major impurities known as micropipes. A significant amount of research was conducted to reduce the density of these defects from hundreds per cm^2 to only a few per cm^2 or even a few per wafer depending on the cost. SiC power diodes are available from Cree, Infineon for a decade.

For low to medium voltage operation, devices with high breakdown voltage may not

add a significant value. A slight increase in efficiency may not be attractive if the cost is very high. However, reliability at high temperatures can be the decisive factor only if the SiC/GaN devices can overcome the prevalent cost issues [22]. SiC/GaN devices seem to be more suitable in renewable energy sectors or in harsh environments, like in space, given that the slight increase in efficiency and high temperature operation can be justified as cost increases.

Other than a slight increase in efficiency and power density, SiC/GaN cannot offer any other favorable features compared to those of Si devices. However, for high power/voltage DC-DC converters such as in accelerators or pulsed power converters for medical systems where a high output voltage is required, SiC/GaN devices can offer a big improvement. In addition, the recent adoption of micro-/nanogrid would be highly unrealistic without the high voltage, high temperature, and low footprint capability offered by the SiC/GaN devices. Therefore, it is apparent that SiC/GaN can go a long way for high power and high voltage operation even considering the higher cost.

In the embedded PV research, the converters are supposed to handle low power as well as low voltage. For low voltage applications, the higher cost incurred by the SiC or GaN devices may not be justified, although other advantages are present. Moreover, the technology to fabricate defect free SiC/GaN is still not mature and therefore, it is a natural choice to investigate the integration capability of Si devices as they use a very mature technology.

2.1.4 Existing Monolithic Power Converter Solutions

The concept of an on-die power conversion unit is becoming more prevalent in microprocessors. However, the power-handling capability of these converters is relatively small, and the same concept could be used in order to design larger converters for photovoltaic applications. Although DC-DC converters have been monolithically fabricated for low-power applications, no attempts have been made to use them in the embedded fashion for PV power generation. In the CMOS process, a linear regulator (LR) could be considered as an excellent candidate because of magnetic-element-free operation. However, linear regulators suffer from an inferior efficiency profile, and these designs do not achieve dynamic voltage regulation. In order to overcome this limited efficiency barrier, switched-capacitor (SC) DC-DC converters have been proposed in the literature [23], [24]. The major limitation of many SC converters is the inability to produce the necessary variable conversion ratio (CR). Reference [25] presents an improved SC DC-DC converter with controllable CR, which was implemented using multiple pumping capacitors.

2.2 Fabrication

Power converter circuits either use capacitors or inductors to transfer energy. Due to the fabrication complexity involved with inductors [7] and substantial development of on-die Si-capacitors [7]–[9], SC circuits are considered to be the most suitable candidate for embedded PV power converters. Switched capacitor converters are also being used in the PV converters [26], [27] in recent days. The feasibility of maximum power point tracking (MPPT) using switched capacitor converter is described in [26], and a low

power SC DC-DC converter is used to charge a battery is presented in [27]. In this regard, a CMOS compatible process was proposed by the authors to fabricate converter components along with the PV cells on the same die (Table 2.1). The process steps are depicted in Fig. 2.1. If the converter is integrated only for a few cells, converters constructed from CMOS switches could easily withstand the low voltage and current stress. Moreover, fabrication of several low power converters will not be an issue as the process is compatible with standard CMOS process, and the feasibility of the implementation of these low power converters can be found in [28].

2.3 Justification of the Proposed Device Architecture

In the standard CMOS process, there are four possible structures of an MOS switch. An NMOS fabricated on the *p*-substrate is shown in Fig. 2.2a. The *P* side (anode) of a *p*-*n* junction PV cell typically has a higher biasing voltage than the *n* side (cathode). In CMOS circuits, the *p*-*n* junction between the source/drain and substrate is reverse-biased; therefore, no current flows through the substrate. If the device structure of Fig. 2.2a is chosen, source/drain of NMOS always needs to have a higher voltage compared to the *p*-substrate (anode of PV cell), which is not feasible because two sources needed to be connected to the cathode of the PV cells to form an H-bridge. Also, a higher threshold voltage will be necessary because the substrate (anode of the PV cell) voltage is not set to zero.

PMOS on the *p*-substrate structure is shown in Fig. 2.2b. The same issue discussed in the previous paragraph exists here as well; the *n*-well/body needs to be at higher potential than the substrate. This can be achieved by connecting the *n*-well/body to the high

voltage bus of the chip. However, *p*-type transistors are not optimum for power converter circuits due to lower mobility issues.

The third structure is PMOS on the *n*-substrate (Fig. 2.2c). As the *n*-substrate is the cathode of the PV cell, it will be the ground (GND) terminal of each segments of the multilevel inverter. Therefore, negative voltage will be necessary to turn on these switches, which is not trivial for integrated circuits.

Based on the above phenomenon, NMOS on *n*-substrate was the best option for the embedded power converter for the AC solar cell (Fig. 2.2d). In this structure, the body terminal is not connected with the source, meaning the NMOS has four terminals—gate, drain, source and body unlike conventional three terminal devices. *P* well or body terminal can be tied with the *n*-substrate or the cathode (GND) of PV cells, in order to make sure this diode will not conduct. Therefore, the drains and sources can be connected to various other devices without any apparent issues.

In addition, simplified gate drivers could be used by virtue of the four terminal structure. The gate pulse applied to the device will be referenced to the GND of one segments of the multilevel inverter. Because the body or the well of each of these devices is connected to this GND (*n*-substrate), NMOS will function properly without the need of any complex gate drive circuits, making power processing simpler. The drawback of this structure is that commercial CMOS foundries like MOSIS or X-FAB do not offer this structure; however, Fig. 2.2a and Fig. 2.2b are available commercially because these structures can be used to make complex circuits with only two supply voltages (5 V and 0 V). Therefore, by designing a new fabrication process, Fig. 2.2d can be considered as the most suitable structure for the proposed embedded power converters.

2.4 Simulation Results

The simplified process described in the previous section has been implemented in the ATHENA [29] process simulator, and the fabricated device characteristics have been obtained using the ATLAS [30] device simulator. These characteristics have been shown in Fig. 2.3. The integrated PV cell has a fill factor of 76%, and the efficiency is found to be 14%. The Atlas software takes a significant amount of time to generate simulation results due to the complexity of the device. In order to reduce simulation time, the Si substrate was considered only 12 μm thick, which is very thin to absorb light properly. Therefore, the open circuit voltage, current density, and efficiency are found to be lower than usual (Fig. 2.3a). The simulated value of the metal polycapacitor was 4 nF/mm^2, and the MOSFET's threshold voltage and breakdown voltage were achieved as 0.75 V and 9 V, respectively (Fig. 2.3b & 2.3c).

The boosting operation of the embedded MMCCC power converter is illustrated in Fig. 2.4—the input was a PV cell with constant illumination and output load was 25 Ω. This entire converter was fabricated in the ATHENA process simulator and simulated in Smart Spice of Silvaco, and the simulation results are shown in Fig. 2.5

2.5 References

[1] T. Afentakis *et al.*, " High performance poly-silicon thin film transistor circuits on flexible stainless steel foils," in *Symp. Material Research Society*, 2003, pp. 212–228.

[2] V. Lumelsky *et al.*, "Sensitive skin," *IEEE Sensors J.*, vol. 1, no. 1, pp. 41–51, Jun. 2001.

[3] O. Bulteel *et al.*, "High efficiency solar cell embedded in SOI substrate for ULP autonomous circuits," in *Proc. IEEE International SOI Conf.*, 2009, pp. 1–2.

[4] B. A. Warneke *et al.*, "An autonomus 16 mm solar powered node for distributed

wireless sensor networks," in *Proc. IEEE Senors*, 2002, pp. 1510–1515.

[5] C. Chen *et al*., "SOI cicuits powered by embedded solar cells," in *Proc. IEEE International SOI Conf*., 2011, pp. 211–214.

[6] D. D. Malinoskova, "Photovoltaic and photoactive paterials - properties, technology and applications," *NATO Sci. Ser., II*, vol. 80, pp. 11– 48, Sep. 2001.

[7] S. C. O Mathuna, *et al*., "Magnetics on silicon : an enabling technology for power supply on chip," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 585–592, March 2003.

[8] F. Roozeboom, "High-density, low-loss MOS capacitors for integrated RF decoupling," *Int. Symp. Microelectronics*, 2001, pp. 477–483.

[9] J. H. Klootwijk *et al*., "Ultrahigh capacitance density for multiple ALD-grown MIM Capacitor Stacks in 3-D silicon," *IEEE Electron Device Lett.,* vol. 29, no. 7, pp. 740–742, July 2007.

[10] M. Gros-Jean *et al*., "High linear Ta2O5 MIM capacitor embedded in Al-interconnected BICMOS technology," in *Proc. WODIM Conf.*, 2002, pp. 73–76.

[11] E. Fribourg-Blanc *et al*., "PMNT films for integrated capacitors," in *Proc. WODIM Conference*, 2002, pp. 89–92

[12] S. M. Sze*, Physics of Semiconductor Devices*, 2nd ed., New York: John Wiley, 1981.

[13] V. A. K. Temple *et al.* , "A 600-V MOSFET designed for low on-resistance," *IEEE Trans. Electron Devices,* vol. 27, no. 2, pp. 343–348, Feb. 1980.

[14] K. Shenai, "Optimally scaled low-voltage vertical power DMOSFET's for high-frequency power switching applications," *IEEE Trans. Electron Devices,* vol. 37, no. 4, pp, 1141–1153, Apr. 1990.

[15] C. O. Mathuna *et al*., " Review of integratred magnetics for power supply on chip (PwrSoC)," *IEEE Trans. Power Electron*., vol. 27, no. 11, pp. 4799–4816 Nov. 2012.

[16] L. Chang *et al*., "A fully integrated switched capacitor 2.1 voltage converter with regulation capability and 90% effcieency at 2.3A/mm^2," in *IEEE Symp. VLSI Circuits*, 2010, pp. 55–56.

[17] H. Le *et al.*, "A 32 nm fully integrated reconfigurable switched capacitor DC–DC converter delivering 0.55 W/mm^2 at 81% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2010. pp. 210– 211,

[18] J. T. DiBene *et al*., "A 400 amp fully integrated silicon voltage regulator with in-die magnetically coupled embedded inductors," in *Proc. IEEE Applied Power*

Electronics Conf., 2010, pp. 212–219.

[19] G. Schrom *et al.,* "A 60MHz 50W fine grain package integrated VR powering a CPU from 3.3V," in *Proc. IEEE Applied Power Electronics Conf.*, 2010, pp. 121–129.

[20] D. Gardner *et al.,*"Review of on-chip inductor structures with magnetic films," *IEEE Trans. Magn.*, vol. 45 no. 10, pp. 4760–4766, Oct. 2010.

[21] J. A. Carr and D. Hotz, "Assessing the impact of SiC MOSFETs on converter interfaces for distributed energy resources," in *Proc. IEEE Industrial Applications Conf.*, 2007, pp. 336–341.

[22] J. Biela *et al*., "Sic vs. Si – evaluation potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductor," *IEEE Trans. Ind. Electron*, vol. 58, no. 7, pp. 2872–2882, Sept. 2010.

[23] S. Al-Kuran *et al*., "GaAs switched capacitor DC-to-DC converter," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1121–1127, Aug. 2000.

[24] D. Ma *et al*., "Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems," *J. Analog Integr. Circuits Signal Process.,* Vol. 62, no. 3, pp. 361–372, Mar. 2010.

[25] I. Chowdhury and D. Ma, "Design of reconfigurable and robust integrated SC power converter for self-powered energy-efficient devices," *IEEE Trans. Ind. Electron.,* vol. 56, no. 10, pp. 4018–4025, Oct. 2000.

[26] J. J. Cooley and S. B. Leeb, "Per panel photovoltaic energy extraction with multilevel output DC-DC switched capacitor converters," in *Proc. IEEE Applied Power Electronics Conf.,* 2011, pp. 419–428.

[27] P. K. Peter and V. Agarwal, " A compact switched capacitor DC–DC converter based global peak power point tracker for partially shaded PV arrays of portable equipment," in *Proc IEEE Photovoltaics Specialists Conf.* , 2011, pp. 194–199.

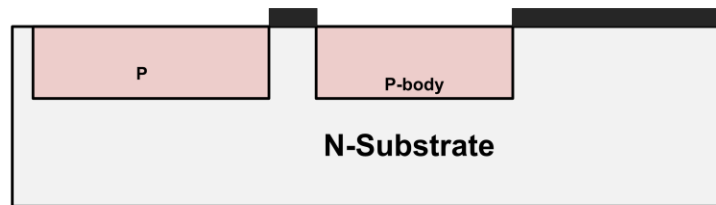
[28] B. Johnson *et al*., "Photovoltaic AC module composed of a very large number of interleaved inverters," in *Proc. IEEE Applied Power Electronics Conf., 2011*, pp. 976–981.

[29] Silvaco. (2014). [Online]. Available: http://www.silvaco.com/products/tcad/process_simulation/athena.html.

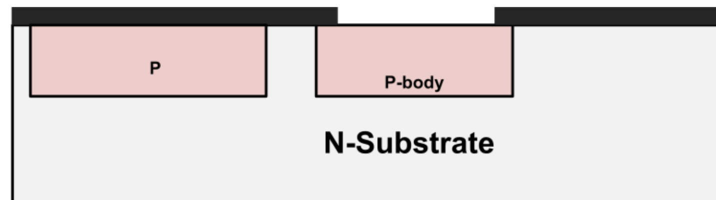
[30] Silvaco. (2014). [Online]. Available: http://www.silvaco.com/products/tacd/device_simulation/atlas.html.

Table 2.1: Processing steps to integrate CMOS devices with PV cells

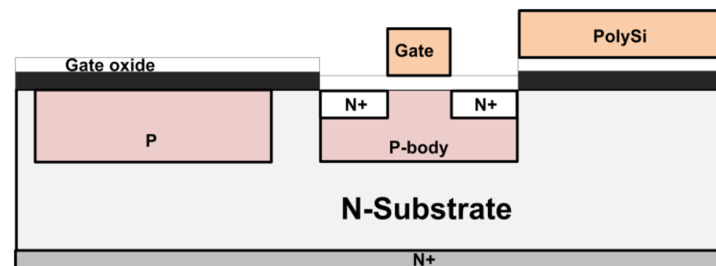
1.	Using an Oxide mask, Boron diffusion (doping density about $2x10^{17}$ cm^{-3}) through ion implantation (120 keV) is carried out to create a 0.8 µm deep p-type body region (p-well) as well as an anode region for PV (Fig. 2.1a).
2.	The second oxide mask blocked the region for the PV cell and opened up the area for the active region (Fig. 2.1b)
3.	10 nm of gate oxide are grown thermally. 1000 nm of polysilicon is deposited by the low pressure chemical vapor deposition (LPCVD) process. This polysilicon layer was patterned to open areas for source and drain (third mask). The remaining polysilicon layer acts as a gate as well as one electrode of the capacitor (Fig. 2.1c)
4.	Ion implantation is carried out to form n+ source region and n+ drain region of the MOSFET (Phosphorus doping of $1x10^{20}$ cm^{-3}, 80 keV) (Fig. 2.1c). The polysilicon layer also gets doped to reduce its resistivity.
5.	A 500 nm thick intermetal oxide layer is deposited by the LPCVD process. The fourth mask is used to open windows in the inter-metal dielectric film for contacts. A Ti/Al layer (0.4–0.8 µm) is deposited by the sputtering process. Patterning of Al (fifth lithographic step) is done to separate gate, capacitor’s upper and lower electrodes, source, drain, and emitter (of solar cell).
6.	The next mask opens up the area for bond pads, and the final mask is used to pattern them. In this way, six pads are created for six terminals—gate, capacitor’s upper and lower electrodes, source, drain, and emitter (of solar cell).
7.	A metal stack is deposited on the back surface to create the contact for the base of the solar cell (Fig. 2.1d). A metal stack consists of a thin Ti film, a thin Ni barrier layer, and a thick Al layer. This stack functions as a heat sink for the entire structure also.



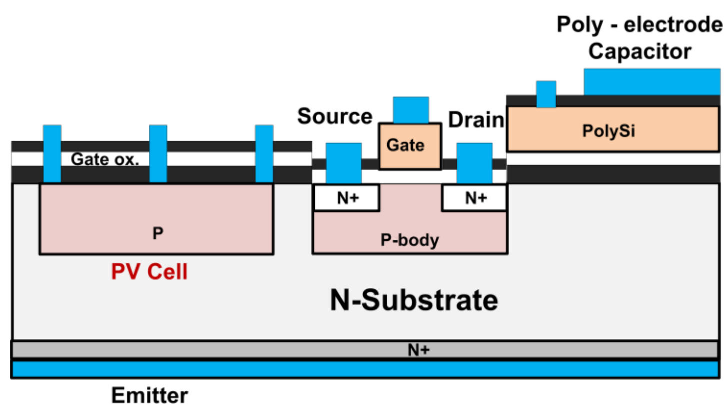
(a)



(b)

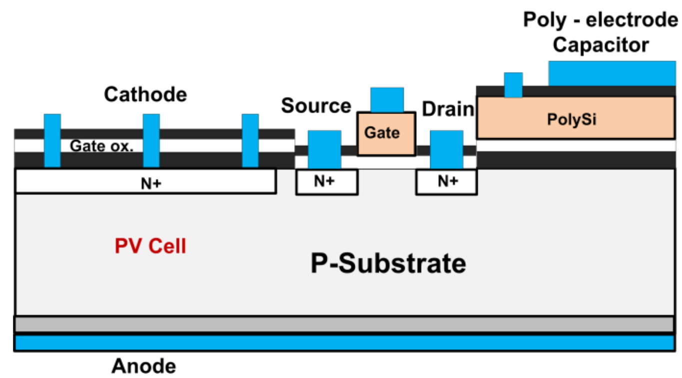


(c)

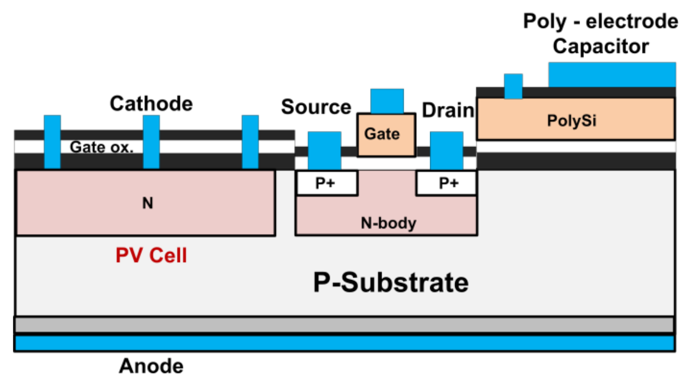


(d)

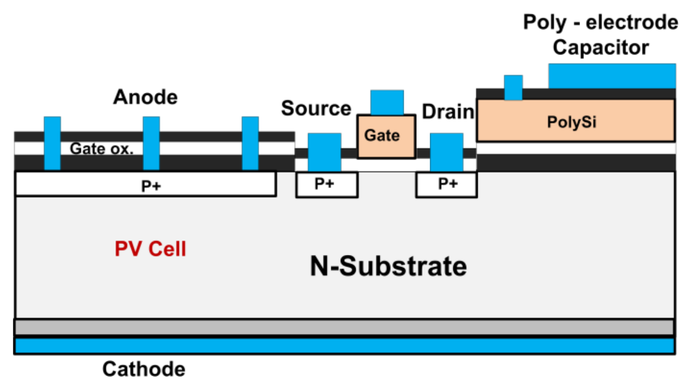
Fig. 2.1: Key processing steps for fabricating MOSFETs, capacitors with the PV cells (cross-sections are not drawn to the scale) (a) p body and PV cell's anode formation, (b) Mask 2, active region for MOSFET, (c) polysilicon patterning and source-drain implantation, (d) complete device cross-section.



(a)

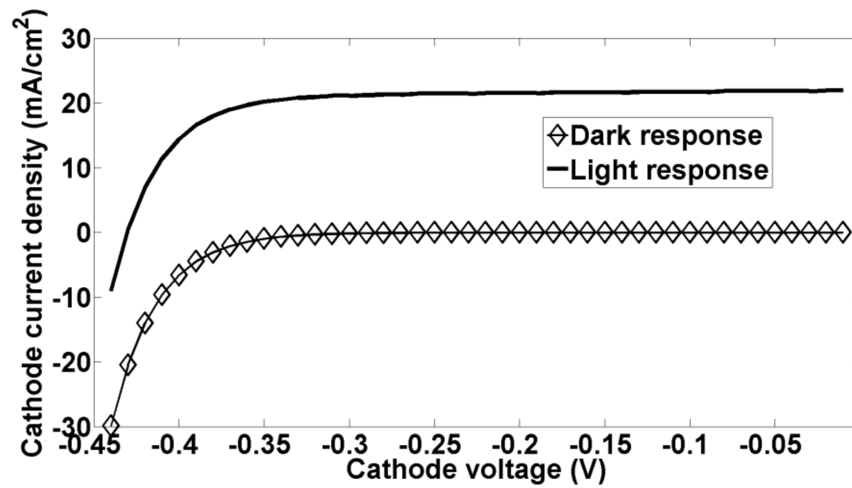


(b)

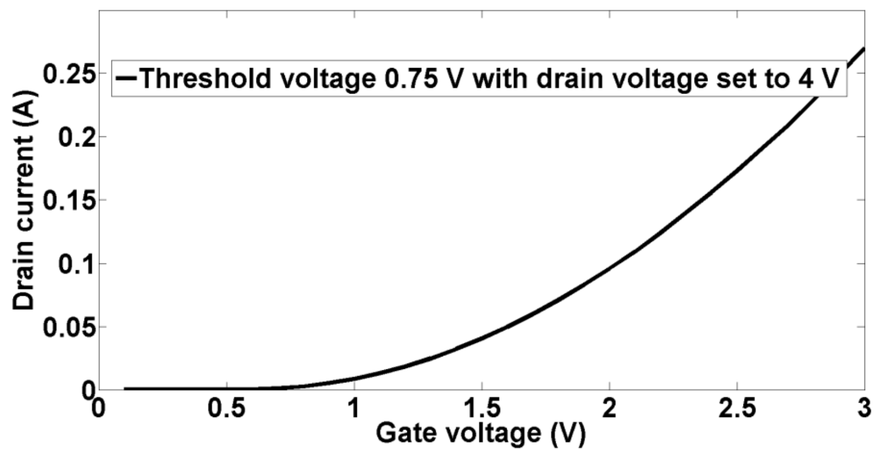


(c)

Fig. 2.2: Tentative MOS switch structures for the proposed integration (a) NMOS on *p*-substrate, (b) PMOS on *p*-substrate, (c) PMOS on *n*-substrate.

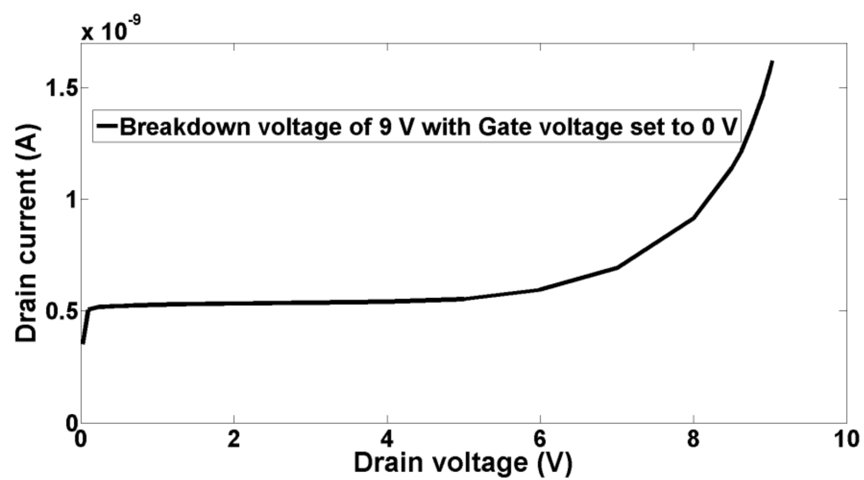


(a)

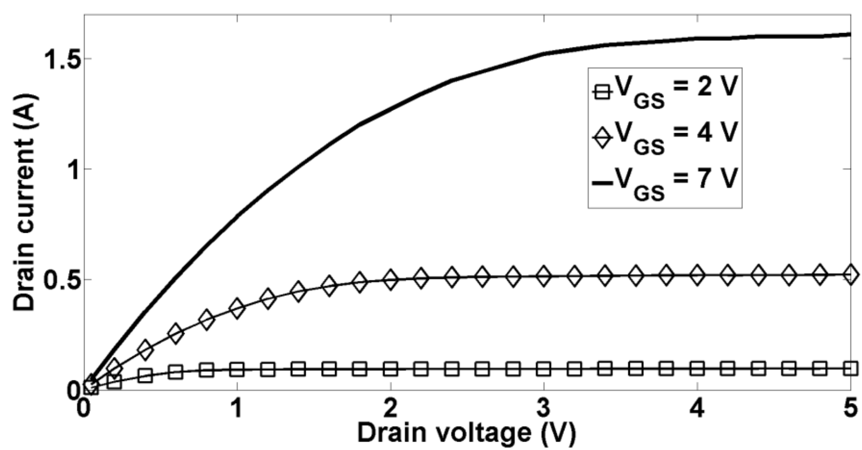


(b)

Fig. 2.3: Characteristics of the PV cell and MOSFET for the proposed processes (a) I-V characteristics of the PV cell, (b) threshold voltage characteristics, (c) breakdown voltage characteristics, (d) I-V characteristics of the MOSFET.



(c)



(d)

Fig. 2.3: Continued.

.

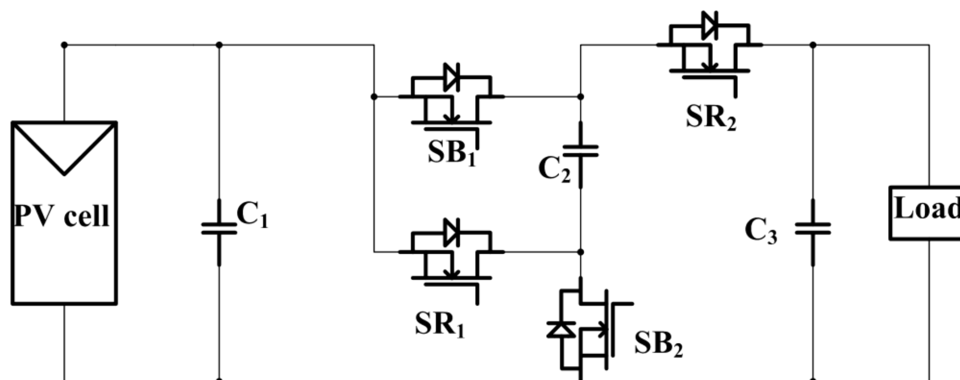


Fig. 2.4: Schematic diagram of a 2-level MMCCC used in Smart Spice.

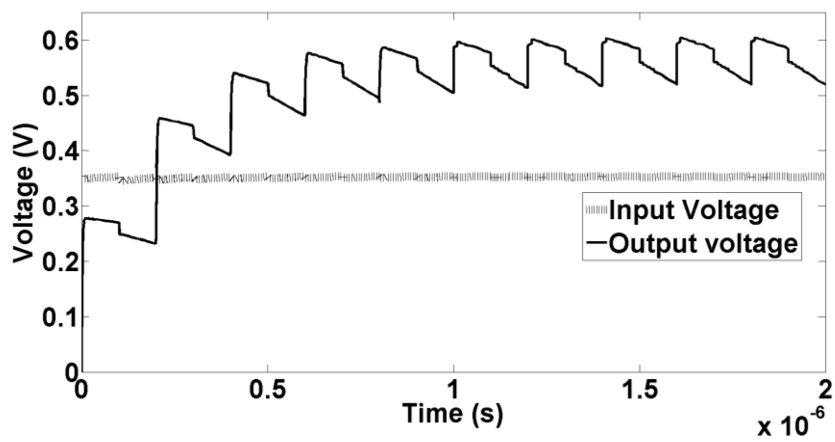


Fig. 2.5: Voltage boosting operation of the embedded MMCCC.

CHAPTER 3

FEATURES AND CHALLENGES IN MONOLITHICALLY EMBEDDED POWER CONVERTERS FOR PV POWER GENERATION

Lately, AC photovoltaic modules have been introduced with the power converter integrated at the back of the panel. [1]. In general, these circuits use several electrolytic capacitors and discrete semiconductor devices to realize the power conversion stages. Large electrolytic capacitors used for energy decoupling are known to be the weakest link in these power converter circuits [2]–[4]. When the ambient temperature is substantial, these electrolytic capacitors significantly suffer from shorter life cycle. The ever increasing energy demand and diminishing natural resources dilemma can be solved by renewable energy sources; extensive research is going on renewable energy sources and energy harvesting. The idea of macroelectronics can be imported in renewable energy sources also such as by integrating the power converter circuit on the same wafer used to build the solar energy harvesting devices. No previous work has been found so far in the literature on this application of macroelectronics. Several PV cells with an integrated low-power converter can significantly address several issues:

- The amount of wiring, soldering.
- Reduced losses.

- Reduced maintenance due to reduced overall system complexity.
- Integrated electronics can provide real time information about the degradation, damage, and potential catastrophic failure, most importantly partial shading phenomenon.
- Maximum power point tracking using fewer sensors.

Detail discussion on these features is also included in this chapter.

3.1 Recent High Reliable, High Efficiency Designs for PV Power Generation

Several commercial microinverters such as Enecsys, Enphase, Sparq and Solar-bridge Pantheon microinverter, etc., promise very high reliability (20–25 years). Large electrolytic capacitors are considered to be the primary cause of converter failure. The power decoupling technique is used to reduce this capacitor size. The Power decoupling techniques can be categorized into three types: PV side decoupling, DC link decoupling, and AC side decoupling. For the first case, the decoupling capacitor is used just after the PV module. For the second case, the decoupling capacitor is used after the boost DC-DC converter. For the last, the decoupling capacitor is placed on the AC stage.

Numerous techniques to reduce power decoupling capacitors can be found in the literature. Reference [5] shows one method to reduce capacitor size for the PV side coupling case. The authors used an active filter just after the PV cells to reduce the capacitance of the decoupling capacitor. However, the smaller decoupling capacitor can induce much stress on the power devices, which can reduce the reliability of the converter. A better solution is proposed in [6]. This topology combined boost and fly-

back converters to produce a very high DC voltage, allowing higher ripple in the DC voltage. Therefore, the decoupling capacitor size can be reduced.

The advantage of using decoupling capacitors after the DC-DC converter stage is that the higher the DC voltage the higher ripple can be tolerated, and this can reduce the size of the decoupling capacitor. The research trend in this direction is to use different control techniques; therefore, the output current distortion can be avoided. In [7], a modulation strategy is proposed to reject the ripple in DC voltage designing a suitable control system. In [8], a control strategy is proposed that can estimate the ripple in the DC voltage and subtract it from the actual voltage; therefore, the pure DC voltage can be fed back to the control circuitry.

One example of AC side decoupling can be found in [9], where additional phase leg is introduced to connect decoupling capacitor between inverter and the grid. This is a current source inverter (CSI) topology.

To achieve higher reliability of the converter, the recent trend is to use three port converters, one port for MPPT and boosting and one for the inverter and the third one is a power decoupling port [10]. A very recent design from University of Illinois Urbana Champaign (UIUC) supposedly having a life-time of 100 years is proposed in [3].

Transformer less PV inverter offers less weight and volume. However, H-bridge topology with a unipolar modulation technique without any transformer suffers from a large leakage current during zero state, reducing the efficiency of the converter. Sunways proposed a PV inverter to solve this issue providing a very high efficiency [11]. In this design, a bidirectional switch is realized that disconnects the PV from the grid during the zero voltage state. Therefore, leakage current through the parasitic capacitance of the PV

becomes negligible. The efficiency of this technique is around 95%. An alternative circuit is proposed in [12], where the zero voltage state circuit utilizes an insulated gate bipolar transistor (IGBT) and diode bridge circuit. The advantage of this topology compared to the previous one is that it can supply reactive power to the grid also. However, this topology offers slightly lower efficiency (94%) compared to the Sunways converter.

In [13], authors designed a very high efficiency (98%) inverter only. The DC-DC converter stage is not considered here. This topology also addresses the leakage current issue as described earlier. To address the zero voltage state, the authors proposed an H6 inverter with two extra switches and freewheeling diodes than an H-bridge inverter. During positive and negative cycles, the current flows through three transistors instead of two transistors for a full-bridge inverter. During zero voltage state, the extra transistors and diodes are activated to disconnect PV from the grid in order to obtain very high efficiency.

In [14], an active power decoupling technique has been proposed. This topology is 94% efficient, and without the power decoupling circuit the efficiency is 95%. According to the authors, this topology offers high efficiency as well as high reliability.

Another highly efficient converter topology can be found in [15]. Here, an H-bridge series-resonant inverter is used after the PV cell, followed by a high frequency transformer to provide isolation and voltage transformation. The high frequency quasi-sinusoidal AC current output from the transformer is passed through a novel half wave cycloconverter to down convert the high frequency current. Therefore, unity power factor at line frequency is achieved at the output. Proper control technique for modulating the cycloconverter ensures reduced power drop in the device and an eventual increase of

efficiency (around 96%).

3.2 Features of the Proposed Integration

The idea of the embedded power converter is in one 200 Wp module there will be around 20 low power (10 W) DC-DC converters. The surface electronics can go a long way to reduce the effect of partial shading. During partial shading, the shaded cells will produce less power; therefore, the converter connected with these cells will not contribute enough to the total output. With smart electronic circuits it is possible to disconnect those cells and converters from the rest of the module, which can significantly reduce the issues of hot spot formation, by-pass diode failure, arcing, etc., in summary increased reliability and life span of the module. This may lead to eliminating the by-pass diode.

3.2.1 Cost Reduction

The cost associated with PV power generation has decreased significantly over the last decade. For big plants with the highest insolation, the cost of PV power generation is about 20–25 cent per kWh, and this is still quite high compared to the power generation cost from coal and other sources (4–5 cents). The cost situation for residential PV power generation and feeding extra power to the grid is worse. As the inverter and installation costs are comparably high for small power production, the average cost for residential PV power generation is more than 35 cents per kWh. However, as the nano-/microgrid concepts are getting more interest, the state of art certainly is moving towards residential PV power generation and feeding extra power to the grid. However, the massive deployment of this idea can be realistic only if the cost can be reduced significantly. The

AC module idea is gaining more insight for this reason. The total cost associated with a typical c-Si PV power generating system is about \$5–\$7 per watt; the breakdown is shown in Table 3.1.

The cost associated with the inverter stage can be significantly reduced if the ages old central inverter scheme is used. However, significant wiring and installation cost are added to connect the very high DC voltage bus to the central inverter. These cost factors are significantly reduced in the AC module. In an AC module, wiring is easier because of the low module voltage. The AC module comes with this wiring from the manufacturer. With no electrical installation cost, only the mechanical installation cost for the AC module leads to reduction of the total installation cost significantly. Therefore, based on the previous analysis, the total PV power generation cost can be reduced to lower than \$5/W if the AC module is used as shown in Table 3.2. All of these cost advantages are also true if the PV converters are integrated with PV cells.

Moreover, there may be other cost advantage associated with embedded PV power converters. Analysis shows that component cost comprises around 60% of the total inverter cost; the rest of the 40% comes from the assembly, packaging, testing, printed circuit board (PCB), etc. Therefore, an embedded power converter can significantly reduce other costs like assembly, PCB. An estimate is shown in Table 3.3.

This cost reduction may not be significant at this moment; however, GaN, thin film, or even polysilicon integration can lead to a significant cost reduction in the future.

3.2.2 Partial Shedding

Now the amount of power harvesting can be compared for different cases. For the conventional central inverter scheme, several modules are connected in series. Shading from dirt, debris or even small shades from tree branches, antenna can reduce the energy harvesting significantly because this limits the energy produced from other modules also. The AC module addresses the partial shading phenomenon in the module level. Therefore, the shading problem of one module does not affect the others, increasing the amount of energy harvested. Present best estimates show that, the AC module can increase the energy yield up to 12% compared to that of a central inverter scheme.

Now, an argument can be made for an embedded PV power converter. Although the AC module can handle partial shading in the module level, on a single module a lot of cells are series connected; shading on one of these cells reduces the energy harvesting of all the series connected cells. If several small power converters are used instead of one power converter for a module, the partial shading phenomenon can be addressed more conveniently; which will harvest more power than an AC module does. However, several (may be 5–10 converters for a 200 Wp module) converters will only be economic if those are fabricated with the PV cells in the embedded fashion.

Another advantage of cell-level converters is the enhancement of module efficiency. In general, the module level efficiency is much smaller than the cell-level efficiency because of the mismatch of cells in a module. Presently, there is no available technique that can address this inherited fabrication phenomenon. However, cell-level converters can address this issue in the same way the AC module addresses the module level mismatch incurred in the central inverter configuration. Using an embedded converter,

cell mismatch phenomenon can be addressed by increasing the module efficiency close to the cell efficiency.

3.2.3 Enhanced Reliability

The most understandable way of expressing reliability is the failure rate, expressed in terms of failures per unit of time (F/hr). Another commonly used term is the mean time between failure (MTBF), which is the inverse of the failure rate being expressed in hours or years. The most commonly used expression for the equipment failure rate is

$$\lambda_{EQUIP} = \sum_{i=1}^{i=n} N_i (\lambda_g \pi_Q)_i \tag{3.1}$$

λ_{EQUIP} = Total equipment failure rate (Failures/10^6 hours)

λ_g = Generic failure rate for the ith generic part (Failures/10 10^6 hours)

π_Q = Quality factor for the ith generic part

N_i = Quantity of the ith generic part

n = Number of different generic part categories in the equipment

Taking the inverse λ_{EQUIP}, MTBF of the particular equipment can be calculated [16]. From the above equation it is clear that a particular component can be very reliable; however, a higher components count of a reliable part can reduce the reliability significantly. With discrete components the situation becomes worse because of the interconnections and wiring.

When the operating temperature of a particular part is changed, the failure rate is

changed significantly. This can be calculated using the Arrhenius relationship:

$$\text{Acceleration factor, } AF = \frac{e^{\frac{a}{kt_1}}}{e^{\frac{a}{kt_2}}} \tag{3.2}$$

a = Activation energy in electron volts

k = Boltzmann's constant

t_1 = Initial temperature in Kelvin

t_2 = New temperature in Kelvin.

In moderate/high power converter, a very high current flows through the MOSFET. Due to ON resistance of the MOSFET, high current causes significant power dissipation in the switch, and this in turn increases the operating temperature of the MOSFET. This heating leads to reduced MTBF for switches in power converter; and this can be explained with the Arrhenius relationship described before. For the proposed low-power converters, low-operating current will lead to less heating. However, the high ambient temperature of the PV cells will still be a concern, as it will force the devices to operate at an elevated temperature, reducing MTBF. The panel integrated microinverter will also be exposed to this elevated temperature. For the microinverter, the heating will be focused to several switches. The proposed scheme of several low power converters may have an edge in this scenario also—the heating will be distributed among tens or more number of switches. Therefore, the extreme ambient heating effect can be mitigated.

Based on references [16]–[18], Table 3.4 is created to show the failure rate of

different components used in a typical power converter. The quality factor is assigned based on the heating of the different components.

Based on this data, (3.1) was used to plot failure rate versus the number of components for different components (Fig. 3.1). A few interesting deductions can be made from this plot. Low-power CMOS transistors are the most reliable component. Inductors and transformers are also very reliable, along with film capacitors. Low-power diodes also show very good MTBF. Power devices like diodes and Si FETs MTBF are worse than that of the electrolytic capacitors. FETs and diodes' MTBFs are much higher than that of the electrolytic capacitors at the same temperature. However, high power dissipation in power devices in a power converter increases the operating temperature of the FETs or diodes. This higher operating temperature is reflected through the high quality factor of those devices in Table 3.4 and the higher failure rate in Fig. 3.1. The proof of this concept can be found in reference [19].

Now, the data from Table 3.4 can be used to compare the reliability of the small converters if they are constructed from discrete components with that of embedded small power converters. It is assumed that there will be 20 10W power converters in a 200 W panel. During this calculation, the control circuitry's MTBF has not been considered, as those will be same for both of the cases. The MTBF calculated here does not give the actual estimation; due to the failure of control circuits, actual MTBF will be much lower.

If we consider a full bridge inverter after a boost MMCCC converter [20]–[22] in the embedded system, then every converter will have a total of eight MOSFETs and three capacitors. To reduce the ON resistance, it is assumed that every MOSFET actually consists of 15 small MOSFETs connected in parallel, enhancing the current rating. The

MTBF calculation is shown in Table 3.5.

Now for a discrete components converter, a typical boost converter followed by a full bridge inverter is considered. Therefore, the total number of MOSFETs and capacitors for each converter will be five (5) and two (2), respectively. Due to the lower power rating of the converters, the film capacitor can be used as an energy decoupling capacitor instead of an electrolytic capacitor. The MTBF calculation for this case is given in Table 3.6. It is clear from Tables 3.5 and 3.6 that the embedded power converter has clear advantages over the discrete components counterparts.

3.3 Challenges of the Proposed Integration

There may be a lot of technological challenges in this integration. The biggest issue is the cost. The process proposed here is based on Si. The current research trend in PV is to avoid Si, to avoid the high material cost. The major cost factor of PV power generation comes from the fabrication of Si wafers from Silica (around 50–60%). Two types of crystalline silicon are used in the industry. The first is monocrystalline, produced by slicing wafers (up to 200 mm in diameter and 200 μm thick) from a high-purity single crystal boule—giving high purity Si for fabrication of transistors, which is the most costly material. The second one is the multicrystalline silicon, made by sawing a cast block of silicon first into bars and then into wafers. The main trend in silicon PV cell manufacturing involves a move toward multicrystalline technology, which reduces the total cost by a few factors.

The fabrication process also uses some costly steps, which the PV cell manufacturer is trying to avoid. For example, doping (ion-implantation or diffusion) is costly as well as

a hard-to-control process. Presently, commercial PV manufacturers do not use any lithography. However, integrating electronics is not possible without lithography, as precision is a key for microelectronics. The screen printing technology can be applied here. However, screen printing introduces a good amount of series resistance, which will definitely degrade the performance of the circuits. Fabrication cost can be reduced by accepting this slight degradation of performance. A significant amount of research is needed to achieve optimization in this regard.

CMOS compatible fabrication processes do not offer significant capacitance; however, sufficient capacitance is necessary even for low power converters. Very high switching frequency can compensate low capacitance; however, the switching loss of the transistors will be high. Optimization will be required for this case also.

Since Si is a semiconductor, the light-generated carriers can travel to the surrounding electronics or capacitors, also reducing the efficiency of the systems, as those carriers will not be collected. No effect of this phenomenon has been observed in simulation; experimental observation is necessary to make any comment at this moment.

The ambient high temperature of the solar cells can be detrimental to the integrated circuits. However, the low power converters will cause low current to flow through the transistors; therefore, heat generated by the electronics themselves will be lower compared to that of conventional AC modules inverters. Reference [23] shows the temperature of the module around the year using data recorded in various places of the USA. According to the results presented in that article, the PV module temperature is less than 60 ^{o}C for 95% of the operating hours and less than 70 ^{o}C for 99% of the operating hours. Most of the commercially available transistors are designed to perform in the

temperature range higher than this temperature range. As long as the devices' own generated heat is not an issue in the integrated circuits unlike conventional solutions, the high ambient temperature from the PV cells should not be a significant failure issue for integrated circuits.

In the conventional module integrated inverters, the transistors generate heat because of high power converters, which adds to the PV module ambient temperature giving a raise to the temperature to a value higher than 80 ^{o}C. This extreme heating is primarily responsible for the reduced life span of the converters. The electrolytic capacitors are mostly prone to higher temperature situations than electronics, and this is due to the materials and the construction of the electrolytic capacitor. As Si capacitors will be used in the integrated circuits, the reliability of these capacitors should be equal to the reliability of the capacitors used in the highly reliable microprocessors. Therefore, the reliability issue related to high ambient temperature is supposed to be less critical in the embedded converter because of the inclusion of Si capacitors and low-power converters.

3.4 References

[1] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[2] T. Key, "Finding a bright spot, utility experience, challenges and opportunities in photovoltaic power," *IEEE Power Eng. Rev.*, vol. 22, no. 5, pp. 34–44, May 2009.

[3] P. T. Krein and R. S. Balog, "Cost effective hundred year life for single phase inverters and rectifiers in solar and LED lighting applications based on minimum capacitance requirements and a ripple power port," in *Proc. IEEE Applied Power Electronics Conf.*, 2009, pp. 620–625.

[4] F. Chan and H. Calleja, "Design strategy to optimize the reliability of grid-connected PV systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4465–4472, Nov. 2009.

[5] A.C. Kyritsis *et al*., "A novel parallel active filter for current pulsation smoothing on single stage grid connected AC PV modules," in *Proc. European Conf. Power Electronics Applications*, 2007, pp. 482–489.

[6] G. H. Tan *et al*., "Soft-switching fly-back inverter with enhanced power decoupling for photovoltaic applications," *IET Trans. Elect. Power Appl*., vol. 1, no. 2, pp. 264–274, Mar. 2007.

[7] P. Enjeti and W. Shireen, "A new technique to reject DC link voltage ripple for inverters operating on programmed PWM waveforms," *IEEE Trans. Power Electron*, vol. 7, no. 1, pp.171–180, Jan. 1992.

[8] N. A. Ninad and L. Lopes, "A low power single phase utility interactive inverter for residential PV generation with small DC link capacitor," in *Proc*. *IEEE Applied Power Electronics Conf.*, 2007, pp. 520–525

[9] B. W. Bush, "A single phase current source solar inverter with reduced size DC link," in *Proc. IEEE Energy Conversion Congress Exposition*, 2009, pp. 54–59.

[10] C. Zhao *et al*., "An isolated three port bidirectional DC-DC converter with decoupled power flow management," *IEEE Trans. Power Electron*., vol. 21, no. 9, pp. 2443– 2453, Sept. 2008.

[11] J. A. Carr and D. Hotz, "Assessing the impact of SiC MOSFETs on converter interfaces for distributed energy resources," in *Proc. IEEE Industrial Applications Conf*., 2007, pp. 336–341.

[12] T. Kerekes, "A new high efficiency single phase transformer less PV inverter topology," *IEEE Trans. Ind. Electron.,* vol. 58, no. 1, pp. 184–191, Jan. 2011.

[13] W. Yu *et al*., "High efficiency MOSFET inverter with H6-type configuration for photovoltaic non-isolated AC module applications," *IEEE Trans. Power Electron.*, vol. 26, pp. 1253–1259, Sept. 2008.

[14] T. Shimizu and S. Suzuki, "Control of a high efficiency PV inverter with power decoupling function," in *Proc. IEEE Int. Conf. Power Electronics*, 2011, pp. 1533–1539.

[15] A. Trubitsyn *et al*., " High efficiency inverter for photovoltaic applications," in *Proc. IEEE Energy conversion congress and Exposition*, 2010, pp. 2803–2810.

[16] *Military Handbook: Reliability Prediction of Electronic Equipment*, Dept. of Defense, Washington, DC, 1990.

[17] C. R. Sullivan, "Integrating magnetics for on-chip power: challenges and opportunities," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2009, pp. 291–298.

[18] F. Waldron *et al*., "Technology roadmapping for power supply in package (PSiP) and power supply on chip (PwrSoC)," *IEEE Tran. Power Electron*., Vol. 28, no. 9, pp. 4137–4145, Sept. 2013.

[19] F. Chan *et al*., "Grid connected PV systems: a reliability based comparison," IEEE Int. Symp. Industrial Electronics, pp. 1583–1588, 2006.

[20] F. H. Khan and L. M. Tolbert, "A multilevel modular capacitor clamped DC-DC converter," *IEEE Trans. Ind. Appl.,* vol. 43, no. 6, pp. 1628–1638, Nov. 2007.

[21] F. H. Khan and L. M. Tolbert, "Multiple load-Source integration in a multilevel modular capacitor clamped DC-DC converter featuring fault tolerant capability," *IEEE Trans. Power Electron.,* vol. 24, no. 1, pp. 14–24, Jan. 2009.

[22] F. H. Khan, and L. M. Tolbert, "Bi-directional Power Management and Fault Tolerant Feature in a 5 kW Multilevel DC-DC Converter with Modular Architecture," *IET Power Electron.*, vol. 2, no. 5, pp. 595–604, May. 2009.

[23] R. S. Balog *et al*., "A Photovoltaic module thermal model suing observed and meteorological data to support a long life, highly reliable module integrated inverter design by predicting expected operating temperature," in *Proc. IEEE Energy Conversion Congress Exposition*, 2009, pp. 3343–3349.

Table 3.1: Cost breakdown of a typical PV power generating system

Solar modules (c-Si)	$2–$4/W
Balance of system (mount, racks, wiring)	$0.75–$1.5/W
Inverter	$0.5–$1/W
Installation	$1–$3/W
Total	$5–$7/W

Table 3.2: Cost breakdown of a typical AC module

Solar modules (c-Si)	$2–$4/W
Balance of system (mount, racks, wiring)	$0.5–$1/W (wiring cost goes down)
Inverter	$0.75–$1.5/W (inverter cost goes up)
Installation	$0.75–$2/W
Total	$4.5–$6/W

Table 3.3: Cost breakdown of the proposed system

Solar modules (c-Si)	$2–$4/W
Balance of system (mount, racks, wiring)	$0.5–$0.75/W (wiring cost goes down)
Inverter	$0.5–$1.25/W (inverter cost goes up)
Installation	$0.75–$2/W (installation cost goes down)
Total	$4.5–$6/W

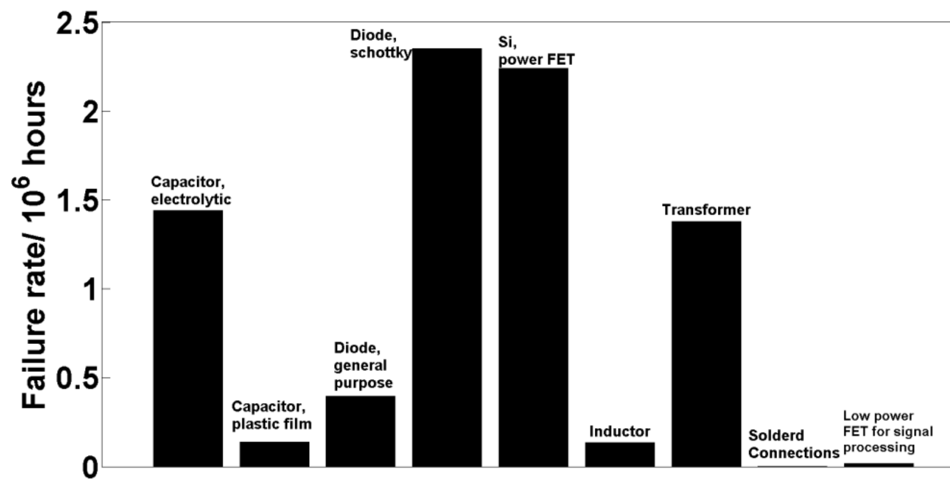


Fig. 3.1: Failure rate vs. different types of components

Table 3.4: Failure rate of different components used in power converters

Component	Failure rate/10^6 hours	Quality factor
Capacitor, electrolytic	0.024	3
Capacitor, plastic film	0.0023	3
Diode, general purpose	0.0036	5.5
Diode, Schottky	0.047	2.5
Si, power FET	0.014	8
Inductor	0.0017	4
Transformer	0.023	3
Soldered connections	0.00007	1
Normal low PR transistor for Signal processing	0.00015	5.5

Table 3.5: MTBF calculation of proposed embedded converter

Components	Failure rate/10^6 hours	Quality Factor	Quantity	Total Failure rate/10^6 hours
Low power MOSFET	0.00015	5.5	8x15x20	1.98
Capacitor, Si	.0023(assumed same as plastic film)	3	3x20	0.414
Total				2.394
MTBF				41 years

Table 3.6: MTBF calculation of the converter constructed from discrete components

Components	Failure rate/10^6 hours	Quality Factor	Quantity	Total Failure rate/10^6 hours
Si, FET	0.014	5.5 (Assumed same, because heating will be same as the embedded case)	5x20	7.7
Capacitor, plastic film	.0023	3	2x20	0.276
Diode, general purpose (can be used due to low power converter)	.0036	5.5	20	0.396
Inductor	.0017	4	20	0.136
Soldered connections	.00007	1	1000	.07
Total				8.578
MTBF				12 years

CHAPTER 4

CHARACTERIZATION OF MONOLITHICALLY EMBEDDED POWER CONVERTERS FOR PV POWER GENERATION

The proposed process to integrate PV cells with converter components resembles the fabrication process of an NMOS in the CMOS process. Therefore, commercial process vendors like MOSIS or X-FAB should be the best choice to implement the proposed AC solar cells. Interestingly, the process is based on creating isolated *p*-wells for PV and converter components. However, the available commercial foundry processes do not fabricate *p*-well structures, and they only provide *n*-well structures due to the material property of Si. In Si, electrons tend to go deeper and faster than holes. If a *p*-well is created before the *n*-doping, there is a possibility that the *n*-doped layer can move deeper than the *p*-well depth, resulting in a short circuit between the *n*-doped layer and the *n*-substrate. In this case the purpose of creating the *p*-well will be compromised. However, if *n*-well is created and then *p*-doping is done, there is no possibility of this doped layer going deeper than the *n*-well. In order to overcome this limitation, it is a common practice to use *n*-well and *p*-substrate for the CMOS process. This is unlike the proposed device structure for AC solar cell, where *p*-well and *n*-substrate has been chosen as described in Chapter 2.

Because the commercial foundry process is not available at this point, the most favorable option was to develop the process in the academic foundry. The University of Utah's Nanofab Lab was the best option in this regard. To make sure the *n* doped layer will not go deeper than the *p*-well, a long drive-in cycle was performed after the formation of the *p*-well.

4.1 Device Fabrication and Characterization

The process for an embedded power converter as described in Chapter 2 is implemented. The microphotographs of the device in different stage of the proposed process are shown in Fig. 4.1. Fig. 4.2 shows the final arrangement having the converter circuit components—NMOS switch, capacitor, diode, and resistor. In the completed prototype, the presence of the switches, diodes, resistors, etc., are indistinguishable because they are very small compared to the PV cells and the capacitors. Capacitors were designed to cover a large area so that adequate capacitance can be achieved for the converter circuit.

Careful inspection of the NMOS switch (Fig. 4.1c) reveals that several parallel fingers were required to increase the current rating. The logic NMOS switches are designed to handle a small amount of current in normal operating conditions. These switches are designed to be used in a converter circuit, and they should have a certain current-draining capability without becoming excessively warm. In this case, the device temperature will not significantly rise because the current will spread through multiple fingers. Depending on the rating of the low-power converter, the current rating can be calculated, hence the required number of fingers. Even though these switches can be

designed to carry decent currents, the process is still a low-voltage process (the breakdown voltage of the switches is smaller than 10 V). The number of fingers should be increased as much as possible to reduce the thermal stress, although this action will not significantly increase gate capacitance (high gate capacitance increases gate drivers' complexity) because of the use of this low voltage process.

Fig. 4.3 shows various device characteristics (experimental) fabricated in the proposed process. The fabricated diode showed no leakage current, and the forward voltage was approximately 0.7 V (Fig. 4.3a). The University of Utah's Nanofab lab is not a semiconductor quality foundry. Therefore, the furnaces used for oxidation, diffusion, drive-in, and annealing had a good amount of metal contamination.

Oxide contamination was a very big challenge during the early days of transistors, and this is why bipolar switches (BJT) were the first practical transistors because of their low sensitivity to oxide contamination. As the semiconductor foundry was able to grow good quality oxide, the MOS devices became prevalent.

In order to reduce the effect of oxide nonuniformity, thicker gate oxide (about 100 nm) was used in the fabrication. This is why the integrated NMOS had a very high threshold voltage, approximately 45 V (Fig. 4.3b). The breakdown/blocking voltage of the MOS switch was approximately 6 V, which can be seen in Fig. 4.3c (low voltage process). Finally, the I-V characteristics of the first MOS switch fabricated in the same process with a PV cell are shown in Fig. 4.3d, and the PV cell characteristics are shown in Fig. 4.4.

The fill factor (FF) of the fabricated cells was found to be approximately 60% while conducting the experiment. The PV cell characteristics at high light intensity showed less

FF due to the set up used for this measurement (Fig. 4.5). The cell was placed on top of an aluminum foil; therefore, the probe made contact with the bottom of the cell via the aluminum foil. The high current generated at this high illumination had to pass through the thin probes used for measuring the I/V characteristics. This combination increased the series resistance compared to the value found with less illumination. Therefore, this higher series resistance contributed to the low FF at high illumination, which will not be a significant factor in reality because thicker wires will be used for interconnections.

4.2 Embedded Power Converter

The next challenge was to construct a practical converter circuit using the devices described last section. In order to prove the same wafer/die concept, a very simple chopper circuit shown in Fig. 4.6 was implemented. Various devices used in this circuit were characterized using a Keithley 4200-SCS semiconductor characterization system. However, an appropriate circuit packaging is essential prior to building this converter. The choice of appropriate packaging was limited because the switches were on the same wafer as the PV cells, making the size of the entire device larger than available semiconductor packages. In addition, the back contact is an integral part of the solar cell, and the proposed integration needed a connection between the back contact and an available pin in the package.

As an initial solution, the entire wafer was attached to a center-drilled PCB using conductive adhesive. MEI wedge wire-bonding was used to create the connection between the bond pads of the switches and pads on the PCB for external connections. A positive gate pulse activates the NMOS, and the switch's V_{DS} drop was about 25 mV due

to the finite on resistance of the MOSFET. A low gate signal deactivated the MOSFET, and the open circuit voltage became irradiation dependent, which in this case was 260 mV (Fig. 4.7). The operation of this circuit indicates that the MOS switches properly function, even when they are exposed to illumination. This observation thus concludes that surface electronics may be viable to fabricate the entire converter on the same wafer/substrate having the PV cells.

4.3 Analysis of Light Generated Effects on the Power Switches (Simulation Results)

When the converter circuit is embedded with the PV cells in a panel, the PV cells as well as various circuit components will be exposed to light, and the p-n junctions or the channels associated with the power switches such as MOSFETs, IGBTs, and diodes are likely to be affected by this light exposure. In this chapter, basic device physics has been used to explain the light exposure effect on these monolithically embedded power switches. Only the key features of a switch such as threshold voltage, breakdown voltage, and output characteristics have been considered at this point. The source and the body terminal of the switching devices in a CMOS process are connected together in most structures, and the gate and drain voltages are applied with respect to the source/body. In this chapter, a similar biasing configuration has been used to analyze the effect of light on the switches used in the power converter.

The process described in section 4.2 has been implemented using Silvaco's ATHENA process software [1]. The fabricated devices were simulated both in dark and in light conditions using the ATLAS device simulator [2]. Fig. 4.8a shows the threshold voltage

characteristics of the switch in both of these conditions, and the threshold voltage remained the same even when the MOSFET was exposed to light.

The *p*-*n* junction created by the *p* body/well and the *n*-substrate will create an open circuit situation. Light generated electrons will be swept towards the *n* substrate, and holes will be swept towards the *p* well. As there will be no paths for these holes to be recombined with the extra generated electrons, the additional holes will effectively increase the conductivity of the body/well layer. This is also true for the created *p*-*n* junction between the drain and the body. Therefore, the conductivity of the drain region will also increase due to extra carriers generated by the incident light.

The threshold voltage of an NMOS switch can be expressed as

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_a (2\phi_F + V_{SB})}}{C_{ox}} \tag{4.1}$$

where V_T is the threshold voltage, V_{FB} flat band voltage, and

$$\phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i} \tag{4.2}$$

where N_a is the body doping concentration. From (4.1) and (4.2), it is apparent that for low/medium *p*-well doping (< $5\text{x}10^{17}$ cm^{-3}, which is usually true for MOS switches), the threshold voltage is a weak function (logarithmic or square root) of the body doping concentration. Therefore, the increase in the carrier concentration due to light exposure is not sufficient to change the threshold voltage to an observable quantity.

Fig. 4.8b shows the I-V characteristics of the switch both in light and in dark conditions, which are quite similar. The conductivity of the drain region increases due to light exposure (discussed above), and these extra light-generated carriers in the drain region increases the current flow by a few μA. This increment is a small fraction of the actual current and therefore cannot be observed in Fig. 4.8b.

Fig. 4.9a and Fig. 4.9b show the breakdown voltage characteristics of the switch in dark and in light, respectively. The blocking voltage of the NMOS switch depends on the depletion region width of the drain and the body, and the blocking voltage is higher for a wider depletion region.

The depletion region width of a *p-n* junction is given by

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)(V_{bi}-V)} \tag{4.3}$$

According to (4.3), higher doping concentration can reduce the depletion width as well as the blocking voltage. When the MOSFET is exposed to light, it generates extra carriers both in the drain as well as in the p body/well region (due to absence of external connection discussed above). Therefore, the increase in the carrier concentration contributed by the drain and body regions combined can reduce the depletion width and blocking voltage significantly.

The effect of light exposure on the breakdown voltage can be seen in Fig. 4.9, where this voltage is reduced to 8 V, which was originally 9 V without any light exposure. The *p-n* junction between the source and the body seems to have no effect on the above characteristics, provided the same biasing condition is met.

4.4 Analysis of Light Generated Effects on the Power Switches (Experimental Results)

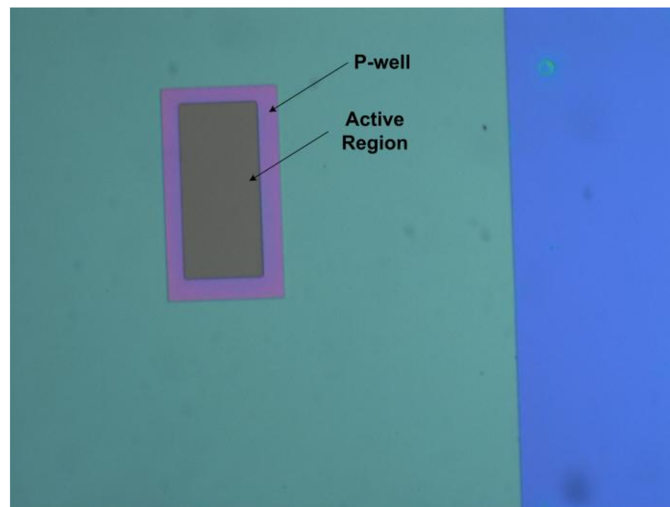
The experimental set up to understand the impact of light exposure to power switches is shown in Fig. 4.10. The experimental characteristics of the NMOS switch under light and in dark conditions are shown in Fig. 4.11. Although, the simulation and experimental results may look similar, there exists a discrepancy between them in terms of numerical values. This may occur because the optimized parameters such as temperature of the furnaces, fabrication time, etch duration, layer thickness, etc., in different steps of the process have not been obtained yet. While illuminated, the threshold voltage remains the same as it was in the dark conditions (Fig. 4.11a). The I-V characteristics at two different gate voltages are shown in Fig. 4.11b and Fig. 4.11c. The amplitude of the current slightly increases due to light generated extra carriers (which effectively increases the doping concentration as mentioned previously). This phenomenon was indistinguishable in Fig. 4.8b because the current amplitude is relatively high compared to that of Fig. 4.11b.

Higher gate bias voltage increases the current amplitude, and light generated amplitude enhancement is difficult to observe in experimental results as well (Fig. 4.11c). This analysis was performed to support the fact that power converters could be efficiently operated even when they are monolithically embedded on the same wafer along with the PV cells and are exposed to sunlight.

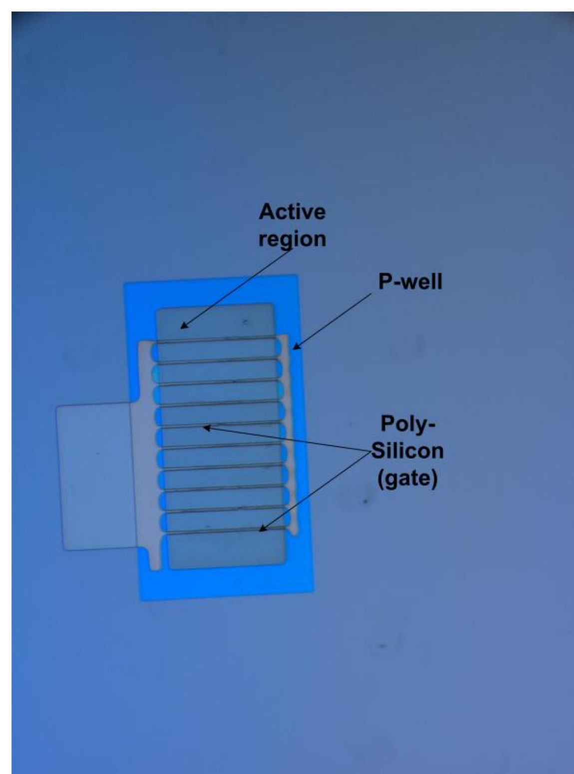
4.5 References

[1] Silvaco. (2014). [Online]. Avaialable: http://www.silvaco.com/products/tcad/process_simulation/athena.html.

[2] Silvaco. (2014). [Online]. Avaialable: http://www.silvaco.com/products/tcad/device_simulation/athena.html.

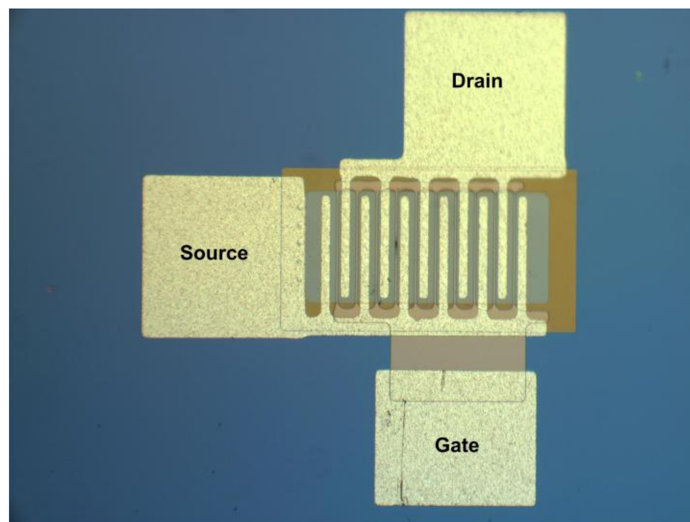


(a)



(b)

Fig. 4.1: Microscopic snapshot of the NMOS switch in different steps of the process (a) after first and second lithography and with gate oxidation, (b) after third lithography and with phosphorus diffusion, (c) final NMOS.



(c)

Fig. 4.1: Continued.

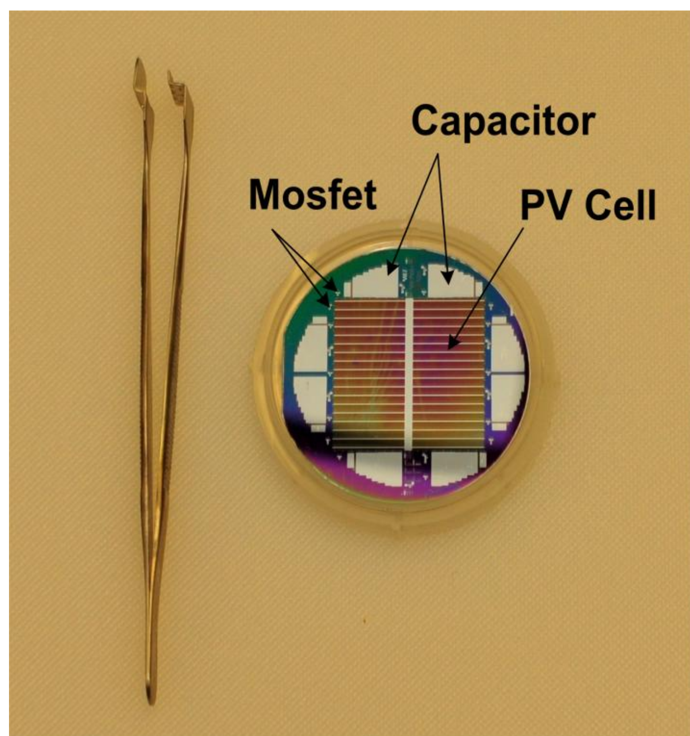
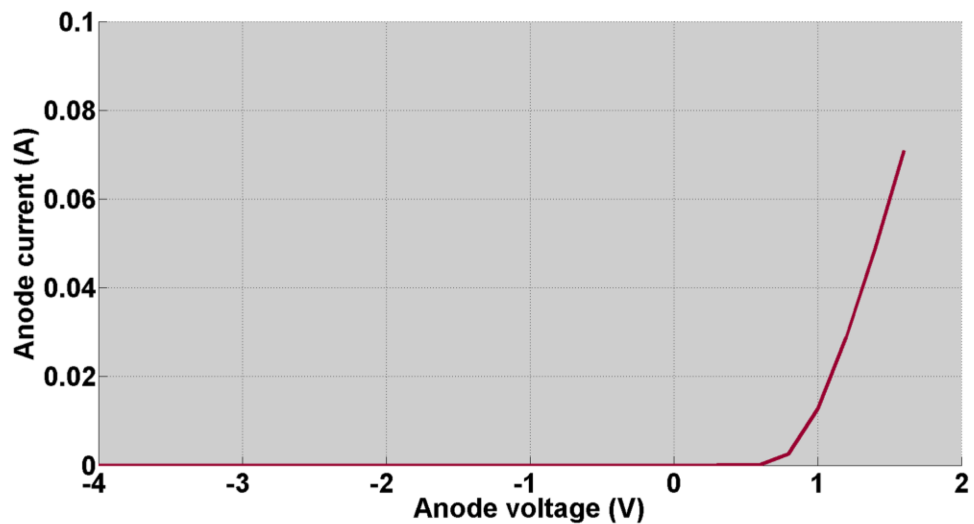
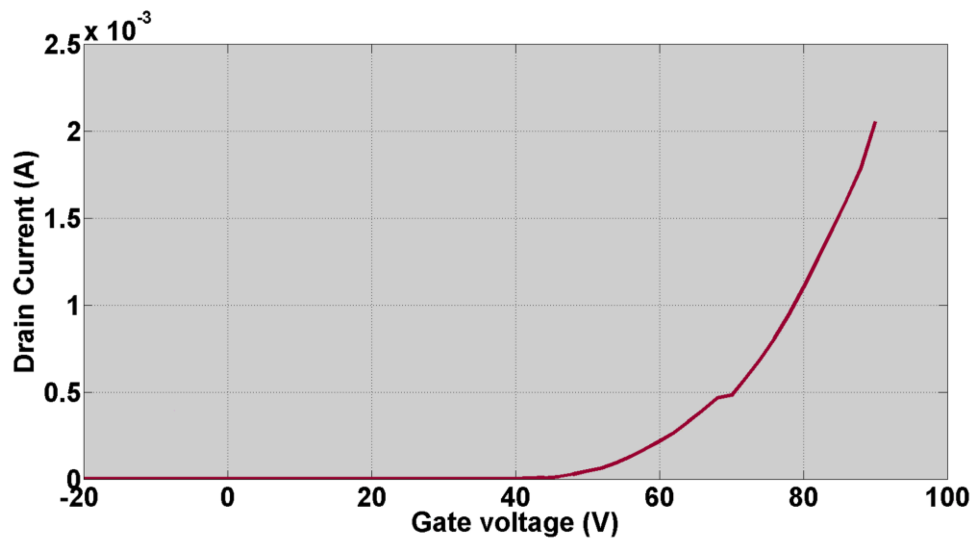


Fig. 4.2: Photograph of final prototype where a PV cell is fabricated in the same process with MOS switches and capacitors.

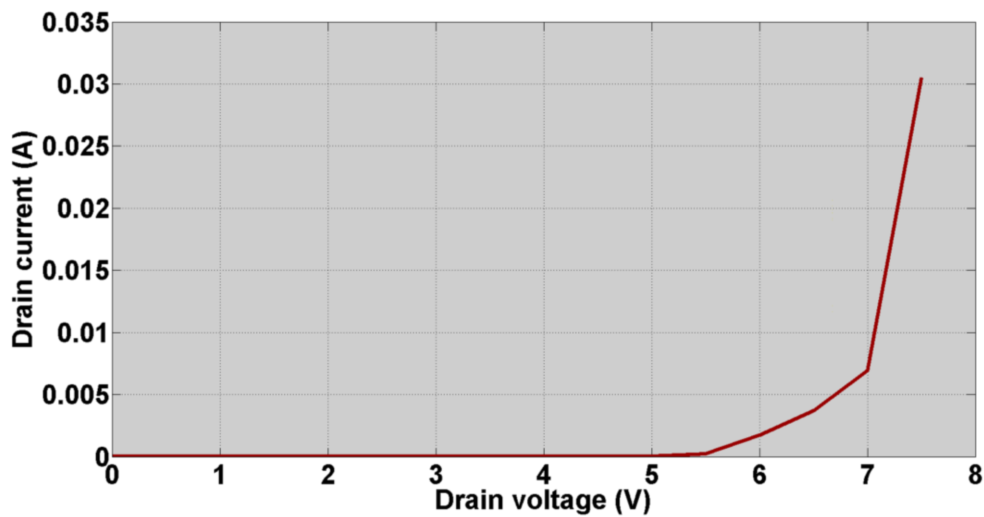


(a)

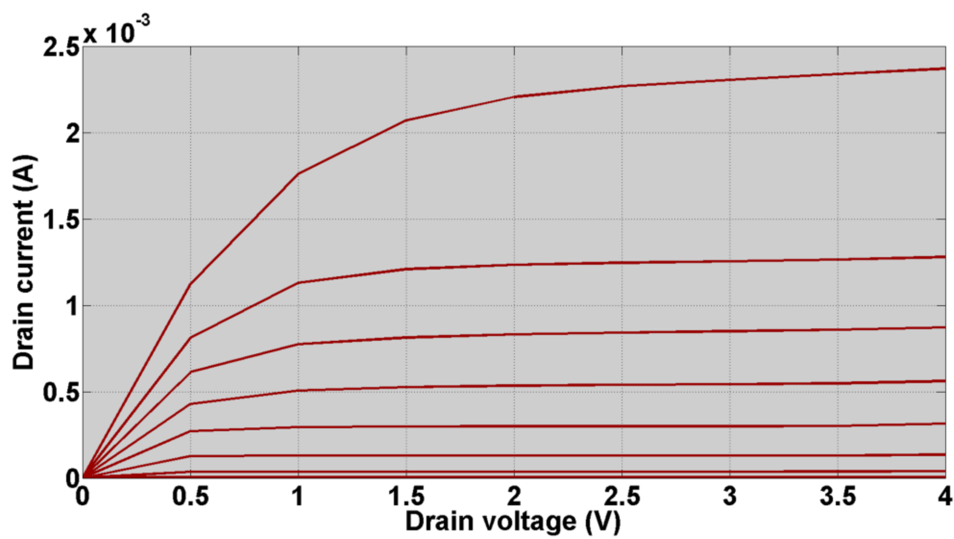


(b)

Fig. 4.3: Experimental characteristics of diode and NMOS switch fabricated on the same die/substrate of a PV cell (a) I-V characteristics of the diode, (b) threshold voltage characteristics of the NMOS, (c) breakdown voltage characteristics of the NMOS, (d) I-V characteristics of the NMOS.



(c)



(d)

Fig. 4.3: Continued.

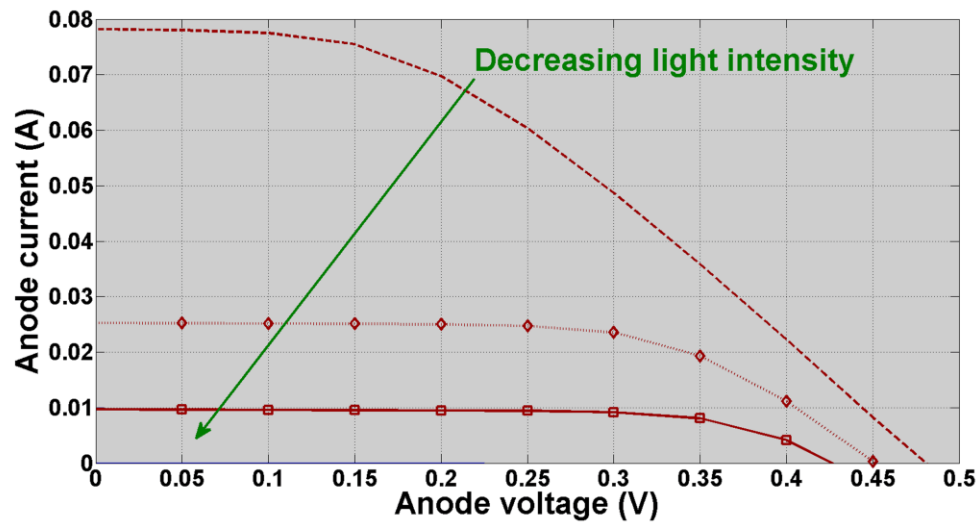


Fig. 4.4: Experimental I-V characteristics of the PV cell.

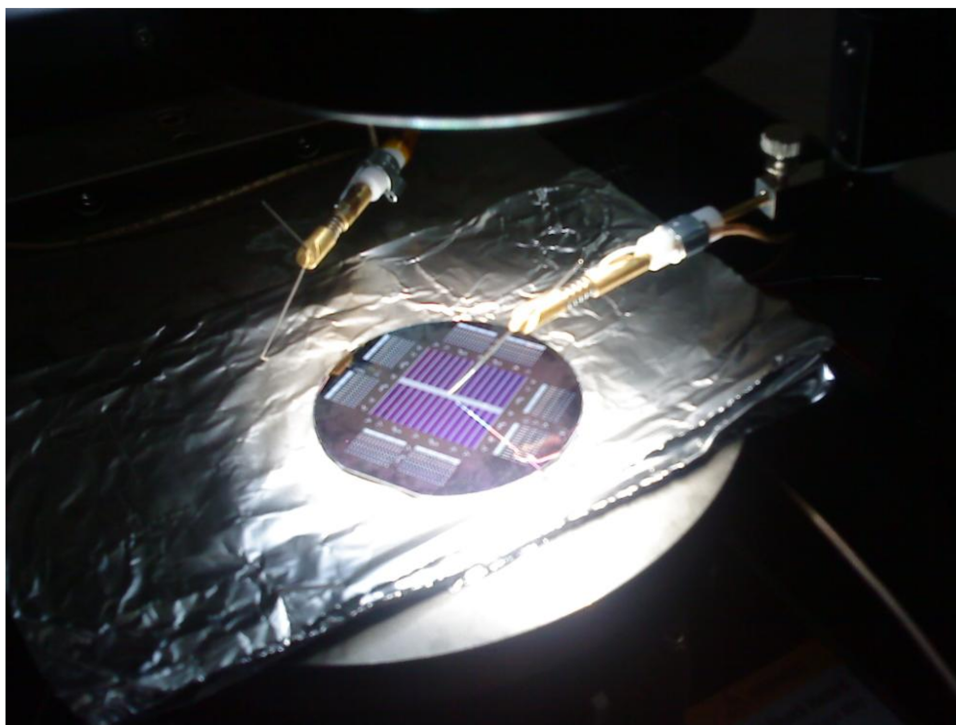


Fig. 4.5: Testing of the fabricated PV cells using Keithley 4200 SCS.

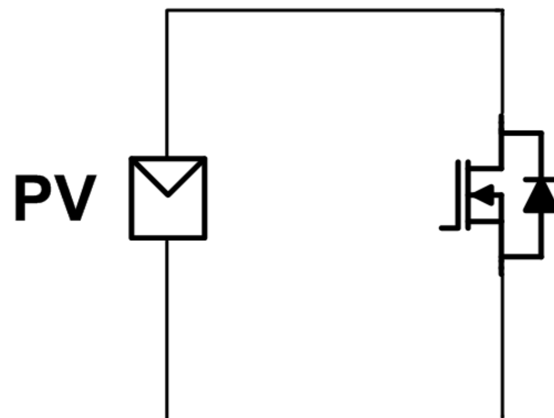


Fig. 4.6: Schematic of the implemented circuit.

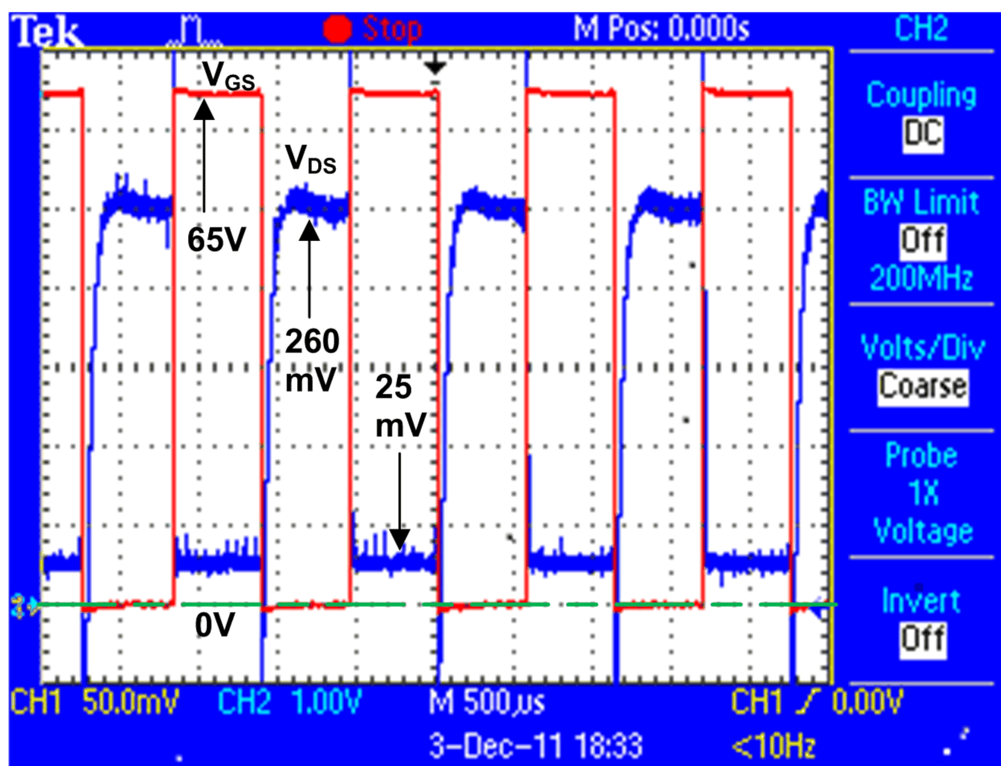
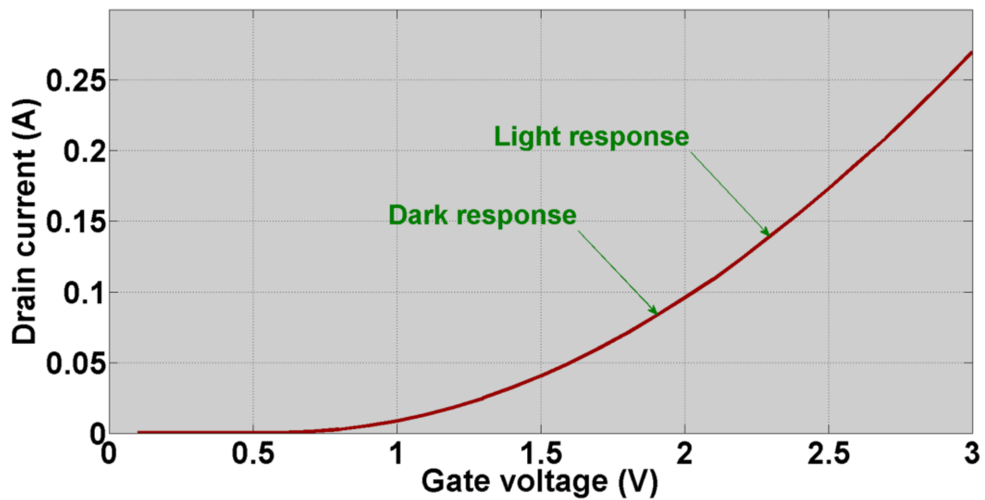
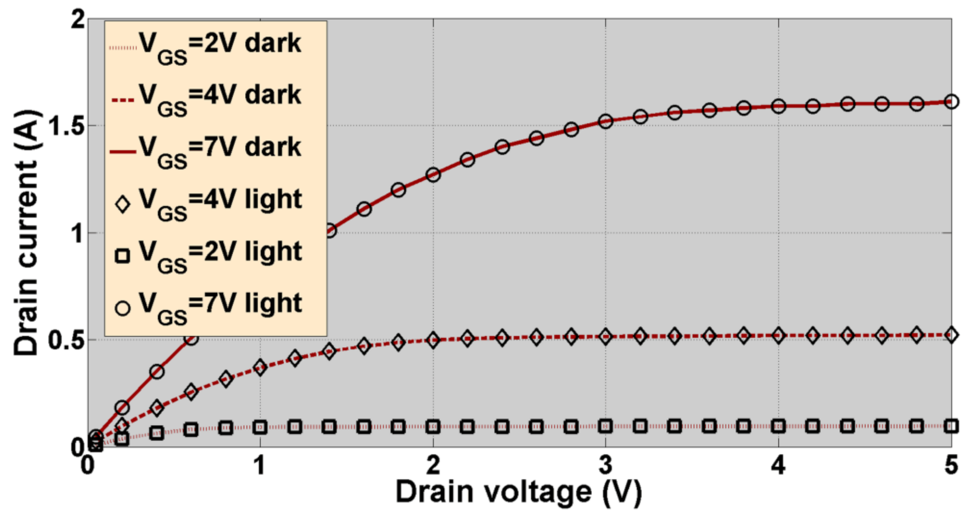


Fig. 4.7: Transient characteristics of the NMOS device and the PV cell located on the same substrate (V_{GS} and V_{DS} are not on the same scale).

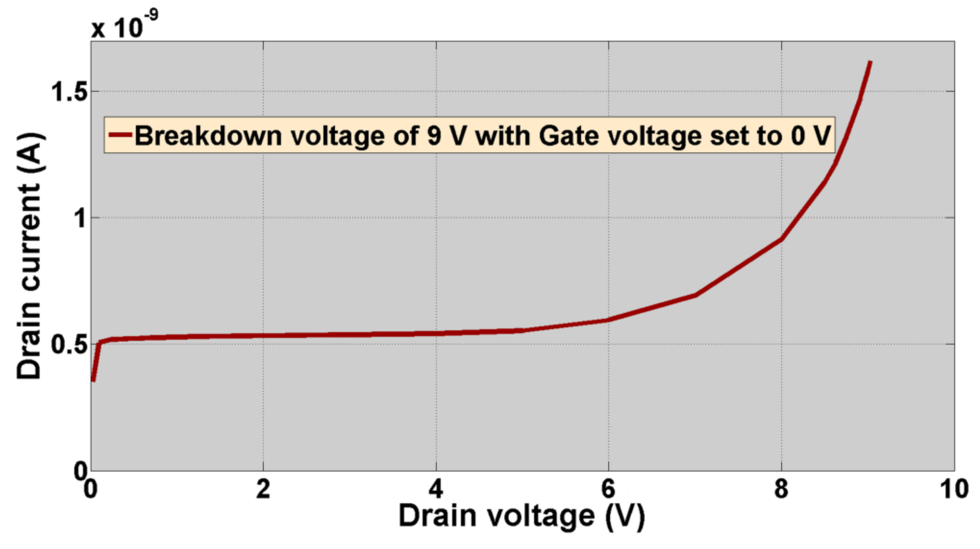


(a)

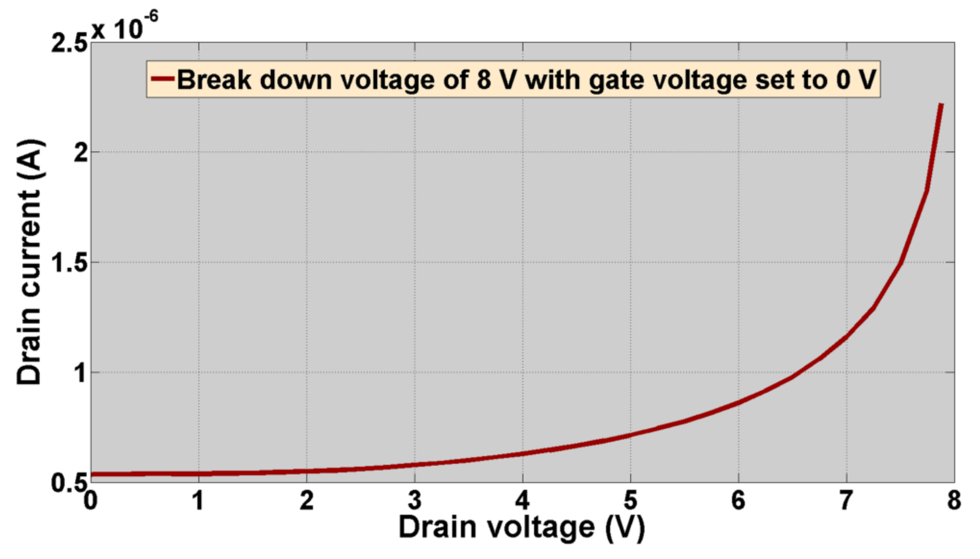


(b)

Fig. 4.8: Simulation results (a) threshold voltage characteristics in dark and in light, (b) I-V characteristics in dark and in light.

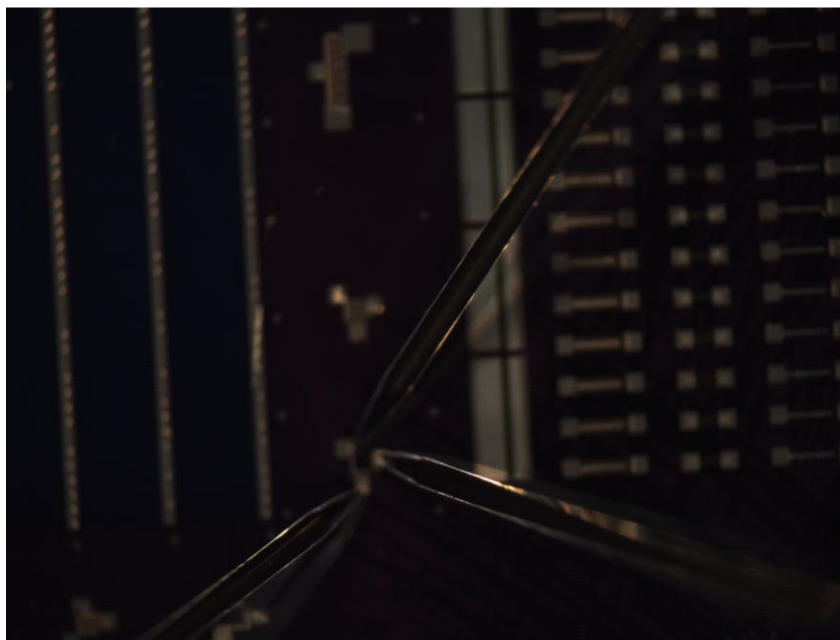


(a)



(b)

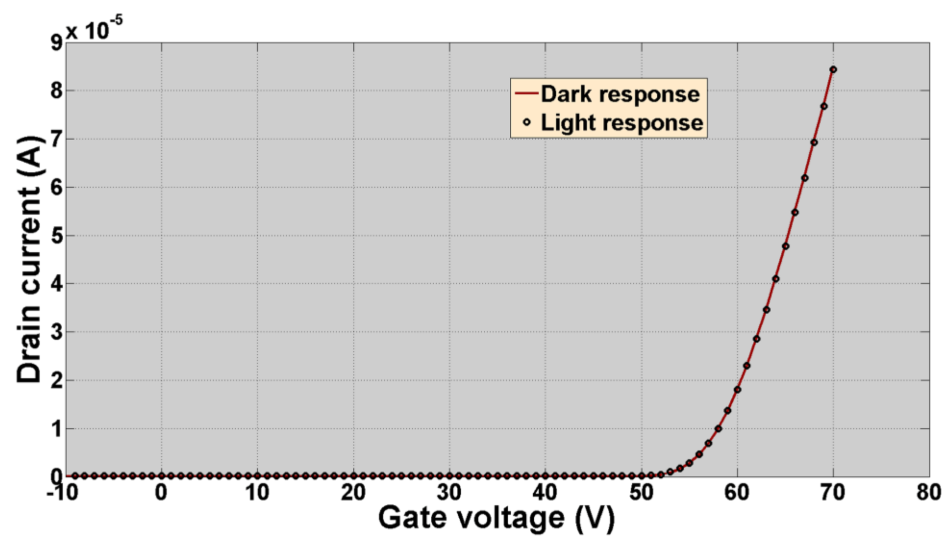
Fig. 4.9: Simulation results (a) breakdown voltage characteristics in dark, (b) breakdown voltage characteristics in light.



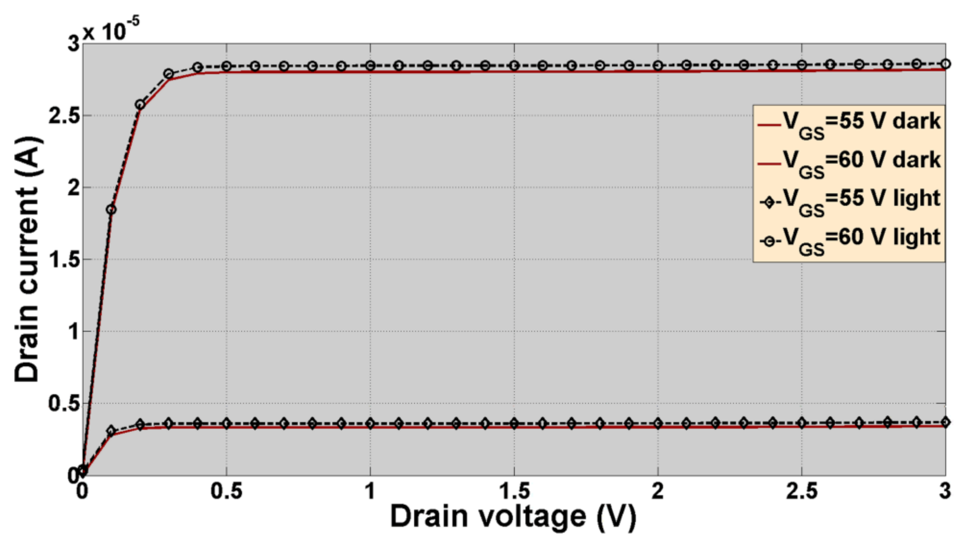
(a)

(b)

Fig. 4.10: Testing of switches using Keithley 4200 SCS (a) in dark, (b) in light.

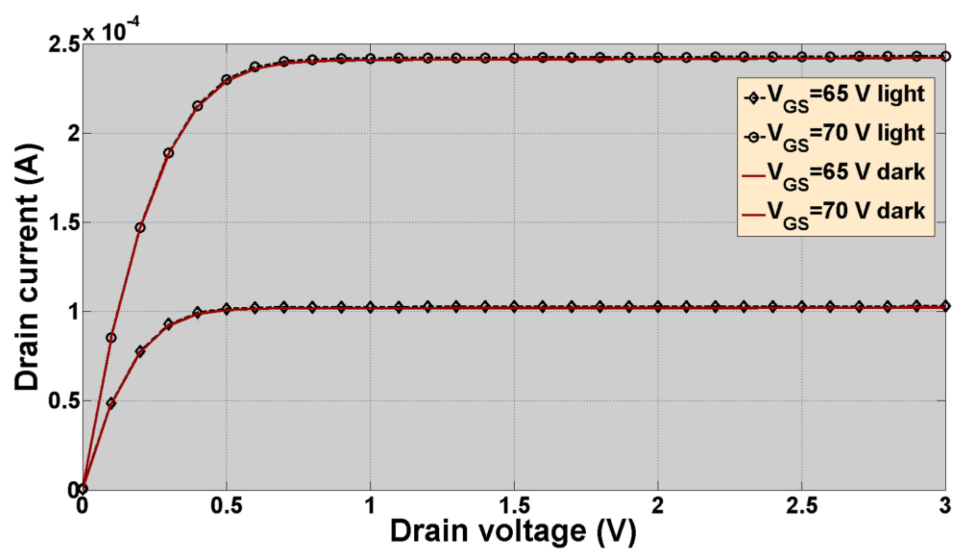


(a)



(b)

Fig. 4.11: Experimental results (a) threshold voltage characteristics in dark and in light, (b) I-V characteristics in dark and in light (V_{GS} = 55 V and 60 V), (c) I-V characteristics in dark and in light (V_{GS} = 65 V and 70 V).



(c)

Fig. 4.11: Continued

CHAPTER 5

PIEZOELECTRIC MEMS RESONATOR IN POWER CONVERSION

A piezoelectric resonator (such as a film bulk acoustic resonator (FBAR) [1]–[3]) is an elastic body consisting of a piezoelectric material that can be excited to cause vibration when an alternating electric field with resonant frequency is applied to it. The mechanical vibration in the neighborhood of the resonant frequency depends on the inertia, elastic compliance, and stiffness of the resonant element, and those correspond to inductance, capacitance, and resistance, respectively, of an equivalent electrical circuit. The equivalent electrical model of a MEMS piezoelectric resonator is shown in Fig. 5.1, known as the Butterworth-Van Dyke (BVD) model [3]–[7]. This resonator can be used to replace the discrete L-C resonant tank used in resonant converters [4]. With no passive components the resonant converter can be easily integrated in a power conditioning circuit with microimplantable devices.

In measuring neural signals and/or stimulating nerves, chronically implanted microelectrodes play a major role. The Utah electrode array (UEA) is one such microelectrode [8], [9] illustrated in Fig. 5.2. Nerve signal recording and stimulation using these electrodes, as shown in Fig. 5.3, is associated with several issues:

- Transcutaneous wired connection has an inherent risk of infection;

- There is a high chance of failure of the interconnects and wires due to mechanical stress and exposure to the in vivo environment;
- Long wires between the electrodes and the electronic circuits may increase the error level in signals; and
- Patients discomfort due to these hanging wires.

The wired connections of the components consisting of neural interface systems can be avoided using a wireless architecture for acquisition and processing biomedical data. This system is traditionally powered wirelessly using a planar spiral power coil [10]. Patients implanted with a neural system with a coil for power transfer cannot go through functional magnetic resonance imaging (FMRI) due to obvious magnetic interference and heating of the coil in an MRI machine.

These implants can be powered by batteries. Because replacement of batteries could be problematic in these systems, generating electrical energy from ambient sources becomes imperative. As these implantable devices are reduced in size, the bulky batteries become less attractive as a primary power source. Hence, it is more suitable to power such implanted systems by harvesting energy from ambient sources, such as acoustic noise, thermoelectric, electrostatic, or piezoelectric devices using ambient light, motion, vibration, etc., [11]–[15]. Further, bio fuels cells that convert power from blood glucose have been reported in [16]. [17] presents a very good summary of the required power level of different implantable devices. Without a few exceptions most of these devices consume 1 mW or more, and only a few of them require more than 100 mW of power.

A power conditioning circuit is essential for most of these energy harvesting techniques. In order to make the UEA system FMRI friendly, the power conditioning

circuit free of inductors or coils is preferable. The issues associated with the fabrication process of MEMS resonators is less cumbersome compared to those of on-chip inductors. Therefore, a piezoelectric microresonator on Si becomes a good candidate for power conditioning circuits for implantable energy harvesting devices. Acoustic coupling rather than inductive coupling makes the resonator based circuits suitable to be used in conjunction with UEA.

5.1 Characteristics of MEMS Resonator

A typical diagram of the FBAR structure is shown in Fig. 5.4. The impedance and phase characteristics between two electrodes of the resonator are shown in Fig. 5.5. This figure indicates that the device behaves like a capacitor below the resonant frequency (Fr) (the phase angle is around -90); the impedance becomes the lowest at resonant frequency (Fr). FBAR behaves like an inductor between resonant frequency (Fr) and antiresonant frequency (Fa) (the phase angle is around 90). The impedance is the maximum at the antiresonant frequency (Fa), and the FBAR is capacitive again beyond the antiresonant frequency (the phase angle is around -90). This behavior can be modeled using an electrical circuit shown in Fig. 5.1. If the resistance Rs is omitted from the equivalent circuit, the impedance between two terminals of the FBAR can be expressed in the following way

$$Z(\omega) = \frac{j(\omega Ls - \frac{1}{\omega Cs})}{1 + \frac{Cp}{Cs} - \omega^2 CpLs} \tag{5.1}$$

From this expression the resonant frequency and antiresonant frequency can be obtained as

$$Fr = \frac{1}{2\pi\sqrt{LsCs}} \tag{5.2}$$

and

$$Fa = Fr\sqrt{1 + \frac{Cs}{Cp}} \tag{5.3}$$

respectively. If the frequency is between Fr and Fa, the equivalent impedance of FBAR is given as

$$Z(\omega) = Rse + j\omega Lse \tag{5.4}$$

which means that FBAR should behave like an inductor Lse (H) having the loss Rse (Ω).

Piezoelectric MEMS resonators vibrating in a contour mode or radial extensional mode are considered in this thesis. The resonant frequencies of FBAR devices are primarily determined by the thickness of the piezoelectric film deposited by planar processing compatible with CMOS technology, such as sputtering or chemical vapor deposition (CVD), according to (1.1) and (1.2) [34]. Therefore, only high frequency FBARs in the GHz range is presently available. Because of this issue, it is a challenging task to verify the operation of a power converter using FBAR. In order to achieve

resonant frequency in the range of several MHz, the thickness of the film should be in the range of tens of micrometers. This is quite difficult to achieve in CMOS processes due to long deposition time and higher stress imposed on the thick film. However, the size and shape of a device operating in contour mode or radial extensional mode sets the resonant frequency. This is unlike an FBAR device, where thickness determines the resonant frequency. Therefore, moderately low resonant frequencies (in the range of MHz) can be achieved for contour mode devices.

5.2 Basic Principles of Contour Mode Piezoelectric Resonator

Piezoelectricity, a physical phenomenon discovered by the Curie brothers, is a linear interaction between electrical and mechanical domains occurring within a single elastic body. The behavior of piezoelectric elements can be described using the two fundamental equations of piezoelectricity [19]–[20]:

$$S = s^E.T + d_t.E \tag{5.5}$$

and

$$D = d.T + \varepsilon^T.E \tag{5.6}$$

where S is the mechanical strain, T is the mechanical stress, E is the electric field, D is the electric displacement, d is the piezoelectric constant, s^E is the elastic compliance at constant electric field, and ε^T is the permittivity at constant stress. According to (5.5),

applying an electric field E on a piezoelectric material results in a mechanical strain S (actuator operation). Equation (5.7) suggests that with an applied mechanical stress T, an electric displacement D is induced on the electric plates of the piezoelectric material (transducer action). Typically, the electrode plates are along the direction of axis 3, as shown in Fig. 5.6; therefore, the electric field, E, and electric displacement, D, are also in the direction of axis 3 (the nonzero component of the electric field is E_3). The fundamental matrix of piezoelectric constants for a typical piezoelectric material is as follows

$$d_t = d_{transpose} = \begin{matrix} 0 & 0 & d_{13} \\ 0 & 0 & d_{23} \\ 0 & 0 & d_{33} \\ 0 & d_{42} & 0 \\ d_{51} & 0 & 0 \\ 0 & 0 & 0 \end{matrix} \tag{5.7}$$

A piezoelectric resonator can be designed to resonate in thickness mode or in contour mode, and the former mode (by means of the d_{33} piezoelectric constant) is exploited in an FBAR. For contour mode, the d_{13} piezoelectric constant is utilized, and strain S_1 can be achieved by applying an electric field across the thickness of the film by substitution of (5.7) into (5.5) according to

$$S_1 = d_{13} E_3 \tag{5.8}$$

More analysis of the contour mode behavior can be found in [21]–[24].

Ring-shaped (circular or square) contour-mode AlN microresonators on Si are shown in Fig. 5.7. An AlN elastic body is sandwiched between two electrodes. With an electric field applied across the thickness of the AlN film, the body of the resonator vibrates in a breathing mode across its width through the d_{31} piezoelectric coefficient. The detailed analysis of the frequency of a circular piezoelectric ring vibrating in a pure radial extensional mode shape is presented in [25] and simplified in [26]. According to [26], if the average radius of the ring R_{avg} is much larger than the width W of the ring itself, the resonant frequency is mainly determined by the width of the ring according to

$$f = \frac{1}{W}\sqrt{\frac{E_f}{\rho(1-\sigma^2)}} \tag{5.9}$$

E_f, ρ, and σ are the elastic modulus, density, and Poisson's ratio of the piezoelectric material, respectively [27]. The motional resistance R_S (Fig. 5.1) at the resonant frequency can be approximated by

$$Rs = \frac{\pi^2}{8}\frac{T}{2\pi R_{avg}}\frac{p^{\frac{1}{2}}}{E_f^{\frac{3}{2}} Q d_{31}^{\,2}} \tag{5.10}$$

where Q is the quality factor of the resonator. The frequency can be adjusted independently of the motional resistance, and the larger dimension (R_{avg} and W) of the

device reduces the frequency and resistance.

The proposed ring shaped (circular and square) resonators were simulated in COMSOL Multiphysics in order to evaluate their resonant frequency. An applied electric field across the thickness of the devices dilates it across its width due to the d_{31} coefficients at the resonant frequency which is 156.4 MHz for the circular device (Fig. 5.8a) and 156 MHz for the square device (Fig. 5.8b). Changing the dimension of the device changes the resonant frequency according to (5.9), and this is shown in Fig. 5.8c.

5.3 Piezoelectric Devices in Power Conversion

Interestingly, piezoelectric devices such as piezoelectric transformers (PT) have been used in power conversion applications for more than a decade [28]. They offer many advantages in terms of size and mass compared to their magnetic counterparts (inductors and transformers).

The detailed description of construction and operating principles of PTs is given in [29]. The equivalent electrical circuit model of the PT makes them very much suitable to use in series resonant converters. PT based series resonant converters can be used as lamp ballast as illustrated in [18]. Inductorless ZVS has been achieved through properly designed PT. This converter can also perform power factor correction without an inductor. The possibility of using piezoelectric transformers to realize an IGBT and MOSFET inverter-leg driver is described in [30]. The procedure to design the PT for gate driver application is detailed. The performance of the PT based gate driver is also included in that article.

A double and multilevel voltage converter based on PT is proposed in [31] and

illustrated in Fig. 5.9. They consist of multiple PT conversion circuits based on one input supply in series form and output the summation of their voltage levels. The performance of multilevel converters based on PTs is also described in that article.

A PT based PFC LED driver has been proposed and developed in [32]. Therefore, piezoelectric devices have been used as an energy conversion device in many applications. However, piezoelectric devices have not been used as a replacement of on-chip inductors to date. Therefore, a piezoelectric MEMS resonator can be integrated with the power conditioning circuit and with this embedded converter, an autonomous microsystem can be powered. This is the central idea of the dissertation.

A comparison of the state of the art devices used as energy conversion to a MEMS resonator (proposed device) is given in Table 5.1. The devices considered in this comparison are air core and thin magnetic film inductors described in Chapter 1, piezoelectric transformers, and the proposed device. Similar to the proposed device, the air core and thin magnetic film inductors can be integrated on Si as reported in the literature. Inductors that cannot be integrated on Si have not been considered here. Utilization of a thin film piezoelectric transformer on Si in power converters is described for the first time in Chapter 8. Articles listed in Chapter 1 and in this chapter were used in order to complete this comparison.

5.4 Merits of Utilization of MEMS Piezoelectric Devices in Power Converters

Electromagnetic interference (EMI) in switch mode power supply is a ubiquitous phenomenon. The MEMS piezoelectric devices being acoustic rather than inductive can reduce this EMI substantially. This makes the piezoelectric devices very attractive to be utilized in power converters.

Piezoceramic material based resonators are commercially available with resonant frequencies in the range of hundreds of kHz. A resonator from Murata electronics (CSBLA400KECE-B0) [33] has been used to validate the EMI advantage of the piezoelectric devices experimentally. This non-MEMS piezoceramic resonator has similar characteristics to the MEMES resonator described in section 5.1.

The EMI measurement of the prototype of Fig. 5.10a with low frequency resonator CSBLA400kECE-B0 (described previously) was performed and compared to that of a discrete L-C resonant inverter (the schematic of this circuit is given in Fig. 5.10b). The load resistance in the prototype was replaced by LEDs in both circuits. The schematic of the experimental set up for conducted EMI measurement is shown in Fig. 5.11; the supply lines passed through a LISN (line impedance stabilization network) to the converter and the output of the LISN was connected to a spectrum analyzer (Agilent E4404B ESA). The results from the spectrum analyzer are shown in Fig. 5.12. The noise generated by the function generator and auxiliary power supply were present in the results also. However, this is a comparison between two converters in terms of the conducted EMI performance; therefore, those noise are common in both results.

From Fig. 5.12 it is clear that the HF emissions in dB μV of both the converters are

below EN55022 (CISPR 22) the class A limit. However, the EMI performance of a piezoceramic resonator based converter is better than the discrete components converter (the noise level at switching frequency is much higher in discrete components circuit compared to that of ceramic resonator based converter). Therefore, a MEMS resonator based resonant converter has the potential to reduce EMI more than conventional resonant converters.

5.5 References

[1] R. Ruby, "A decade of FBAR success and what is needed for another successful decade," *Symp. Piezoelectricity, Acoustic Waves and Device Application (SPAWDA)*, 2011, pp. 365–369.

[2] P. Osbond *et al.*, "The influence of ZnO and electrode thickness on the performance of thin film bulk acoustic resonators," in *Proc. IEEE Ultrasonics Symp.*, 1999, pp. 911–914.

[3] J.D. Larson *et al.*, " Modified Butterworth-Van Dyke circuit for FBAR resonators and automated measurement system," in *Proc. IEEE Ultrasoincs Symp.*, 2000, pp. 863-868.

[4] A. M. Imtiaz and F. H. Khan, "Film bulk acoustic resonator (FBAR) based power converters: a new trend featuring EMI reduction and high power density," in *Proc. IEEE Applied Power Electronics Conf.*, 2013, pp. 1485–1492.

[5] A. M. Imtiaz *et al.*, "Contour mode piezoelectric ring micro-resonator on Si for series resonant converters" in *Proc. IEEE Applied Power Electronics Conf.*, 2014, pp. 1381–1389.

[6] A. M. Imtiaz and F. H. Khan, "Design and simulation of contour mode MEMS resonator on Si for power converters" *IEEE Control Modeling Power Electronics,* 2013, pp. 1–7.

[7] G. Piazza, "Piezoelectric aluminum nitride RF MEMS for radio frequency front end technology," Ph. D. dissertation, Dept. Electr. Comput. Eng., Univ. Calif., Berkeley, CA, 2005.

[8] A. Branner *et al.*, "Long term stimulation and recording with penetrating micro electrode array in cat sciatic nerve," *IEEE Tran. Biomed. Eng.* vol. 51, pp. 146-157, 2004.

[9] P. K. Campbell *et al*., "A silicon-based, three dimensional neural interface: manufacturing process for an intra cortical electrode array," *IEEE Trans. Biomed. Eng*., vol. 38, no. 8, pp. 758–768, Aug. 1991.

[10] S. Kim *et al*., "Influence of system integration and packaging on its inductive power link for an integrated wireless neural interface," *IEEE Trans. Biomed. Eng*., vol. 56, pp. 2927–2938, Dec. 2009.

[11] A. Chen, "Energy harvesting in the human body (implantable self powered sensors)," Ph. D. dissertation, Dept. Electr. Comput. Eng., Univ. Calif., Berkeley, CA, 2011.

[12] S. E. Jo *et al*., "Flexible thermoelectric generator for human body heat energy harvesting," *IEEE Electronics Lett.*, vol. 48, no. 16, Aug. 2012.

[13] M. A. Karami and D. J. Inman, "Powering pacemakers from heartbeat vibrations using linear and non-linear energy harvesters," *Appl. Phys. Lett*., vol. 100, no. 4, pp. 2901–2905, 2012.

[14] J. Lueke and W. A. Moussa, "MEMS based power generation technique for implantable biosensing applications," in *Proc. IEEE Sensors*, 2011, pp. 1433–1460.

[15] K. A. Cook-Chennault *et al*., "Powering MEMS portable devices – a review of non-regenerative and regenerative power supply systems with emphasis on piezoelectric energy harvesting systems," *Smart Materials Structures*, vol. 17, no.4, pp. 1068–1075, June 2008.

[16] F. V. Stetten *et al*., "A one-compartment, direct glucose fuel cell for powering long–term medical Implants," in Proc. *IEEE Micro Electro Mechanical Systems Conf*., pp.934–937, 2006.

[17] R. Bashirullah, "Wireless Implants," *IEEE Microwave*, vol. 11, no. 7, pp. S14–S23, Dec. 2010.

[18] R.-L. Lin, "Piezoelectric transformer characterization and application of electronic ballast," Ph.D. dissertation, Dept. Electr. Comput. Eng.,Virginia Tech, Blacksburg, Virginia, 2001.

[19] C. Y. Lin, "Design and analysis of piezoelectric transformer converters," Ph. D. dissertation, Dept. Electr. Comput. Eng.,Virginia Tech, Blacksburg, Virginia, 1997.

[20] S. W. Tehon, "Piezoelectric and magnetostrictive transducers," Ph. D. dissertation, Dept. Electr. Comput. Eng., Univ. Illinois, Urbana-Champign, Illinois, 1958.

[21] C. A. Rosen, "Analysis and design of ceramic transformer and filter elements,"

Ph.D. dissertation, Dept. Electr. Comput. Eng., Syracuse University, New York, NY, 1956.

[22] M. Onoe, “Contour vibrations of isotropic circular plates,” *J. Acoustical Society America*, vol. 28, no. 1, pp. 1158–1162, Jan. 1956.

[23] R. Holland, “Contour extensional resonant properties of rectangular piezoelectric plates,” *IEEE Trans. Sonics. Ultrason*., vol. 15, no. 2, pp. 97–105, 1968.

[24] M. Onoe, “Contour vibration of thin rectangular plates,” *J. Acoustical Society America*, vol. 30, no. 4, pp. 1159–1162, April 1958.

[25] G. Ambati *et al*., “In plane vibrations of annular rings,” *J. Sound Vibrations*, vol. 47, no. 1, pp. 415–432, Jan. 1976.

[26] B. Bircumshaw *et al*., “The radial bulk annular resonator: towards a 50 omega RF MEMS filter,” in *Proc. Transducers, Solid-State Sensors, Actuators Mircrosystems*, 2003, pp. 875–878.

[27] G. P. Philip *et al*., “Piezoelectric thin film AlN annular dual contour mode band-pass filter,” in *Proc. Int. Mechanical Engineering Congress Exposition*, 2005, pp. 517–523.

[28] E. L. Horsley *et al*., “State of the art piezoelectric transformer technology,” *European Conf. Power Electronics*, 2007, pp. 311–318.

[29] E. M. Baker, “Design of radial mode piezoelectric transformers for lamp ballast applications,” MS dissertation, Dept. Electr. Comput. Eng., Virginia Tech, Blacksburg, Virginia, 2002.

[30] D. Vasic, and F. Costa, “Piezoelectric transformer for integrated MOSFET and IGBT gate driver,” *IEEE Tran. Power Elecn*. vol. 21, no. 1, pp. 56–65, Jan. 2006.

[31] Y. Yuanmao, and K. Ding, “A novel method for connecting multiple piezoelectric transformers converters and its circuit applications,” *IEEE Tran. Power Elecn.*, vol. 27, no. 4, pp. 1926–1935, April 2012.

[32] M. S. Rodgaard *et al*., “Forward conduction mode controlled piezoelectric transformer based PFC LED driver,” *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4841–4849, Oct. 2013.

[33] Murata. (2014). *Ceramic Resonator* [Online]. Available: http://www.digikey.com.

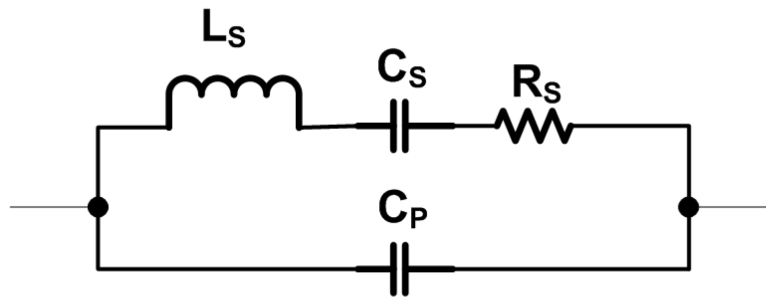


Fig. 5.1: Equivalent electrical circuit model of a piezoelectric resonator.

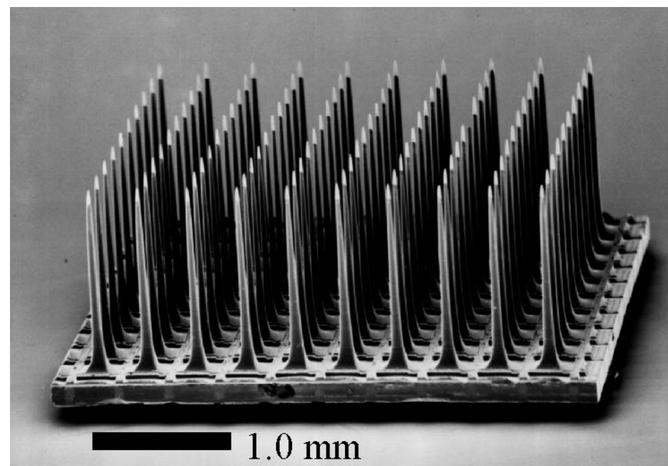


Fig. 5.2: Scanning electron microscope (SEM) image of the Utah electrode array (UEA) (courtesy of the Center for Neural Interfaces at the University of Utah)

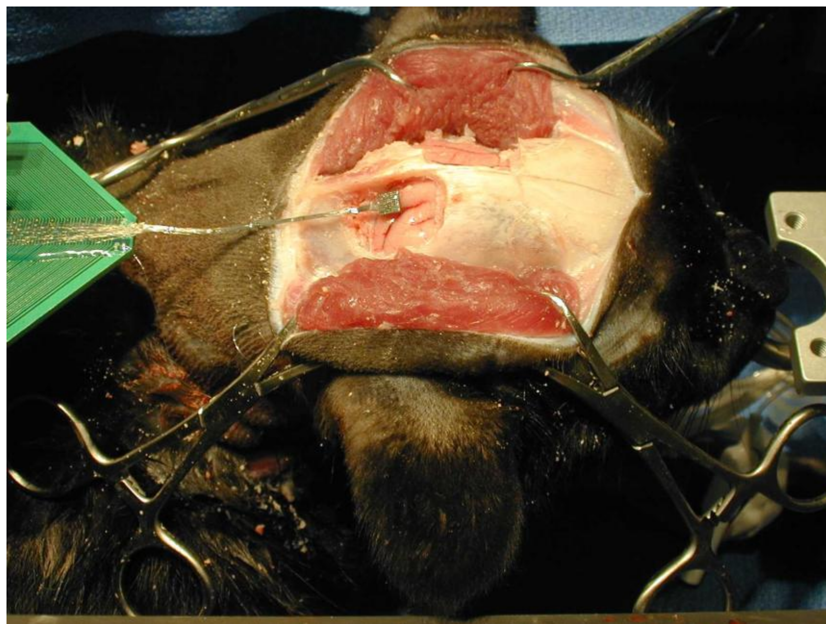


Fig. 5.3: Nerve signal recording and stimulation using UEA (courtesy of the Center for Neural Interfaces at the University of Utah)

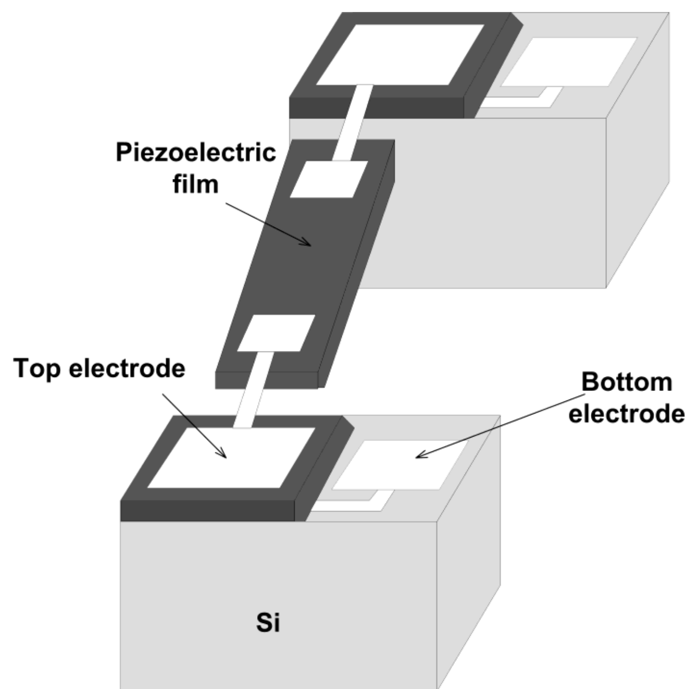


Fig. 5.4: Diagram of a typical FBAR

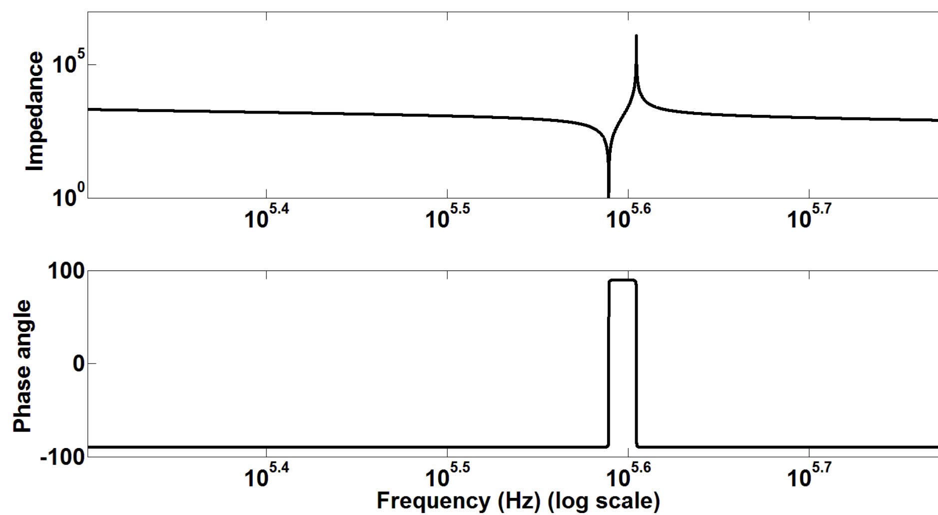


Fig. 5.5: Characteristics of an FBAR or MEMS resonator

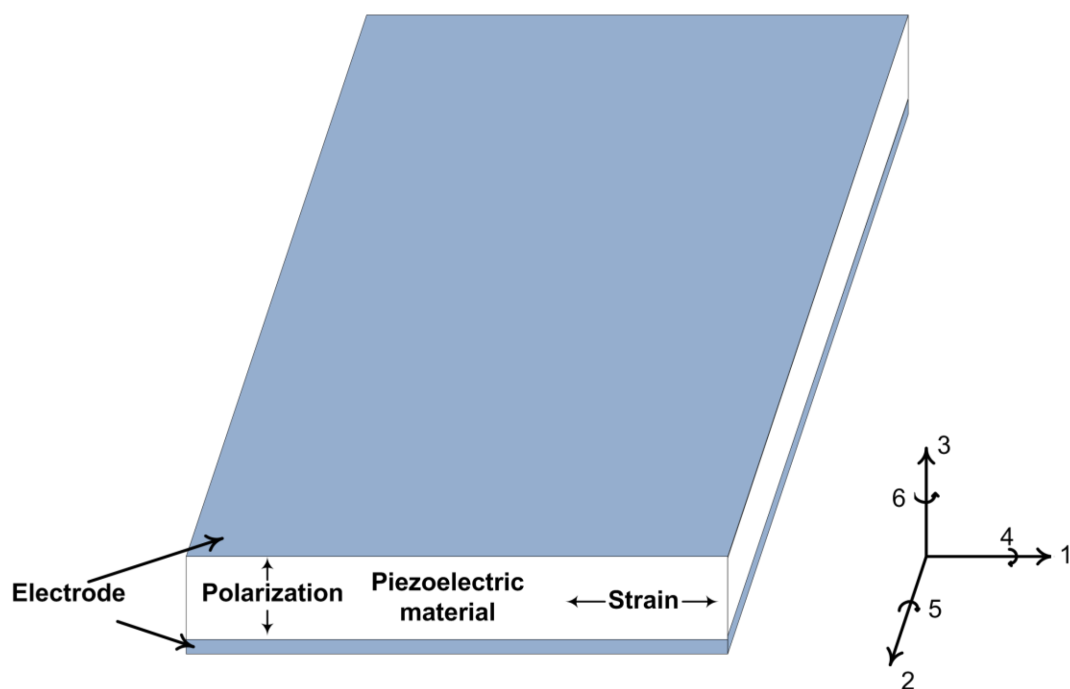
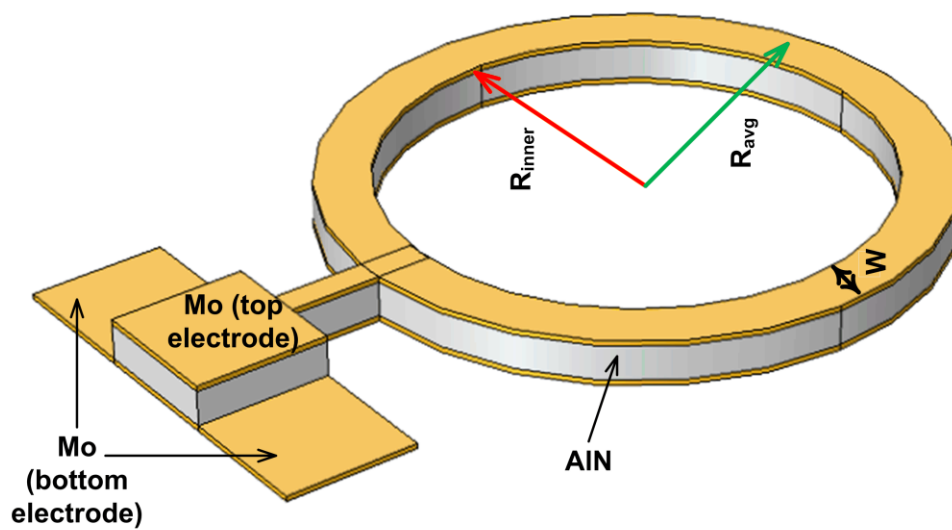
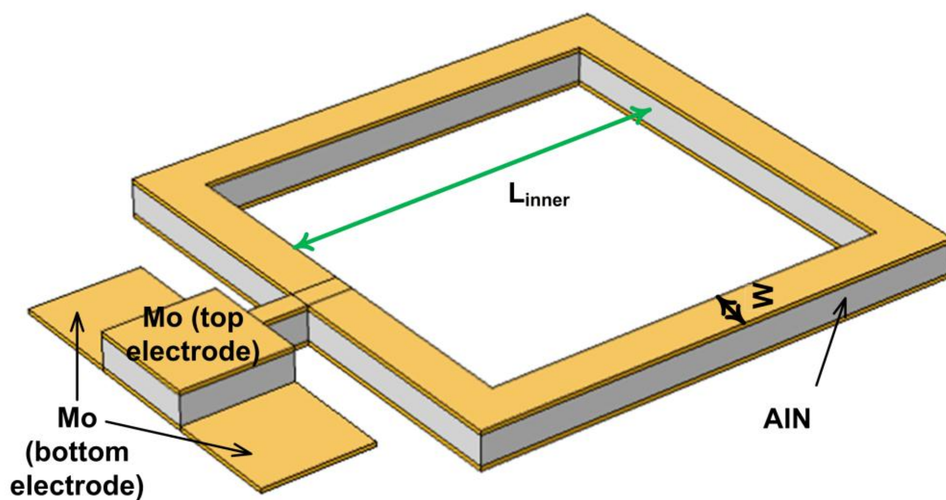


Fig. 5.6: Contour mode piezoelectric resonator. 1) X axis, 2) Y axis, 3) Z axis, 4) sheer around x, 5) sheer around y, and 6) sheer around z .

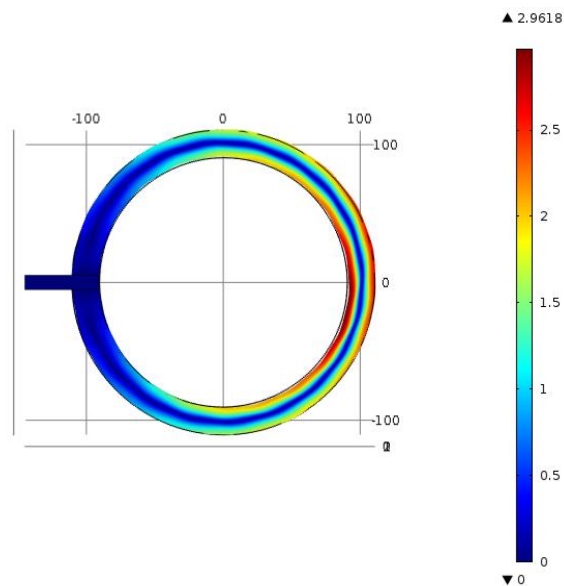


(a)

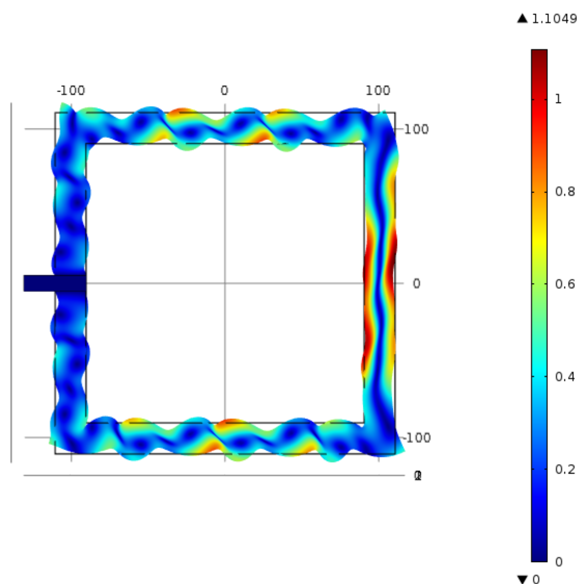


(b)

Fig. 5.7: Schematic diagram of contour mode piezoelectric microresonators on Si (a) circular ring, (b) square shaped ring.

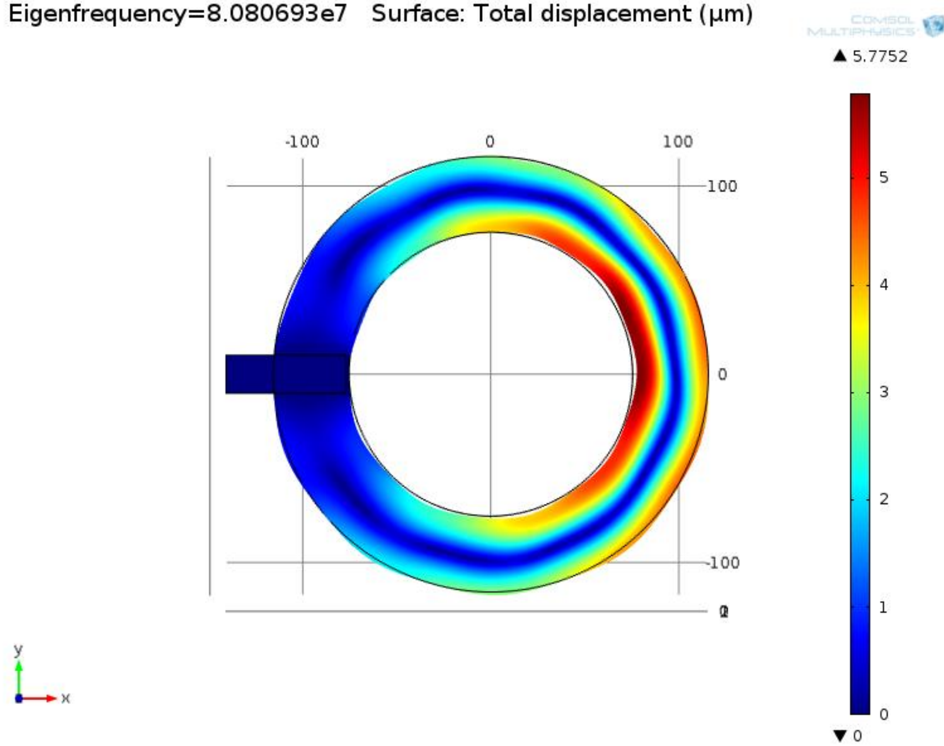


(a)



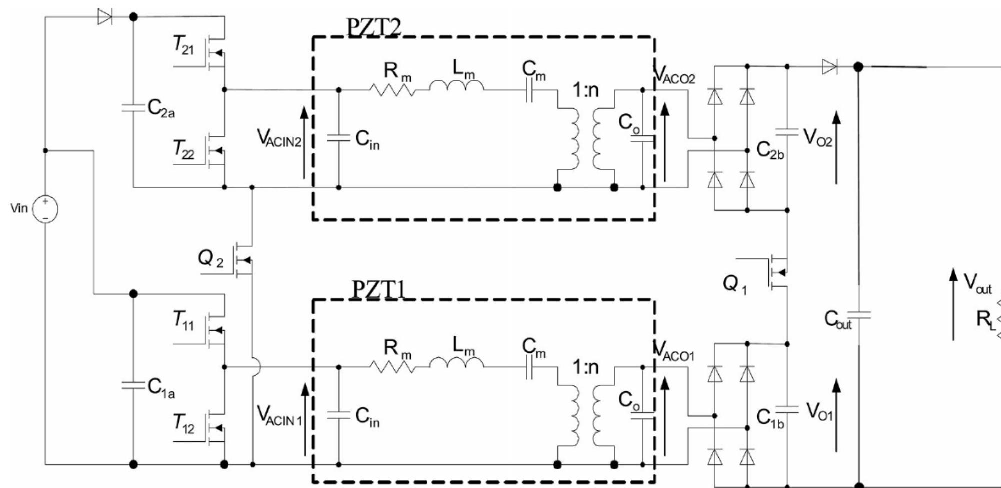
(b)

Fig. 5.8: COMSOL simulation results, nondeformed shape of the devices are presented by solid black lines, (a) W= 20 µm and R_{inner} = 90 µm circular ring; there is a dilation along the width of the device at the resonant frequency (156.4 MHz), (b) W= 20 µm and L_{inner} = 180 µm square shaped ring; there is a dilation along the width of the device at the resonant frequency (156 MHz), (c) W = 50 µm and R_{inner} =75 µm circular ring; there is a dilation (5.7752 µm) along the width of the device at the resonant frequency (80.8 MHz).

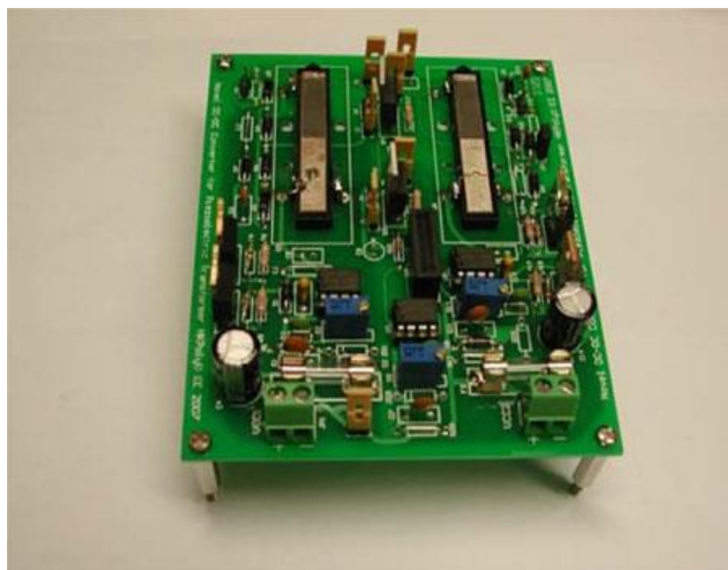


(c)

Fig. 5.8: Continued.

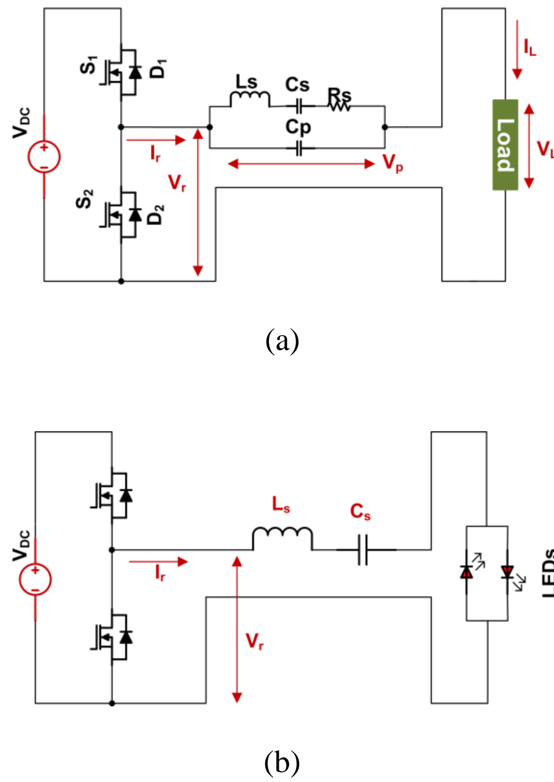


(a)



(b)

Fig. 5.9: Double-level PT based DC-DC converter (a) structure, (b) prototype; © 2012 IEEE [31].



(a)

(b)

Fig. 5.10: Schematic (a) the prototype circuit used for EMI performance comparison incorporating the piezoceramic resonator (b) the conventional discrete L-C components based series resonant converter.

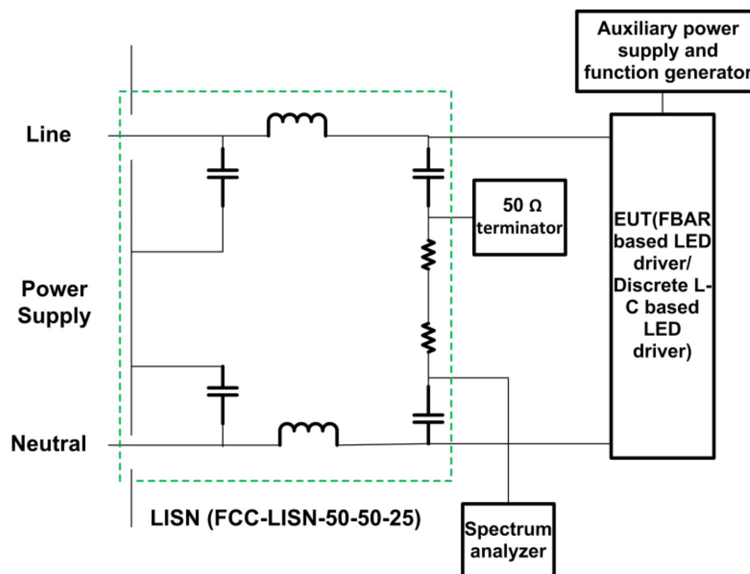
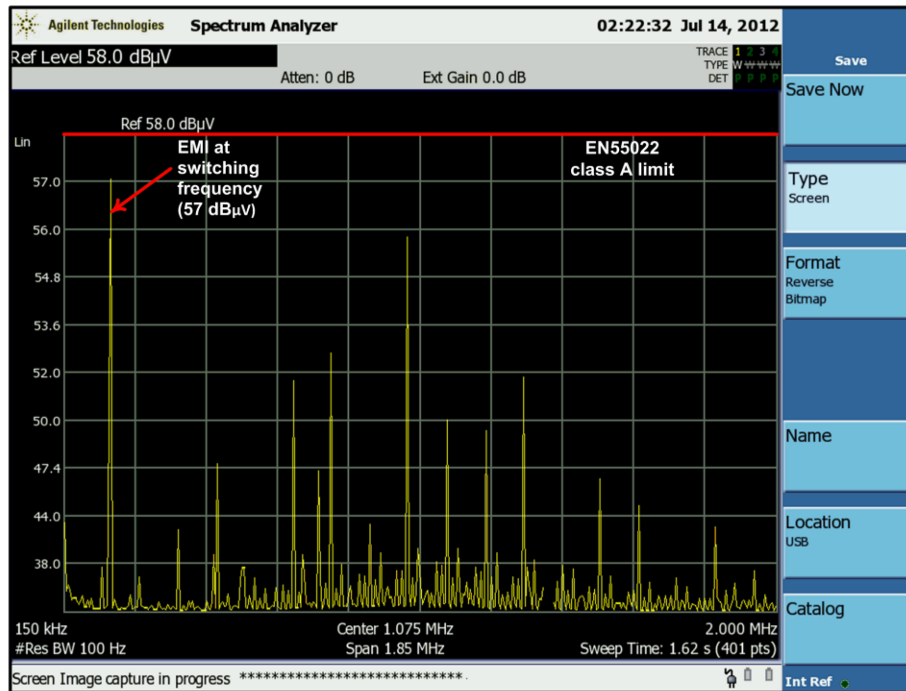
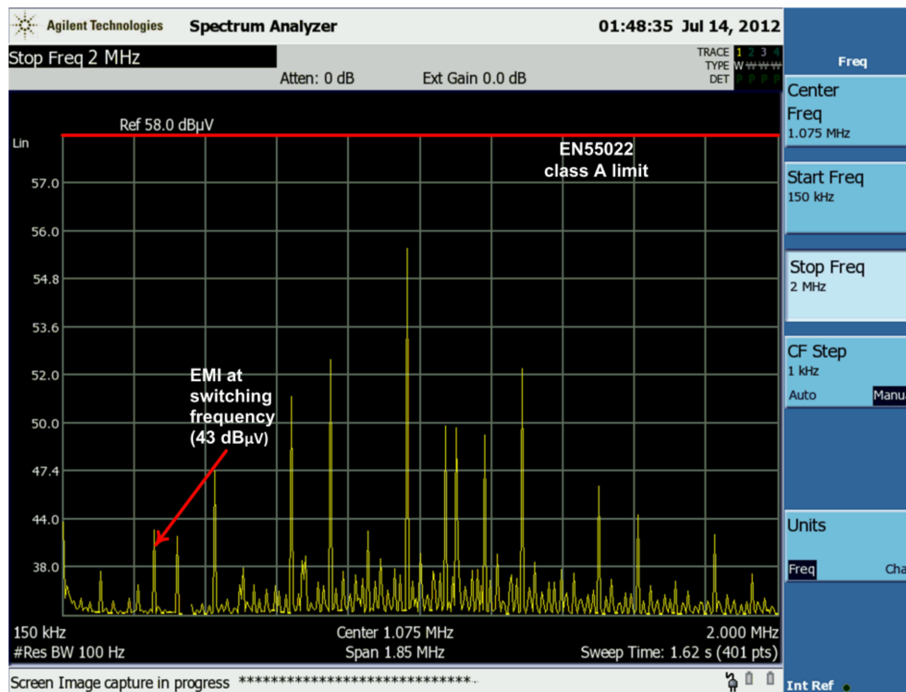


Fig. 5.11: Schematic of the experimental setup used for EMI measurement.



(a)



(b)

Fig. 5.12: Conducted EMI comparison (a) measured EMI: discrete L-C resonant converter (Fig. 5.12b), (b) measured EMI: piezoceramic resonator based resonant converter (Fig. 5.12a).

Table 5.1: Estimated comparison of the state of the art devices to MEMS resonator

<table>
<tr><th colspan="2">Performance Metrics</th><th>Micro inductors (Air core/without thin film magnetic materials)</th><th>Microinductors (with thin film magnetic core)</th><th>Piezoelectric transformers (PZT)</th><th>MEMS Micro resonator (Proposed)</th></tr>
<tr><td colspan="2">Inductance (nH)</td><td>1–10</td><td>20–250</td><td>>10^6</td><td>200–5000</td></tr>
<tr><td colspan="2">Inductance density (nH/mm^2)</td><td>10–200</td><td>50–1500</td><td>1000–10000</td><td>1000–10000</td></tr>
<tr><td colspan="2">Quality factor</td><td>1–10</td><td>5–70</td><td>>1000</td><td>>1000</td></tr>
<tr><td colspan="2">Power Density of the converter (W/mm^3)</td><td>0.01–0.1</td><td>0.1–0.4</td><td>0.1–0.4</td><td>0.05–0.2</td></tr>
<tr><td colspan="2">Efficiency</td><td>80%–95%</td><td>80%–95%</td><td>60%–95% (load dependent parameter)</td><td>40%–80% (load dependent parameter)</td></tr>
<tr><td rowspan="2">Processes</td><td>Deposition process</td><td rowspan="2">Fully compatible with existing CMOS processes</td><td>Screen printing, Electroplating</td><td rowspan="2">Integration has not been reported in the literature yet</td><td>Sputtering</td></tr>
<tr><td>Thickness of the magnetic film (µm)</td><td>3–100 (very thick film)</td><td>0.5–4.0</td></tr>
</table>

CHAPTER 6

FABRICATION AND CHARACTERIZATION OF CONTOUR MODE PIEZOELECTRIC AlN MEMS RESONATOR

Piezoelectric film with very good piezoelectric features is essential for the piezoelectric resonator. A major issue related to fabrication of MEMS resonators is the deposition of highly polycrystalline and well oriented piezoelectric thin films in a repeatable manner. Lead Zirconate Titanate (PZT) is a widely used material for discrete resonators and transformers available in the commercial market. However, it suffers from compatibility issues with the semiconductor fabrication processes and is not acceptable in most CMOS foundries. On the other hand, thin AlN piezoelectric film can be deposited using conventional physical vapor deposition (PVD) tools using Al as the target material. Therefore, the resonator can be integrated easily with CMOS devices.

Table 6.1 gives a comparison of three piezoelectric materials—AlN , ZnO, and PZT in terms of their properties. AlN has higher sound velocity, which means for a given frequency, larger structure can be made with AlN. This gives an advantage for contour mode devices where the resonant frequency is mainly determined by the device length. The high dielectric breakdown voltage of AlN increases the voltage rating of the device fabricated from AlN.

High resistivity of the film ensures good electrical isolation, and a lower dielectric constant means lower parasitic capacitance. This lower capacitance imposes less constraint to achieve zero voltage switching (ZVS). Therefore, AlN is chosen as the piezoelectric film of the proposed resonator.

Developing a new process is a rigorous and time consuming task. In order to define the proper process parameters and suitable etchants at different stages several run of the complete fabrication process was necessary. In this chapter, two fabrication processes are described for fabricating the proposed device. The second process resulted in the devices with proper characteristics. Therefore, the second process will be used in all other future research.

6.1 Fabrication Process on SOI Wafer

The four mask/lithography process starts with an SOI wafer having a heavily doped Si device layer (the resistivity of the top Si layer is .001 ohm-cm with a thickness of 9 μm). These special wafers were supplied by Ultrasil [1]. The bottom Si layer is 500 μm thick and the thickness of the buried oxide layer is 3 μm. 500 nm thin AlN film was deposited using an Advanced Modular Sputtering (AMS) PVD tool (Fig 6.1a). A pure Al is used, and Ar/N_2 forms the plasma for the deposition. This process was performed in an outside commercial foundry [2] in order to achieve a highly c-axis (002) oriented AlN film with good polycrystalline structures. The uniformity of the film was verified by optically based film thickness measurement using Nanospec (AFT model 3000). The uniformity was better than 1% for a 100 mm (4 inch) wafer.

Dry etching is the preferred etching process for AlN. Cl_2 based inductively coupled

plasma (ICP) reactive ion etching (RIE) is widely used for this purpose. Unfortunately, Utah Nanofab does not have this etching process available and therefore, wet etching in warm phosphoric acid was adopted to etch AlN for this device. This etch rate depends strongly on the temperature of the acid. It is also difficult to achieve good uniformity over the entire wafer. Therefore, careful inspection was necessary during wet etching of AlN, and efforts will be given to implement a dry etch process for AlN for future devices. Phosphoric acid at 100 ^{o}C etches the AlN layer and opens up the area for the bottom electrode (Fig. 6.1b)

The Al metal layer was deposited in the next step. This layer was patterned using Al-11 etchant to create top and bottom electrodes (Fig. 6.1c). Wire bonding to Si is not feasible; therefore, it was necessary to deposit Al on top of Si for the bottom electrodes (Fig. 6.1c). Phosphoric acid at 100 ^{o}C was used again to etch AlN in order to form the device's structure (Fig. 6.1d). The well-known Bosch deep reactive ion etching (DRIE) process was used to etch the top 9 µm Si layer. In the Bosch process SF_6 etches the Si, and C_4F_8 polymer is deposited on sidewalls to prevent undercut. In this way very deep trenches with straight side walls can be created. The resonator structure was completed with this step (Fig. 6.1d).

However, the structure needs to be released in order to resonate. This can be achieved by etching the 3 µm buried oxide layer. In order to release the large dimensioned structures, several hours of oxide etching in Buffered Oxide etchant (BOE) is necessary. BOE (HF:NH_4OH) is a strong etchant and attacks both Al and AlN. Therefore, it is not feasible to use BOE for a long duration as it will destroy the device structure, and for the same reason it was necessary to etch the device through the Sidebottom surface. The 500

μm handle Si layer was etched with the same Bosch DRIE process (SF_6:C_4F_8) to reach the buried oxide layer from the back side (Fig. 6.1e), and a careful back side lithography was necessary to achieve this. Dry etching using CF_4:O_2 plasma was used to etch the oxide layer and release the structure (Fig. 6.1f). Fig. 6.2a and 6.2b show the microscopic snapshots of the devices before back-side lithography (corresponding to Fig. 6.1d), and the microscopic image of the final devices are shown in Fig. 6.2c and Fig. 6.2d

6.2 Fabrication Process on Si Wafer

The second process starts with a *p*-type Si wafer. This is a three masks/lithography process. A thin AlN seed layer (30 nm) is deposited to grow highly textured Molybdenum (Mo) bottom electrode (200 nm). This textured Mo layer enables the growth of highly c-axis oriented AlN film. Highly c-axis oriented AlN film is essential to achieve good piezoelectric properties. The AlN seed layer also acts as a buffer layer to reduce losses through the Si substrate.

2000 nm AlN film on top of Mo was deposited next using an Advanced Modular Sputtering (AMS) PVD tool (Fig. 6.3a). This layer is used for piezoelectric actuation. A pure Al target is used during deposition, and Ar/N_2 forms the plasma for the deposition. This process was performed in an outside commercial foundry [2] in order to achieve highly c-axis (002) oriented AlN film with good polycrystalline structures. The uniformity of the film was verified by an optically based film thickness measurement using Nanospec (AFT model 3000). The uniformity was better than 1% for a 100 mm (4 inch) wafer.

X-Ray diffraction (XRD) rocking curve (provided by the foundry, shown in Fig. 6.4)

analysis has been used to verify the c-axis (002) orientation of the sputtered AlN film. A coupled scan of a single crystal produces only one Bragg peak in the diffraction pattern, and this peak is at 17.75^{o} for c-axis (002) orientation [3]. Full width at half maximum of the peak of the XRD rocking curve is only 1.06^{o}, as shown in Fig. 6.4. In general, values below 2° are considered good indications of high quality, well-oriented films [4]. Some measured materials coefficients of the AlN thin film are listed in Table 6.2.

Most of the common developers found in the foundries tend to attack AlN film. The most common developers contain NaOH. NaOH reacts with AlN film even at room temperature. Metal ion free (MIF) developers contains TMAH (tetramethylammonium hydroxide), which also reacts with AlN. Therefore, it was necessary to use a masking layer on top of the AlN film for reliable photolithography. A very thin layer of Mo (20 nm) was deposited by DC sputtering as the masking layer (Fig. 6.3b).

First lithography defines the device structure. Four step etching was performed to remove four layers (Mo-AlN-Mo-AlN) to reach the original Si layer (Fig. 6.3c) Al-11 etchant etches Mo and removes the masking layer. Al-11 etchant also attacks the AlN film, which is very slow at room temperature (<5 nm/min). Warm (80 ^{o}C) phosphoric acid (H_3PO_4) bath increases the AlN etch rate significantly (~2 μm/min). Therefore, about a minute etch in warm H_3PO_4 was performed after Al-11 etching to remove the actual piezoelectric AlN layer. Mo etching with Al-11 etchant was performed again to etch the bottom Mo layer. The AlN seed layer was removed by etching again in warm H_3PO_4. Warm H_3PO_4 does not etch Mo; therefore, Mo can be used as a mask as well as an etch stop layer while etching with warm H_3PO_4.

Second lithography opens up the area for the bottom electrode (Fig. 6.3d). Al-11

etching followed by warm H_3PO_4 etching was repeated again during second lithography to remove the top Mo and AlN layers, respectively. This finishes all of the lithography process associated with AlN. Therefore, the top masking layer was removed completely with a very short dry etching in XeF_2 (Fig. 6.3e). A microphotograph of the device at this stage is shown in Fig. 6.5a.

The top metal layer (Al with thickness of about 250 nm) was deposited by DC sputtering in the next step. This Al layer was patterned using warm H_3PO_4 at 35 ^oC to create the top electrode (Fig. 6.3f). The etch rate of Al and AlN in warm H_3PO_4 at 35 ^oC is 50 nm and 1 nm, respectively. Therefore, this step can efficiently remove the Al layer without attacking underneath AlN and Mo layers.

The final step was to release the resonator by etching the Si layer. Interestingly, all the etchant that etches Si etches Mo also. The etch ratio of Si to Mo in dry XeF_2 is about 50:1, which was obtained experimentally. Therefore, the resonator can be released by etching in dry XeF_2 without any significant undercut of the Mo layer (Fig. 6.3g). There is almost no attack on Al/AlN layers by dry XeF_2 etching. A microphotograph of the released device is shown in Fig. 6.5b.

6.3 Device Characterization

Typically, devices operating at high frequencies are characterized on the wafer with RF probes connected to a vector network analyzer [5]. The fabricated resonators need to be wire-bonded in order to utilize them in the power converter. Therefore, it is necessary to characterize the devices along with wire-bonding. In order to do so, the devices have been diced from the wafer and glued to a PCB. A Grounded coplanar waveguide (CPW)

is designed on a PCB to test the devices.

A picture of the PCB layout designed to characterize the device is shown in Fig. 6.6. The characteristic impedance of the designed waveguide structure is close to 50 Ω in order to match that of the measurement setup. The dielectric material of the PCB is an FR-4 laminate with dielectric constant ε_r in the range of 4.2 to 5 and with a thickness of (h) 1.5748 mm (0.062 in). The characteristic impedance of the CPW of Fig. 6.6 is Z_0 = 51.59 Ω. The equations to calculate Z_0 for grounded CPW are included in section 6.4. The schematic of the experimental set up is shown in Fig. 6.7a, and the actual PCB with diced and wire-bonded resonators is shown in Fig. 6.7b.

The S_{11} parameter of the device obtained from the vector network analyzer was converted to impedance magnitude (in dBΩ) and phase angles. The impedance of the devices fabricated using the fabrication process described in section 6.2 in Fig. 6.8 and Fig. 6.9. The resonant frequencies of the circular and square shaped ring resonators are 183 MHz and 193 MHz, respectively, which are slightly higher than those obtained in the simulation. However, the Q-factor of the resonator is low (~100), which impeded the implementation of the device in a power converter. Nonoptimized anchoring and electrode designs may lead to this low Q. These issues has been solved through experimentation, and the devices fabricated using the process described in section 6.2 have a comparatively high Q-factor.

The impedance magnitude of the device fabricated using the process described in section 6.2 has been plotted in Fig. 6.10a. The unloaded Q-factor of the device is measured to be >1000. The data from Fig. 6.10a can be used to obtain the equivalent circuit parameters of the resonator shown in Chapter 5 in Fig. 5.1. The reactance of the

device at much higher frequencies than the resonant frequencies is used to calculate C_P, because C_P dominates the reactance at those frequencies. The following equations are used to obtain C_S [3]:

$$\left(\frac{f_P}{f_s}\right)^2 = 1 + \frac{1}{r} \tag{6.1}$$

$$r = \frac{C_P}{C_S} \tag{6.2}$$

where f_s and f_p are the resonant and antiresonant frequencies of the resonator. These are found to be 87.28 MHz and 87.4 MHz, respectively. The SEM image of the device is shown in Fig. 6.10b. With C_s known, L_s can be obtained from the following:

$$f_s = \frac{1}{2\pi\sqrt{L_s C_S}} \tag{6.3}$$

The impedance at the resonant frequency f_s is the motional resistance R_s shown in Fig. 5.1. The equivalent electrical circuit model of the resonator is shown in Table 6.3. The important point to note is this circuit model is only valid for resonators with high Q factors. The impedance of this model is given by

$$Z(\omega) = \frac{R_S + j(\omega L_S - \frac{1}{\omega C_S})}{-(\omega L_S - \frac{1}{\omega C_S} - \frac{1}{\omega C_P})(\omega C_P) + j(R_S \omega C_P)} \tag{6.4}$$

The magnitude of the impedance (in dBΩ) of the equivalent circuit model is plotted on the same plot with the experimental data in Fig. 6.10a. The model resembles the experimental data with <2% average error. Note, there are several additional peaks in Fig. 6.10a. These are due to spurious modes of vibration. The ring is not perfectly circular in shape due to fabrication issues, which cause the spurious modes of vibration. However, the spurious modes are weak compared to the fundamental mode and hence are neglected in the equivalent circuit model. We believe that as the fabrication process is perfected, these peaks will be further reduced.

Using (5.9) and (5.10), f_S and R_S calculated to be approximately 100 MHz and 34 Ω, respectively (thickness T = 2 μm), for the resonator corresponding to Fig. 6.10. These values are close to the experimental results. Therefore, (5.9) and (5.10) provide satisfactory estimation of f_S and R_S for a contour mode piezoelectric resonator.

As mentioned in section 5.2, the width W of the device can be set in the designed layout to obtain the desired resonant frequency according to (5.9). Therefore, different dies on the wafer had resonators with different *W*. Fig. 6.11a shows the impedance magnitude of another resonator with different dimensions (R_{inner} = 75 μm and W = 35 μm). The f_S and f_P are found to be 126.4 MHz and 126.48 MHz, respectively, in Fig. 6.11a, and the unloaded Q-factor of the device is measured to be $Q_S \approx 2100$. The parameters of the equivalent electrical circuit model corresponding to this resonator are

provided in Table 6.4. The calculated f_S and R_S corresponding to the dimensions of this resonator are approximately 142 MHz and 55 Ω, respectively. Therefore, by decreasing W, higher resonant frequencies can be achieved. The SEM image of the device is shown in Fig. 6.11b.

As the resonant frequency of the device increases, the operating frequency of the converter increases as well. This in turn reduces the range of the dead time (i.e., $0 \le t_d \le T/4$), which may not be sufficient to charge/discharge C_T. Moreover, the losses associated with switching the FETs also increases with the operating frequency [7]. The switching losses are negligible if the ZVS condition is ensured. However, the gate switching loss is proportional to the switching frequency [7]. In order to facilitate the design of the converter, the resonant frequency of the contour mode device should be as low as possible. This will increase the efficiency of the converter as well.

Equation (5.9) suggests that a device with a larger W can exhibit a smaller resonant frequency. Residual stress gradient issue in suspended thin film devices (e.g., the variation of stress in the direction of the film growth) is a very well known phenomenon in MEMS research. The devices may warp in the z-direction due to this stress once released [8]–[10]. Therefore, the suspended microstructure should not be too long to avoid stress large enough to damage the device. In general, the length can be at most 200 times higher than the film thickness to minimize warping. This sets the resonant frequency limit of the contour mode ring shaped MEMS resonator (the total thickness of the Mo-AlN-Al film stack resonator is approximately 2.4 μm). However, a slight warp in the z-direction still exists, which is in the range of 2–3 μm for the resonators corresponding to Fig. 6.10 and 6.11. In our observation, this small warp did not have any

noticeable effect on the performance of these devices. Fig. 6.12 shows the impedance magnitude of another resonator with a larger W (R_{inner} = 110 μm and W = 65 μm) than that of the resonator corresponding to Fig. 6.10. The f_S and f_P are found to be 74.04 MHz and 74.22 MHz, respectively, in Fig. 6.12. The resonant frequency has been reduced due to the larger W. However, the warp in the z-direction has been increased to approximately 10–12 μm. This resulted in a low $Q_S \approx 350$ of the resonator. Due to this low Q_S (<2000), it is not possible to obtain the equivalent electrical model. For the same reason, this device cannot be used in a power converter.

All the possible dimensions of the resonators were set through simulation in COMSOL Multiphysics. The spurious modes of vibration are less pronounced for the devices having mentioned dimensions as seen from the finite element simulations.

This residual stress issue could be avoided by depositing a thicker film. However, depositing higher thickness of AlN film is expensive and time consuming. Moreover, it is difficult to maintain very good piezoelectric quality for the thick film. Depending on the characteristics of the devices fabricated at this initial stage, it can be concluded that the lowest resonant frequency of the ring shaped contour mode resonators should be in the range of 80–90 MHz to achieve sufficient Q_S with a 2 μm thick AlN film.

The efficiency of the converter can be improved by decreasing the R_S of the resonator, and this can be achieved by increasing the R_{avg} according to (5.10). Therefore, the device corresponding to Fig. 6.10 has a smaller R_S compared to that of the device corresponding to Fig. 6.11. The same residual stress gradient issue as discussed above puts a limit on the R_{avg} also. The resonator corresponding to Fig. 6.10 has the

highest R_{avg} (100 μm) among the resonators exhibiting sufficient Q_S, and therefore has the lowest R_S. This resonator also exhibits the highest Q_S, which can be related to the larger volume of the structure. It has been reported in [11] that Q_S tends to increase with volume for microresonators.

6.4 Appendix

Coplanar waveguide (CPW) is an electrical transmission line which can be easily incorporated on a PCB, and used to convey microwave signals. Fig. 6.13 shows the cross-section of a grounded CPW consists of a single conducting track of width a printed onto a dielectric substrate (the dielectric constant ε_r) with a pair of return (ground) conductors, one on either side of the track, separated from the central track by a small gap of W. The width of all the tracks is constants along the length of the track. There is a ground plane underneath to cover the entire design.

The characteristics impedance (Z_0) of a coplanar waveguide with ground can be calculated with the following formulas [12]:

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{\frac{K(k)}{K(k^{\alpha})} + \frac{K(kl)}{K(kl^{\alpha})}}$$

$$k = \frac{a}{b}$$

$$k^{\alpha} = \sqrt{1-k^2}$$

$$kl^{\alpha} = \sqrt{1-kl^2}$$

$$kl = \frac{\tanh(\frac{\pi a}{4h})}{\tanh(\frac{\pi b}{4h})}$$

$$e_{eff} = \frac{1 + \varepsilon_r \frac{K(k^{\alpha})}{K(k)} + \frac{K(kl)}{K(kl^{\alpha})}}{1 + \frac{K(k^{\alpha})}{K(k)} + \frac{K(kl)}{K(kl^{\alpha})}}$$

where, $b = a + w$ and $K(p)$ is an elliptical integral of first kind and can be calculated using the following equations iteratively

$$a_0 = 1$$

$$b_0 = \sqrt{1 - p^2}$$

$$c_0 = p$$

$$a_n = \frac{a_{n-1} + b_{n-1}}{2}$$

$$b_n = \sqrt{a_{n-1} b_{n-1}}$$

$$c_n = \frac{a_{n-1} - b_{n-1}}{2}$$

$$K(p) = \frac{\pi}{2a_n}$$

6.5 References

[1] Ultrasil. (2013). [Online]. Available: http://www.ultrasil.com

[2] OEM Group. (2013). [Online]. Available: http://www.oemgroupinc.com/foundry.php

[3] A. Ababneh *et al*., " c-axis orientation and piezoelectric coefficients of AlN thin films sputter deposited on titanium bottom electrode," *Journal of Applied Science*, vol 259, pp. 59–65, 2012.

[4] R.S. Naik *et al*., "Measurements of the bulk c-axis electromechanical coupling constant as a function of AlN film quality," *IEEE Tran. Ultrason. Ferroelecr., Freq. Control*, vol. 47, no. 1, pp. 292–296, 2000.

[5] C. Doan, (2013). *Characterization at Microwave Frequnecies*, [Online]. Available: http://web.doe.carleton.ca/~nagui/labequip/loadpull/papers/calibration/CascadeMicro_On-Wafer_Characterization.pdf

[6] J. D. Larson *et al*., "Modified Butterworth-Van Dyke circuit for FBAR resonators and automated measurement system," in *Proc*. *IEEE Ultrasoincs Symp*., pp. 863–868, 2000.

[7] A. D. Sagneri *et al*., "Optimization of integrated transistors for very high frequency DC-DC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3614–3626, July 2013

[8] W. Fang and J. A. Wickert, " Determining mean and gradient residual stresses in thin films using micromachined cantilevers," *J. Micromech. Microeng*., vol. 6, no. 3, pp. 420–427, March. 1996.

[9] S. Greek and N. Chitica, "Deflection of surface-micromachined devices due to internal, homogeneous or gradient stresses," *J. Sensors Actuators A: Physical*, vol. 78, no. 1, pp. 182–187, Jan. 1999.

[10] F. Ericson *et al*., "High sensitivity surface micromachined structures for internal stress and stress gradient evaluation," *J. Micromech. Microeng*., vol. 7, no. 1, pp. 219–226, Jan. 1997.

[11] K. L. Ekinci and M. L. Roukes, "Nanoelectromechanical systems," *Review Scientific Instruments*, vol. 76, no.1, pp. 61101-1–61101-12, Jan. 2005.

[12] B. Cadwell, *Transmission line design.* Artech House, Norwood, MA, 1991, pp. 79.

Table 6.1: Comparison of the electromechanical properties of three piezoelectric materials

Property	AlN	ZnO	PZT
Sound velocity (km/s)	11.4	5.35	4.5
Permittivity (ε_3)	9	10	1000
Resistivity (Ωµm)	10^9	10^3	10^5
Dielectric strength (V/µm)	100	10	100
Piezoelectric coupling coefficient (K^2_{t31}) (%)	2.5	2.5	8-12

Table 6.2: Materials coefficients of the AlN thin film

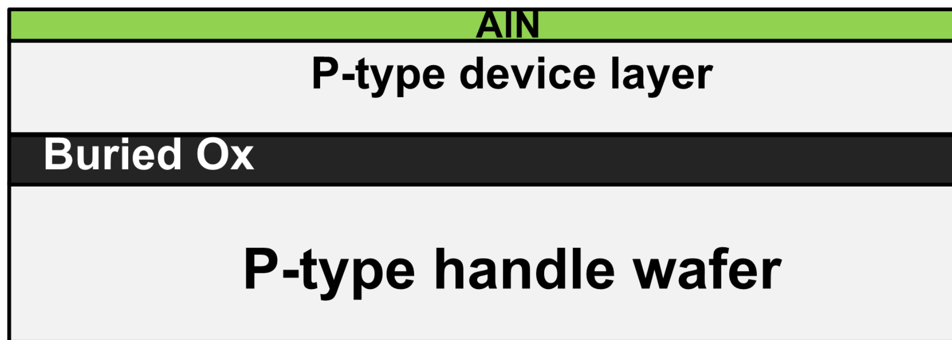
e_{31} (provided by foundry)	-(0.5 - 0.75) C/m^2
Piezoelectric constant (d_{31}) (provided by foundry)	- (1.7 – 1.9) pC/N
Coupling coefficient ($k^2{}_{31}$) (measured)	0.35%
Permittivity (ε_3) (measured)	9-10

Table 6.3: Equivalent electrical circuit model parameters of the fabricated resonator corresponding to Fig. 5.1 in Chapter 5 using the data shown in Fig. 6.9a

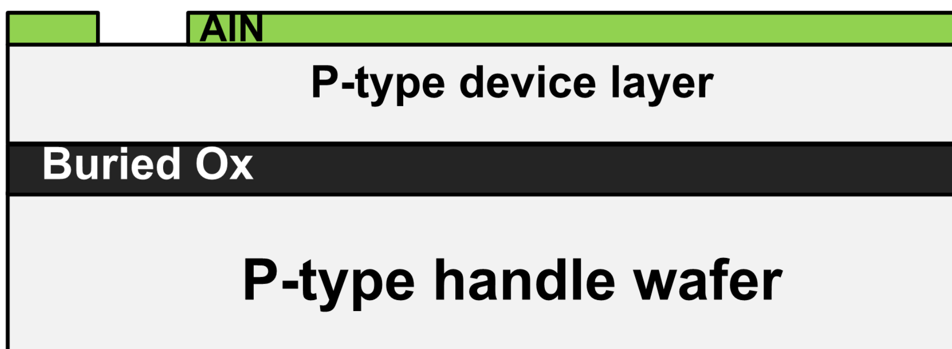
L_S	172.6309 μH
C_S	19.2616 fF
R_S	36.728 Ω
C_P	7 pF

Table 6.4: Equivalent electrical circuit model parameters of the fabricated resonator corresponding to Fig. 5.1 in Chapter 5 using the data shown in Fig. 6.10a

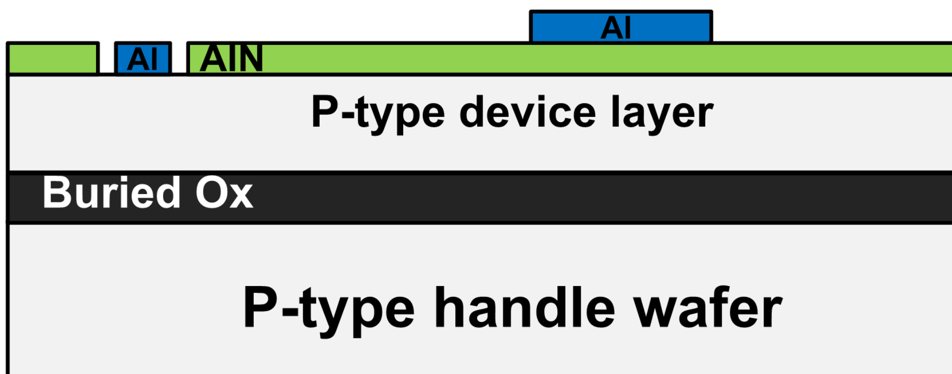
L_S	177.12935 μH
C_S	8.9506 fF
R_S	71 Ω
C_P	7.25 pF



(a)

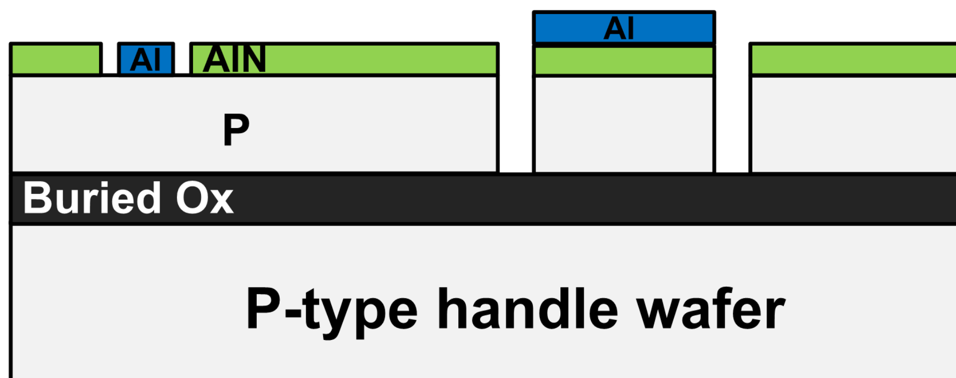


(b)



(c)

Fig. 6.1: Proposed fabrication process (a) sputtering AlN piezoelectric film directly on SOI wafer, (b) opening areas for bottom electrodes (first lithography), (c) deposition and patterning top and bottom electrodes (second lithography), (d) AlN wet etching and Bosch DRIE Si in order to define the device structure (third lithography), (e) backside etching using Bosch DRIE (fourth and final lithography), (f) resonators are released by dry etching of oxide layer.

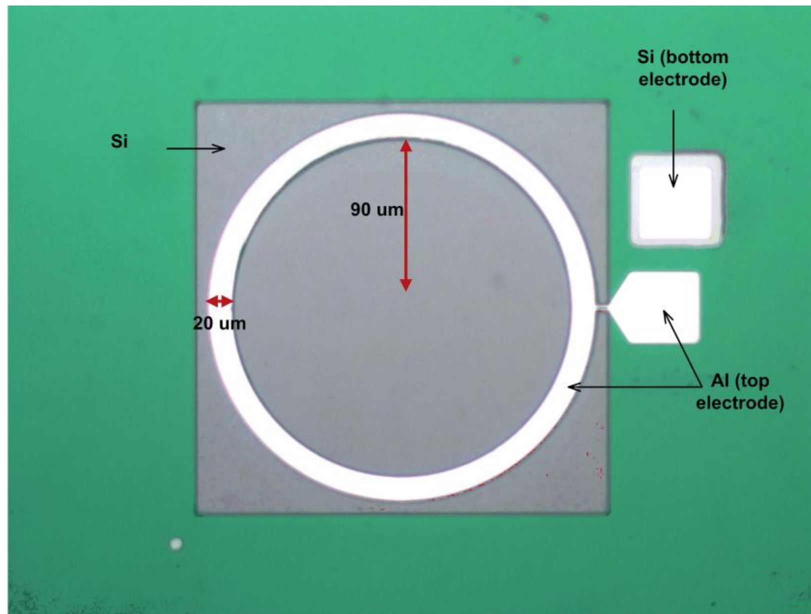


(d)

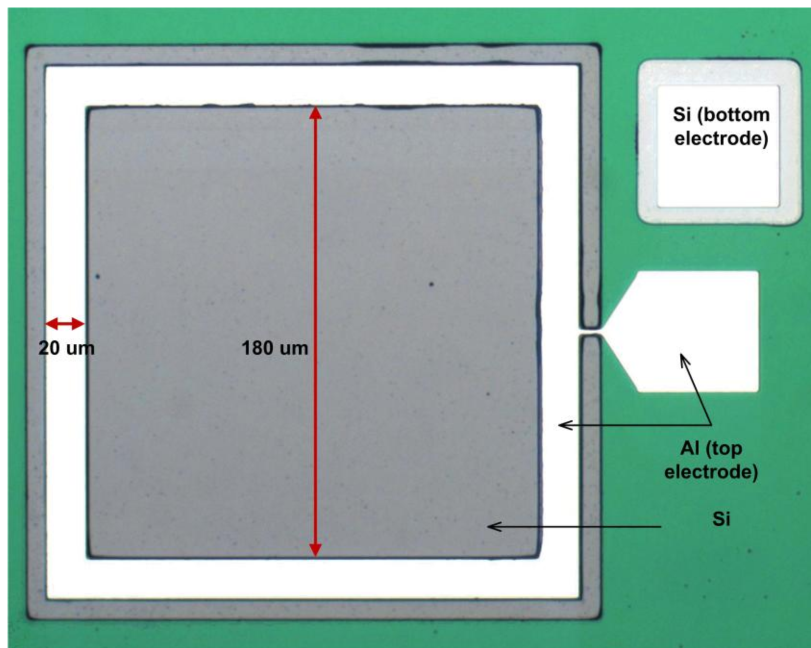
(e)

(f)

Fig. 6.1: Continued.

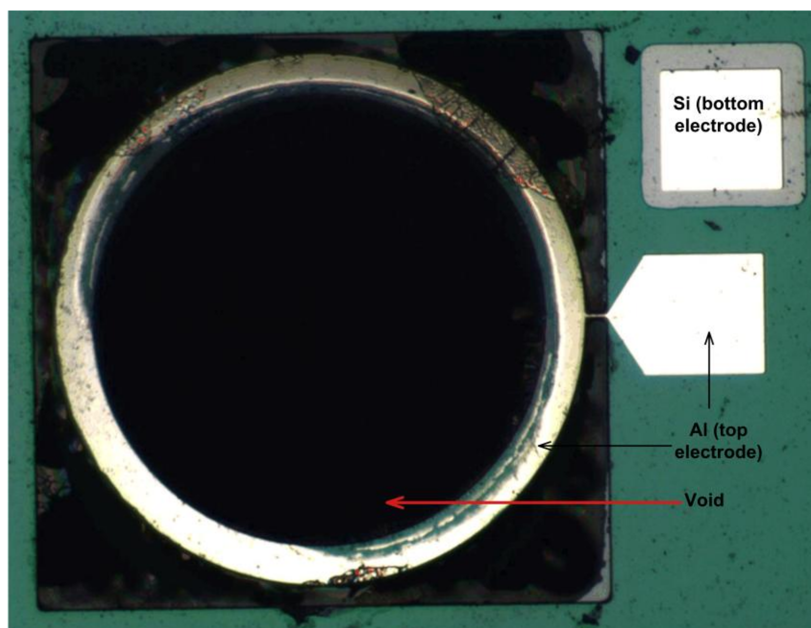


(a)

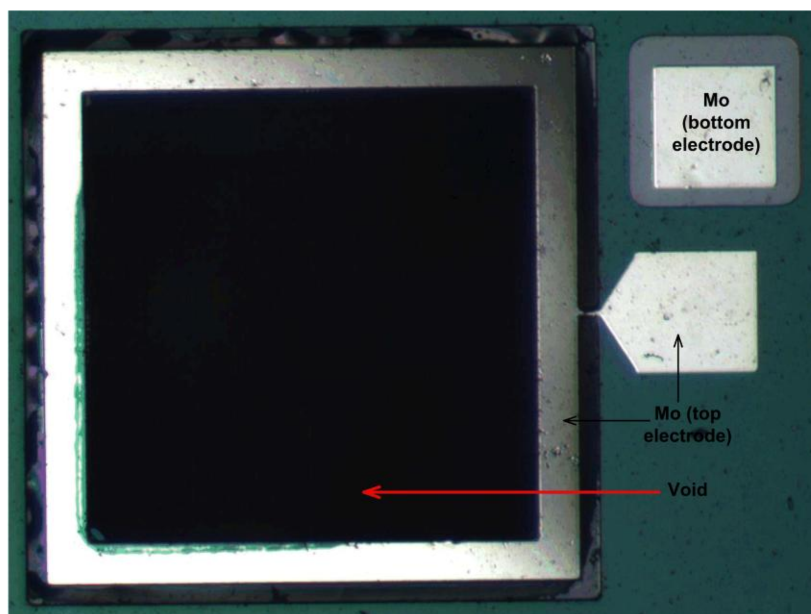


(b)

Fig. 6.2: Microphotographs of the prototype devices (a) circular ring resonator after third lithography (5 times zoomed), (b) square shaped ring resonator after third lithography (5 times zoomed), (c) final circular ring resonator, and (d) final square shaped ring resonator (the green background is the 500 nm thick AlN piezoelectric film).



(c)



(d)

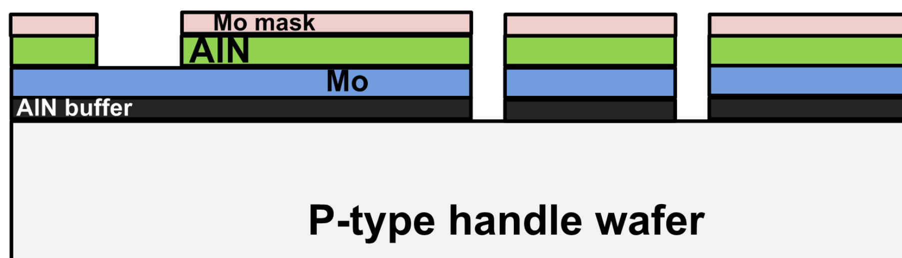
Fig. 6.2: Continued.

(a)

(b)

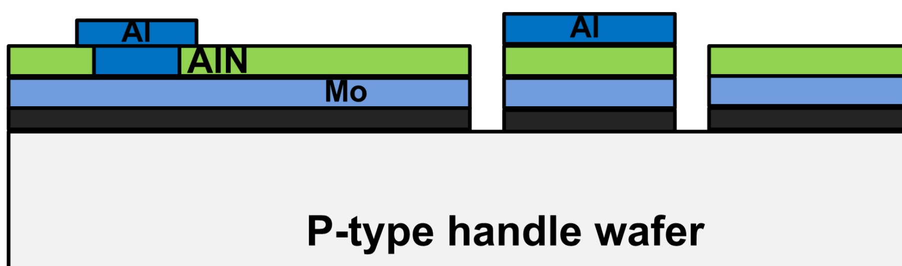
(c)

Fig. 6.3: Proposed fabrication process (a) sputtering AlN buffer layer, Molybdenum (Mo) and AlN (actual piezoelectric film) stack, (b) sputtering Mo mask layer, (c) patterning mask Mo, AlN, Mo, and AlN buffer layer in order to define the device structures (first lithography), (d) opening areas for the bottom electrodes (second lithography), (e) removing Mo mask layer, (f) deposition and patterning top electrodes (third lithography), (g) resonators are released by XeF_2 dry etching the Si layer. XeF_2 has high etch selectivity for Al and AlN (1:2000) to Si. The same of Mo is 1:50.

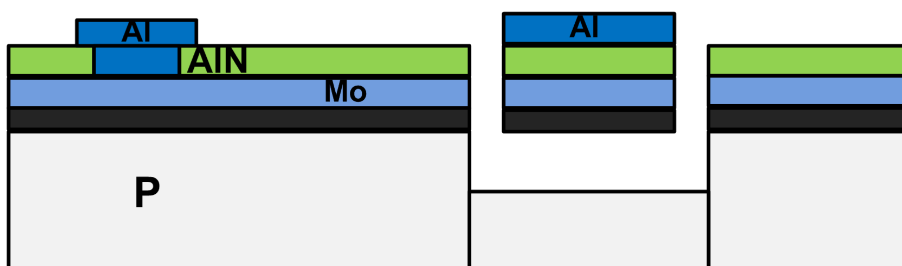


(d)

(e)



(f)



(g)

Fig. 6.3: Continued.

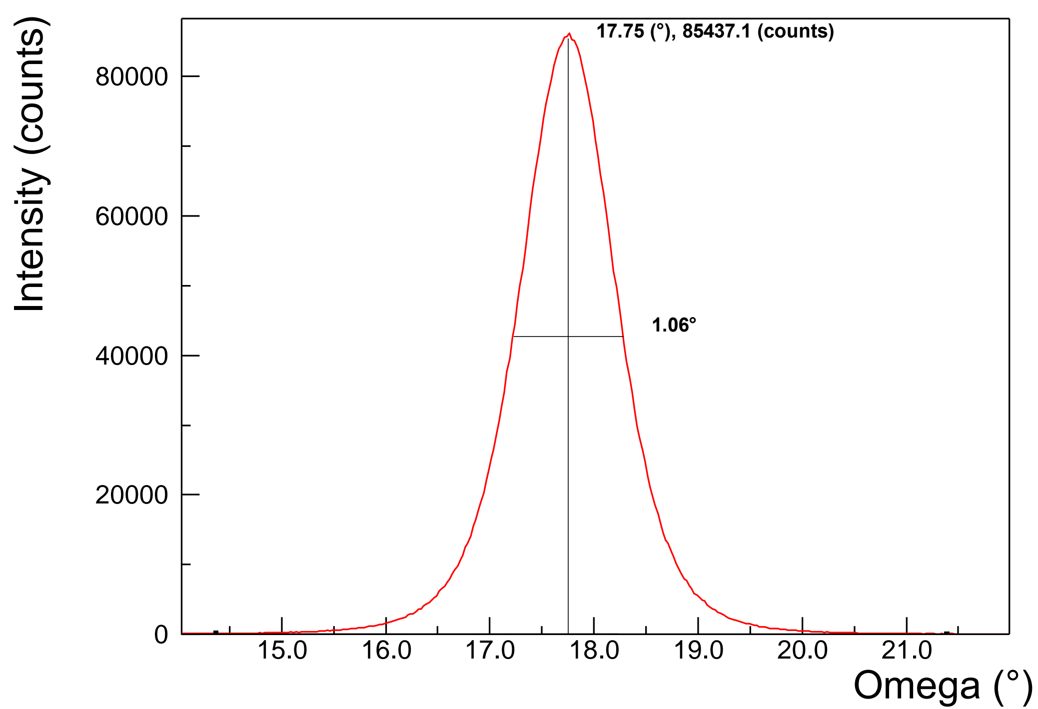
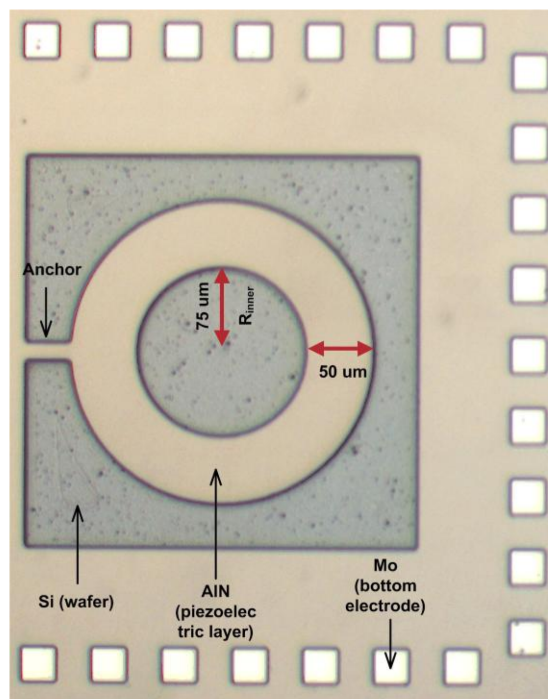
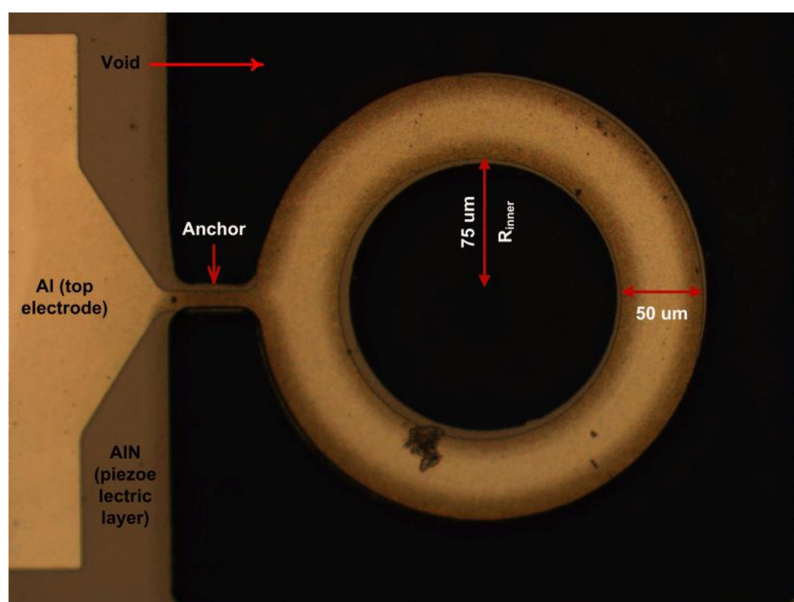


Fig. 6.4: XRD rocking curve of the AlN film (image provided by the foundry)



(a)



(b)

Fig. 6.5: Microphotograph of the resonator (a) after second lithography (10X) corresponding to Fig. 6.3e. The shiny rectangles are the vias to bottom Mo electrode. The gray background is the piezoelectric AlN film, and the dark area is the actual Si layer (b) final resonator (20x) corresponding to Fig. 6.3g.

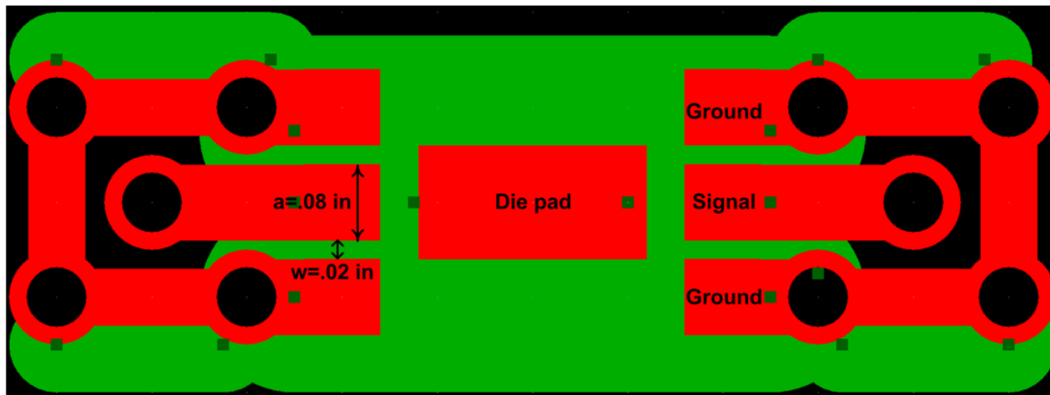
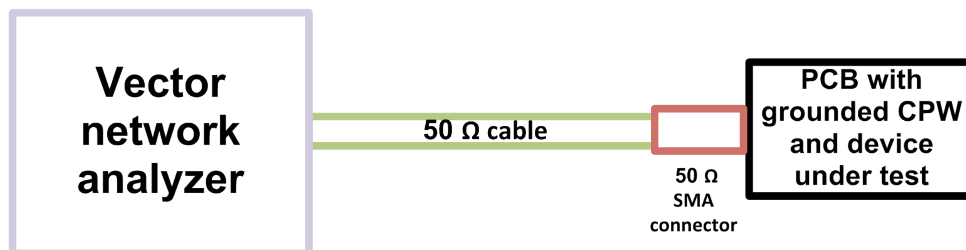
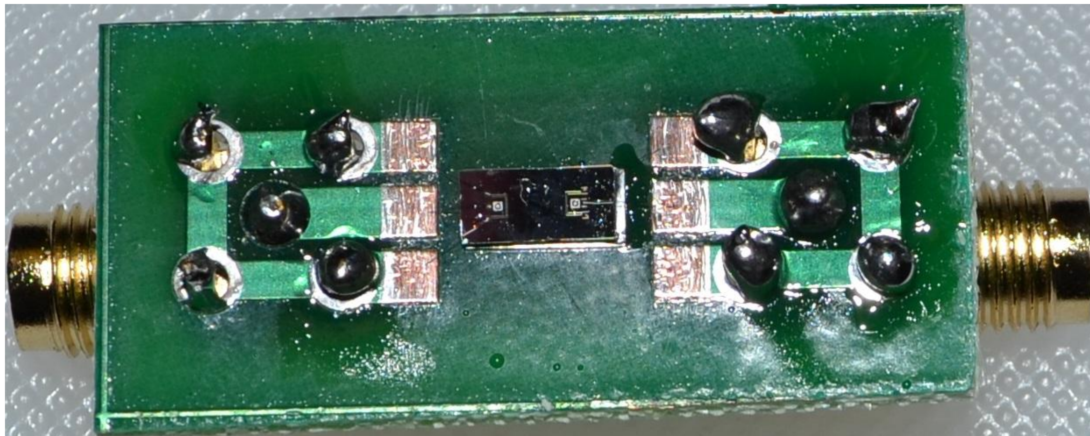


Fig. 6.6: PCB layout with the designed grounded CPW having characteristic impedance $Z_0 = 51.69\ \Omega$. Every die contains two fabricated resonators; thus, there are two CPWs on each PCB

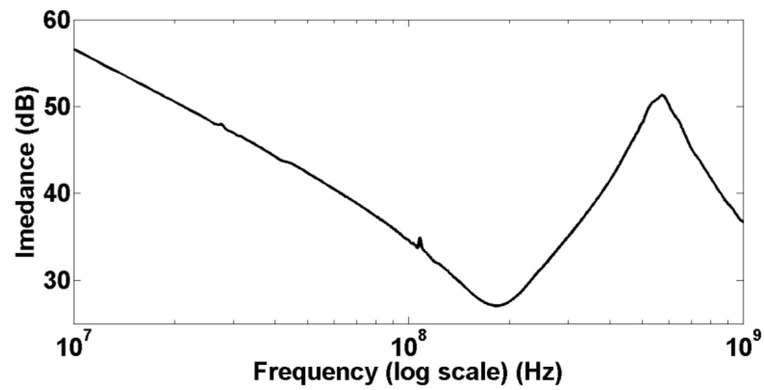


(a)

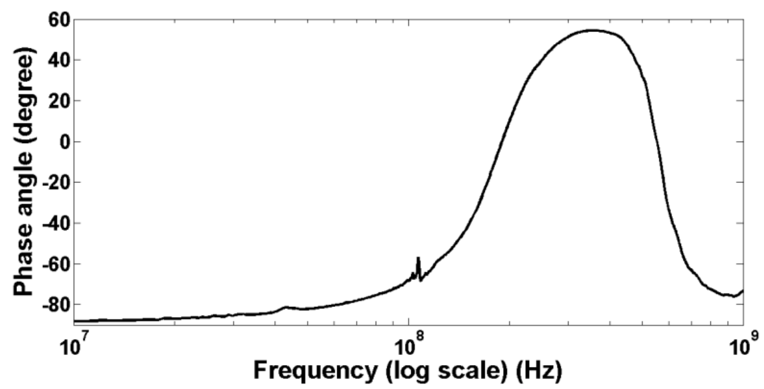


(b)

Fig. 6.7: Prototype (a) schematic of the set up used to characterize the resonators, (b) diced and packaged resonators on PCB with the grounded CPW for testing. Careful inspection of the figure reveals the actual microresonators on the center of the die.

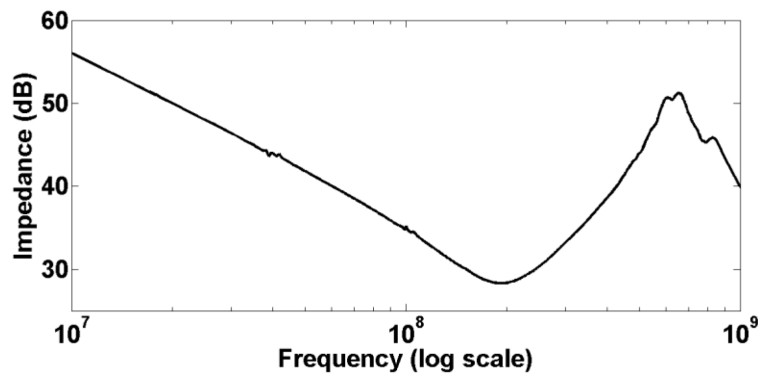


(a)

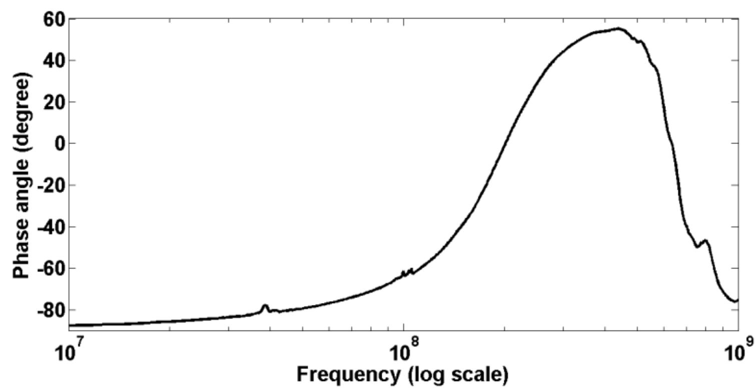


(b)

Fig. 6.8: Fabricated circular ring resonator (a) impedance and (b) phase angle with respect to frequency. The impedance is the lowest at the resonant frequency (183 MHz) where the resonator behaves like a resistor.

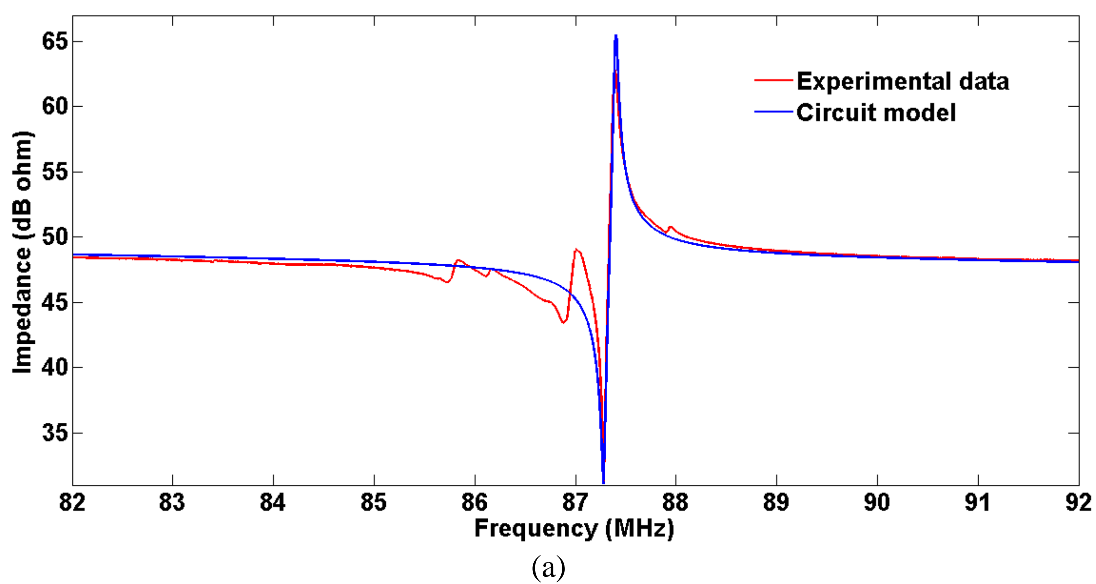


(a)

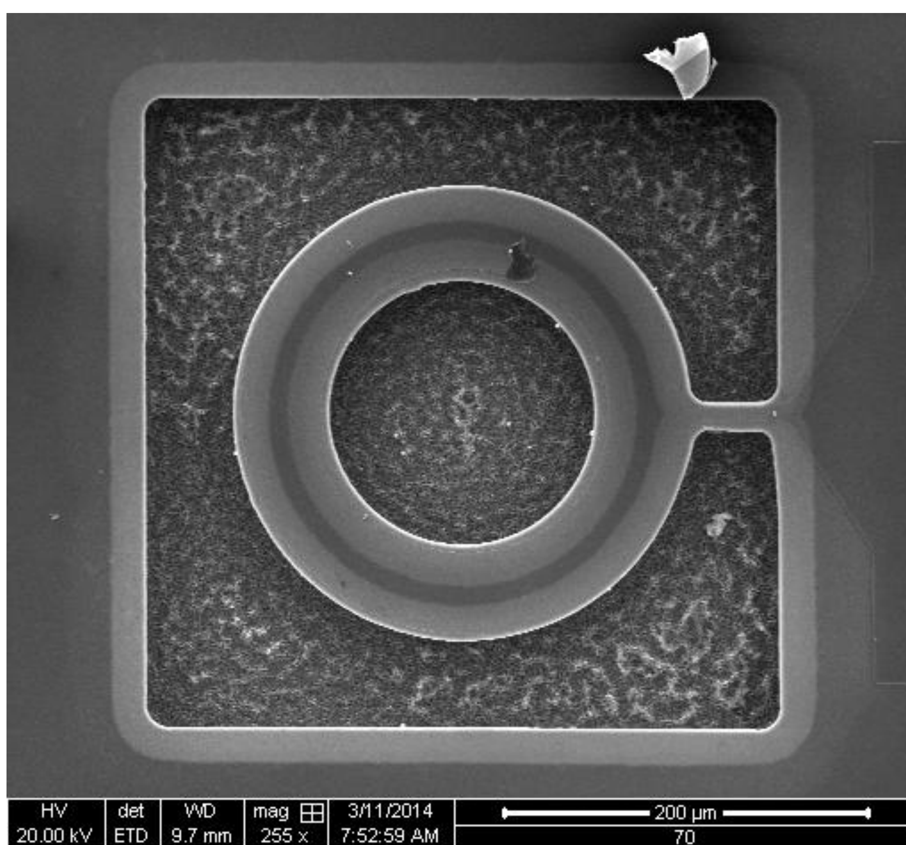


(b)

Fig. 6.9: Fabricated square shaped ring resonator (a) impedance and (b) phase angle with respect to frequency. The impedance is the lowest at the resonant frequency (193 MHz) where the resonator behaves like a resistor.

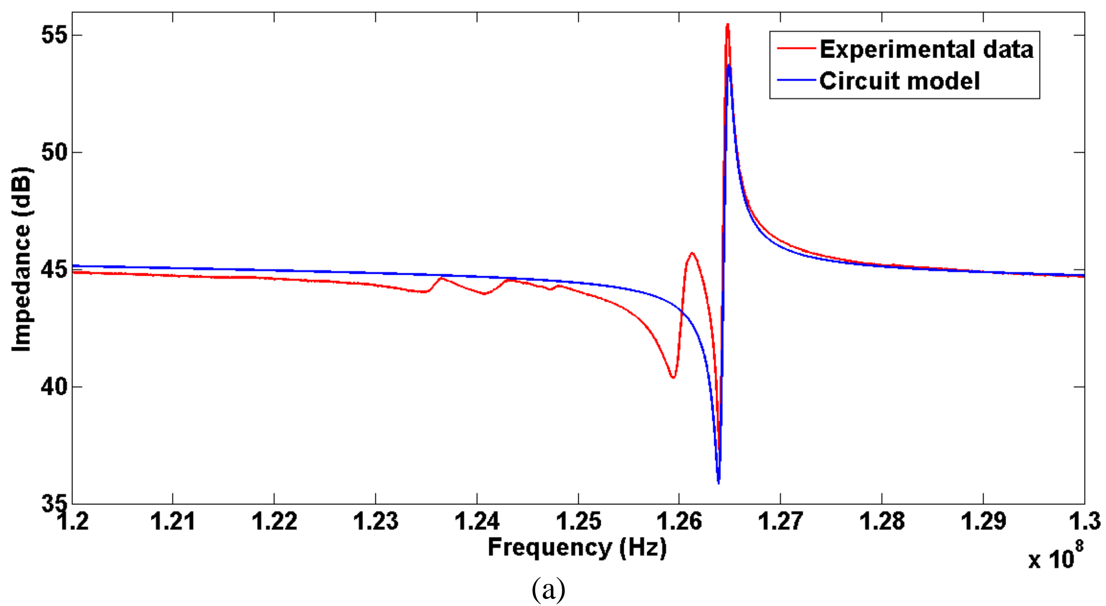


(a)

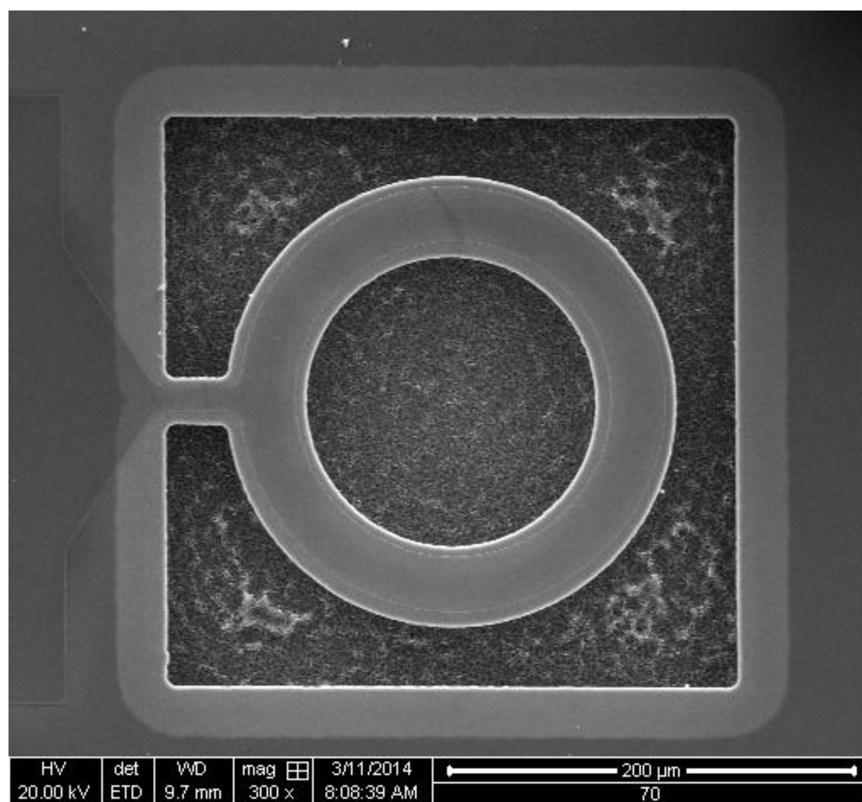


(b)

Fig. 6.10: Fabricated resonator (a) experimental characteristics, (b) SEM image.



(a)



(b)

Fig. 6.11: Fabricated resonator with different dimensions (a) experimental characteristics, (b) SEM image

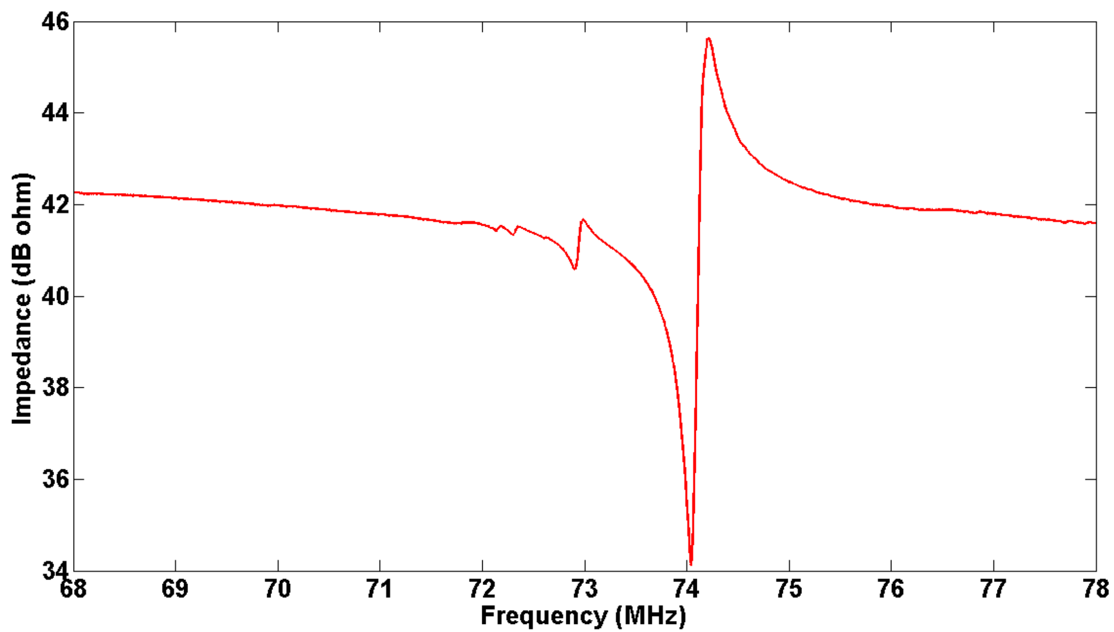


Fig. 6.12: Experimental characteristics of the fabricated resonator with dimensions; R_{inner} = 110 μm and W = 65 μm

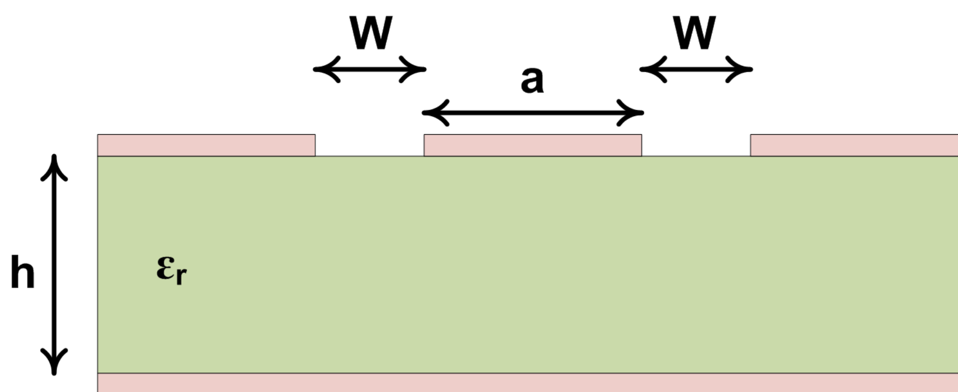


Fig. 6.13: Cross-section of a grounded coplanar waveguide

CHAPTER 7

FEASIBILITY ANALYSIS OF USING MEMS RESONATOR IN SERIES RESONANT CONVERTER

The feasibility of the application of MEMS piezoelectric resonator on Si described in Chapters 6 and 7 in an AC-output series resonant converter is performed through zero-voltage switching (ZVS) analysis using a state space model in this chapter. To the knowledge of the authors, a ZVS model for thin film devices has not yet been reported in the literature. With the equivalent electrical model of the resonator known, this analysis can be used as a guide to design MEMS resonator based series resonant converters. An analysis of the efficiency of the device in the same converter is performed as well.

Similar to piezoelectric transformers (PT), the topologies that are most suitable for use with the microresonators are push-pull, half-bridge, and class –E. Among these, the half-bridge topology is the most widely used driver for PTs. Earlier designs of PT-based power converters used additional series inductors to achieve soft-switching [1]–[5]. In doing so, the advantages of using PT were lost. However, with careful design, it is possible to remove inductors completely from the converter [6]–[12]. The same technique can be applied for microresonators as well.

7.1 Inductorless ZVS Condition of MEMS Resonator Based Converter

The most basic half-bridge series resonant converter is considered here because of its simple architecture. Half-bridge AC output series resonant converters incorporating a MEMS resonator is shown in Fig. 7.1a. Replacing the device with the equivalent electrical model gives the circuit shown in Fig. 7.1b. This circuit is very similar to a conventional LC series resonant converter; however, it has an additional capacitor C_P in parallel with the series L-C tank. A very small capacitor C_O (in the range of a few pF) is added at the output to cancel high-frequency components. The output capacitance of the FET devices C_T (also in the range of a few pF) is added to the analysis.

In order to simplify the analysis, the parallel-connected load resistor R_O and capacitor C_O can be transformed to series-connected equivalents as shown in Fig. 7.2 for a given frequency f.

$$C_{OT} = C_O \frac{1+(\omega C_O R_O)^2}{(\omega C_O R_O)^2} \tag{7.1}$$

$$R_{OT} = \frac{R_O}{1+(\omega C_O R_O)^2} \tag{7.2}$$

where $\omega = 2\pi f$.

The conventional series resonant converter operates at a frequency slightly higher than the resonant frequency to achieve soft-switching or ZVS, and this frequency is typically below 1 MHz. The dead time (time between the high-side FET being turned off

and the tank current zero crossing, i.e., the phase angle at which the tank is operated) requirement between the switching of the half-bridge switches to charge/discharge C_T can be achieved very easily for low-frequency (<1 MHz) operation. The resonant frequencies of the fabricated microresonators presented here are greater than 50 MHz. Moreover, there is an extra capacitor C_P associated with the resonators. These factors make inductorless ZVS with a microresonator quite challenging. Without ZVS, the power dissipation that occurs in the FETs is larger with resonators compared to their discrete components' counterparts due to C_P and the high operating frequency.

The basic requirement for ZVS—the voltage across the capacitor C_T is equal to the DC bus voltage (or clamped by the high side body diode forward voltage to just above the DC bus voltage) when the high-side FET is turned on and equal to 0 V (or clamped by the low-side body diode forward voltage to just below 0 V) when the low-side FET is turned on [9], [10], [13].

The ZVS analysis presented here is based on the circuit of Fig. 7.1b and 7.2. The six different stages of Fig. 7.2 during any switching period are shown schematically in Fig. 7.3a–f. The sequence begins with the high-side FET (S_1) being turned OFF. The corresponding waveforms associated with every stage are shown in Fig. 7.4. This is the case when ZVS is achieved quite easily in the dead time, as indicated by the diode conduction. If the dead time is such that the ZVS is only just achieved, the diodes' conducting stages are absent (stage 2 and stage 5), and the stage sequence is 1-3-4-6. For this case, stage 3 begins as soon as the voltage across C_T is approximately equal to 0 V as depicted in Fig. 7.5. 1-3-4-6 is the sequence when ZVS is not achieved also; however, the voltage across C_T cannot reach close to 0 V within the dead time as illustrated in Fig.

7.6.

In order to minimize dead time/circulating current, it is desirable to set the operation of the converter such that the converter is just below, or just on the point of achieving ZVS. Therefore, an analysis of stage sequence 1-3-4-6 is performed. Assuming equal on time for the low- and high-side FETs permits to analyze stages 1 and 3 only. Therefore, the voltage across C_T at the end of dead time (which is equal for both of the FETs also) can be obtained numerically, and this voltage depends on the resonator's equivalent circuit parameters, converter switching frequency, load resistance, and dead time.

Stage 1 begins at $t = 0$ and ends at $t = t_d$, where, t_d is the dead time (as in Fig. 7.5 and 7.6). Voltage across capacitors C_S, C_P, C_{OT}, and C_T are assigned as state variable x_1, x_2, x_4, x_5, and the current through the inductor is assigned as x_3 (Fig. 7.7a). Then from Fig 7.7a:

$$C\hat{x}_1 = x_3 \tag{7.3}$$

$$R_S x_3 + L_S \hat{x}_3 + x_1 = x_2 \tag{7.4}$$

$$x_2 + x_4 + C_{OT} R_{OT} \hat{x}_4 = x_5 \tag{7.5}$$

$$C_P \hat{x}_2 + x_3 = C_{OT} \hat{x}_4 \tag{7.6}$$

$$C_T \hat{x}_5 = -C_{OT} \hat{x}_4 \tag{7.7}$$

They can be rearranged and combined into the state equation as follows

$$\begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{x}_3 \\ \hat{x}_4 \\ \hat{x}_5 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_S} & 0 & 0 \\ -\frac{1}{R_{OT}C_P}(0 & 1 & R_{OT} & 1 & -1) \\ \frac{1}{L_S}(-1 & 1 & -R_S & 0 & 0) \\ -\frac{1}{R_{OT}C_{OT}}(0 & 1 & 0 & 1 & -1) \\ -\frac{1}{R_{OT}C_T}(0 & -1 & 0 & -1 & 1) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} \tag{7.8}$$

Simplified to

$$\hat{X} = A_1 X \tag{7.9}$$

The solution to the state equation is given by

$$X(t) = e^{A_1 t} X(0) \tag{7.10}$$

where $X(t) = X(0)$ at $t = 0$.

For, $t = t_d$,

$$X(t_d) = e^{A_1 t_d} X(0) \tag{7.11}$$

which implies

$$\begin{bmatrix} x_1(t_d) \\ x_2(t_d) \\ x_3(t_d) \\ x_4(t_d) \\ x_5(t_d) \end{bmatrix} = \begin{bmatrix} k_{11} & k_{12} & k_{13} & k_{14} & k_{15} \\ k_{21} & k_{22} & k_{23} & k_{24} & k_{25} \\ k_{31} & k_{32} & k_{33} & k_{34} & k_{35} \\ k_{41} & k_{42} & k_{43} & k_{44} & k_{45} \\ k_{51} & k_{52} & k_{53} & k_{54} & k_{55} \end{bmatrix} \begin{bmatrix} x_1(0) \\ x_2(0) \\ x_3(0) \\ x_4(0) \\ x_5(0) \end{bmatrix} \tag{7.12}$$

where $e^{A_1 t_d} = \begin{bmatrix} k_{11} & k_{12} & k_{13} & k_{14} & k_{15} \\ k_{21} & k_{22} & k_{23} & k_{24} & k_{25} \\ k_{31} & k_{32} & k_{33} & k_{34} & k_{35} \\ k_{41} & k_{42} & k_{43} & k_{44} & k_{45} \\ k_{51} & k_{52} & k_{53} & k_{54} & k_{55} \end{bmatrix}$,can be obtained using MATLAB, and we define

$$A = \begin{bmatrix} k_{11} & k_{12} & k_{13} & k_{14} \\ k_{21} & k_{22} & k_{23} & k_{24} \\ k_{31} & k_{32} & k_{33} & k_{34} \\ k_{41} & k_{42} & k_{43} & k_{44} \end{bmatrix} \tag{7.13}$$

Stage 3 begins at $t = t_d$ and ends at $t = \frac{T}{2}$, where, $T = \frac{1}{f_s}$, f_s being the switching frequency (Fig. 7.5 and Fig. 7.6). The same state variables and state equation of stage 1 holds true, except there is no state variable x_5. Therefore, from Fig. 7.7b

$$\begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{x}_3 \\ \hat{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_S} & 0 \\ -\frac{1}{R_{OT}C_P}(0 & 1 & R_{OT} & 1) \\ \frac{1}{L_S}(-1 & 1 & -R_S & 0) \\ -\frac{1}{R_{OT}C_{OT}}(0 & 1 & 0 & 1) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} \tag{7.14}$$

Simplified to

$$\hat{X} = A_2 X \tag{7.15}$$

The solution to the state equation is given by

$$X(t) = e^{A_2 t} X(t_d) \tag{7.16}$$

where $X(t) = X(t_d)$ at $t = t_d$.

For, $t = \frac{T}{2}$,

$$X(\frac{T}{2}) = e^{A_2(\frac{T}{2} - t_d)} X(t_d) \tag{7.17}$$

which implies

$$\begin{bmatrix} x_1(\frac{T}{2}) \\ x_2(\frac{T}{2}) \\ x_3(\frac{T}{2}) \\ x_4(\frac{T}{2}) \end{bmatrix} = e^{A_2(\frac{T}{2}-t_d)} \begin{bmatrix} x_1(t_d) \\ x_2(t_d) \\ x_3(t_d) \\ x_4(t_d) \end{bmatrix} \tag{7.18}$$

As the voltage across C_T at $t=0$ is V_D, therefore, $x_5(0)=V_D$. Using (7.12) and (7.13), from (7.18),

$$\begin{bmatrix} x_1(\frac{T}{2}) \\ x_2(\frac{T}{2}) \\ x_3(\frac{T}{2}) \\ x_4(\frac{T}{2}) \end{bmatrix} = e^{A_2(\frac{T}{2}-t_d)} \bullet A \bullet \begin{bmatrix} x_1(0) \\ x_2(0) \\ x_3(0) \\ x_4(0) \end{bmatrix} + e^{A_2(\frac{T}{2}-t_d)} \begin{bmatrix} k_{15}V_D \\ k_{25}V_D \\ k_{35}V_D \\ k_{45}V_D \end{bmatrix} \tag{7.19}$$

Since the dead/off times and on times of the FETs are equal, the initial condition of stage 1 is related to the final condition of stage 3 by the following:

$$x_1(\frac{T}{2}) = -x_1(0) + \frac{C_{OT}}{C_P + C_S + C_{OT}} V_D \tag{7.20}$$

$$x_2(\frac{T}{2}) = -x_2(0) + \frac{C_{OT}}{C_P + C_S + C_{OT}} V_D \tag{7.21}$$

$$x_3(\frac{T}{2}) = -x_3(0) \tag{7.22}$$

$$x_4(\frac{T}{2}) = -x_4(0) + \frac{C_P + C_S}{C_P + C_S + C_{OT}} V_D \tag{7.23}$$

Therefore, the initial conditions $x_1(0)$, $x_2(0)$, $x_3(0)$ and $x_4(0)$ can be found using (7.20)–(7.23):

$$\begin{bmatrix} 1+p_{11} & p_{12} & p_{13} & p_{14} \\ p_{21} & 1+p_{22} & p_{23} & p_{24} \\ p_{31} & p_{32} & 1+p_{33} & p_{34} \\ p_{41} & p_{42} & p_{43} & 1+p_{44} \end{bmatrix} \begin{bmatrix} x_1(0) \\ x_2(0) \\ x_3(0) \\ x_4(0) \end{bmatrix} = \begin{bmatrix} -b_1 + \frac{C_{OT}}{C_P + C_S + C_{OT}} V_D \\ -b_2 + \frac{C_{OT}}{C_P + C_S + C_{OT}} V_D \\ -b_3 \\ -b_4 + \frac{C_P + C_S}{C_P + C_S + C_{OT}} V_D \end{bmatrix} \tag{7.24}$$

Where $\begin{bmatrix} p_{11} & p_{12} & p_{13} & p_{14} \\ p_{21} & p_{22} & p_{23} & p_{24} \\ p_{31} & p_{32} & p_{33} & p_{34} \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} = e^{A_2(\frac{T}{2} - t_d)} \bullet A$ and $\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = e^{A_2(\frac{T}{2} - t_d)} \begin{bmatrix} k_{15}V_D \\ k_{25}V_D \\ k_{35}V_D \\ k_{45}V_D \end{bmatrix}$ can be obtained using MATLAB.

Therefore, the value of voltage across C_T at the end of dead time can be found from

$$x_5(t_d) = k_{51}x_1(0) + k_{52}x_2(0) + k_{53}x_3(0) + k_{54}x_4(0) + k_{55}V_D \tag{7.25}$$

This ZVS model can be used as a design guide while using piezoelectric MEMS resonators in a resonant converter. None of the existing ZVS analysis is suitable for the MEMS resonator based converters. The equivalent electrical model of the resonator

presented is different from the traditional equivalent circuit model of a PT. A PT is a 2-port four terminal device [9]–[12], [13] similar to transformers. The existing ZVS analyses in the literature are based on this model of the PT as shown in Fig. 7.8. However, resonators are 1-port two terminal devices as indicated in Fig. 7.9a, which is similar to passive components such as capacitors, resistors, and so on.

The half-bridge AC output series resonant topology incorporating the model of the PT with transformed load is shown in Fig. 7.8. This circuit can be simplified to the circuit shown in Fig. 7.9b [13], which has only three state variables. The time domain analysis of this circuit results in homogeneous second-order differential equations, which can be analytically solved to obtain the ZVS conditions [13]. There is an extra capacitor C_P in the electrical model of the resonator, and these results in five state variables in the half-bridge AC output series resonant topology as shown in Fig. 7.9a. The ZVS model based on Fig. 7.9b having three state variables is not suitable for the converter incorporating the presented resonator. Therefore, it was necessary to propose a ZVS model based on the equivalent electrical model of the two terminal resonator.

The time-domain analysis of Fig. 7.9a involves solutions of homogeneous third-order differential equations, which is impractical. Therefore, a state space-model of the circuit has been used in this paper. In addition, a state space presentation of the converter makes the various analyses simpler to implement in MATLAB without deriving complex equations. This can be very useful in future designs of the AlN microresonator based converter.

7.2 Model Verification

The model described in the previous section has been verified using a bulk piezoceramic resonator. It is evident from the analysis that proper dead/off time must be set to achieve ZVS, which is in the range of a few nano-seconds (ns) for the fabricated device described in Chapter 6. Moreover, existing half-bridge driver ICs do not operate beyond 20 MHz. However, piezoceramic material based resonators are commercially available with resonant frequencies in the range of hundreds of kHz. For the proposed device, the piezoelectric material is deposited using sputtering or chemical vapor deposition (CVD). Fabrication is not mandatory for piezoceramic resonators, as they are commercially available.

In this paper, a resonator from Murata electronics (CSBLA400KECE-B0) has been used to validate the performance of the model with available half-bridge drivers. The electrical equivalent parameters of this resonator with reference to Fig. 5.1 are given in Table 7.1. TI's high frequency half-bridge driver IC (LM5106) has been used as the driver in the prototype. This IC has an adjustable dead time feature, which is an essential feature for this experiment. Rohm MOSFETs (RHK005N03) have been used as the half-bridge switches. The total output capacitance of the FETs was estimated to be 50 pF. Fig. 7.10 shows the 50 mW prototype of the piezoceramic resonator based AC output half-bridge series resonant converter.

In order to verify the model, $x_5(t_d)$ is subtracted from V_D in order to obtain the voltage across C_T when the high-side FET S_1 is turned ON. Normalizing this with respect to V_D, we define $\overline{V}_R(t_d)$ as

$$\bar{V}_R(t_d) = \frac{V_D - x_5(t_d)}{V_D}$$

Therefore, the ZVS condition is met if $\bar{V}_R(t_d) \geq 1$. $\bar{V}_R(t_d)$ with varying load resistance is shown in Fig. 7.11 for two different dead time intervals (e.g., 125 ns and 325 ns). The switching frequency in Fig. 7.11 is 390.6 kHz. PSIM simulation results and the model follow each other very closely in Fig. 7.11. Ideal bidirectional switches are used in the PSIM simulations, and this allows $x_5(t_d)$ going further below 0 V. Therefore, the simulation results and model predictions can be compared with each other. The three different scenarios (ZVS condition met easily, ZVS condition just met and ZVS condition not met) similar to discussion in the previous section is shown in Fig. 7.12.

However, there is a discrepancy between experimental and simulation results in Fig. 7.11. The parasitic capacitance of the PCB contributes to this mismatch. This capacitance is on the same order of magnitude of C_T and reduces $\bar{V}_R(t_d)$ in the experimental results. Harmonics introduced by the switching signal excite other vibration modes within the resonator. The standard equivalent circuit model considers the fundamental vibration mode only. Therefore, these vibration modes also contribute to lower $\bar{V}_R(t_d)$ in experimental results.

7.3 Efficiency Analysis of MEMS Resonator Based Converter

In order to perform the efficiency analysis, the circuit of Fig. 7.2 can be further simplified for a certain, f, as shown in Fig. 7.13, by transforming the parallel model of the resonator to a series equivalent:

$$R_T = \frac{1}{(\omega C_P)^2} \frac{R_S}{R_S{}^2 + (\omega L_S - \frac{1}{\omega C_S} - \frac{1}{\omega C_P})^2} \quad (7.26)$$

$$L_{ST} = \frac{1}{\omega^2 C_P} \frac{\frac{L_s}{C_P} + 2\frac{L_S}{C_s}}{R_S{}^2 + (\omega L_S - \frac{1}{\omega C_S} - \frac{1}{\omega C_P})^2} \quad (7.27)$$

$$C_{ST} = C_P \frac{R_S{}^2 + (\omega L_S - \frac{1}{\omega C_S} - \frac{1}{\omega C_P})^2}{R_S{}^2 + (\omega L_S)^2 + (\frac{1}{\omega C_S})^2 + \frac{1}{\omega^2 C_S C_P}} \quad (7.28)$$

The circuit shown in Fig. 7.13 can be used for efficiency analysis of the MEMS resonator based converter (excluding losses associated with the FETs). Considering only real power, the ratio of R_{OT} to the sum of the series resistance R_T and R_{OT} yields the efficiency of the circuit:

$$\eta = \frac{R_{OT}}{R_T + R_{OT}} \quad (7.29)$$

Maximizing R_{OT} can maximize η. The R_O (Fig. 7.1) that maximizes R_{OT} can be obtained by taking the derivate of (7.1) with respect to R_O and equating it to zero:

$$R_{O,\max} = \frac{1}{\omega C_o} \quad (7.30)$$

Substituting $R_{O,\max}$ in (7.1),

$$R_{OT,\max} = \frac{1}{2\omega C_o} \tag{7.31}$$

Therefore,

$$\eta_{\max} = \frac{1}{1 + 2\omega C_o R_T} \tag{7.32}$$

7.4 Performance Analysis of the Fabricated Device in Series Resonant Converter

The parameters of Table 6.3 can be used to evaluate the ZVS operating condition (as in section 7.1) of the AC output topology (Fig. 7.1b). For various load resistances and frequencies, it is possible to obtain a dead time t_d within the range $0 < t_d < \frac{T}{4}$ [10] that minimizes $x_5(t_d)$ in (7.25). With this t_d, a profile of the inductorless ZVS can be obtained for the MEMS resonator presented.

The parameters of Table 6.3 can be replaced in Fig. 7.1b as shown in Fig. 7.14, and the ZVS profile of the fabricated MEMS resonator-based converter can be obtained as shown in Fig. 7.15a. The operating frequencies over which inductorless ZVS is possible for a certain load can be known from this profile. As it is desirable that the converter is just below or just on the point of achieving ZVS (the same assumption was made in section 7.1), the ZVS margin is set to 0.1 V in Fig. 7.15a. Fig. 7.15b shows the peak

efficiency of the fabricated device with respect to frequency using the analysis discussed in section 7.3. The peak efficiency decreases as the operating frequency increases in Fig. 7.15b. Therefore, the minimum possible frequency of the ZVS frequency range for a certain load should be chosen as the operating frequency, and this will allow for achieving higher efficiency. The peak efficiency of Fig. 7.15b corresponds to a 50 mW converter. Reducing this power rating, much higher efficiency can be obtained.

PSIM simulations of Fig. 7.14 for operating frequency and load resistance of 87.32 MHz and 70 Ω, respectively, have been shown in section IV (Fig. 7.4–7.6) for different dead times.

The low efficiency is mainly due to the large R_S of the device. In order to show the effect of R_S on the peak efficiency, the same analysis (as discussed in section 7.3) is performed on the model of the piezoceramic resonator (from Table 7.1) and shown in Fig. 7.16. Similar to the MEMS resonator, the peak efficiency decreases as the frequency increases. However, it remains higher than 90% for a wide frequency range (388.4–395 kHz). However, this commercially available resonator cannot be integrated on Si.

As mentioned earlier, the piezoelectric transformer (PT) based converter has been reported in the literature [7], [9], [14] as lamp ballast or an LED driver. The efficiency of these converters has been compared to the estimated efficiency of the presented microresonator based converter as depicted in Table 7.2. The size of the PTs used in those works is also included in Table 7.2. As the size and volume directly influence the motional resistance of the device, the efficiency of the microresonator based converter is low compared to the existing works on PT based converters.

Recently, many low-power converters have been reported utilizing on-chip air-core

[17], [18] or copackaged microfabricated air-core/thin magnetic film core inductors [19]-[21], [22] as well as copackaged inductors on ferrite substrates [23]. These miniature (on-chip) converters may also be used as power conditioning circuits for implantable devices. Table 7.3 presents a comparison of these inductor-based converters with piezoelectric resonator-based converters. As observed from Table 7.3, the operating frequency is comparable with existing works. The efficiency is comparatively low due to the high motional resistance. Please note that the efficiency reported here is the estimated value and could be different in the actual implementation. However, the AlN resonator has a very high equivalent inductance density and does not require thick piezoelectric or metal films as the others, e.g., thick magnetic film for the core or thick copper windings. Additionally processing of the proposed resonator can be improved in order to reduce the resistance and improve efficiency. Therefore, the reported piezoelectric microresonator has clear advantages in terms of size and volume, as seen from Table 7.3. For low-power (<50 mW) biomedical applications, where size and volume, reduction can be of utmost significant, the presented device becomes a prime candidate. Superior electromagnetic interference performance is another feature of the proposed resonator-based converter. In addition, this device has the highest equivalent on chip inductance density reported in the literature for power conversion applications.

7.5 References

[1] C. Y. Lin, "Design and analysis of piezoelectric transformer converters," Ph.D. dissertation, Dept. Electr. Comput. Eng, Virginia Tech, Blacksburg, VT, 1997.

[2] T. Zaitsu *et al.*, "Piezoelectric transformer operating in thickness extensional vibration and its application to switching converter," in *Proc IEEE Power Electronics Specialists Conf.,* 1994, pp. 585–589.

[3] H. Kakedhashi *et al.*, “Electronic Ballast Using Piezoelectric Transformers for Fluorescent Lamps,” in *Proc. IEEE Power Electronics Specialists Conf.,* 1998, pp. 29–35, 1998.

[4] T. Ninomiya *et al*., “Zero-Voltage-Switching Techniques and Their Application to High Frequency Converter with Piezoelectric Transformer,’ in *Proc. IEEE Industrial Electronics Conf*., 1994, pp. 1665–1669.

[5] M.J. Prieto *et al*., “A Very Simple DC-DC Converter Using Piezoelectric Transformer,” *Proc. IEEE Power Electronics Specialists Conf*., 2001, pp. 1755–1760.

[6] R.-L. Lin, “Piezoelectric transformer characterization and application of electronic ballast,” Ph.D. dissertation, Dept. Electr. Comput. Eng., Virginia Tech., Blacksburng, VA, 2001.

[7] E. M. Baker *et al*., “Radial mode piezoelectric transformer design for fluorescent lamp ballast applications,” *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1213–1220, Sep. 2005.

[8] M. S. Rodgaard *et al*., “Forward conduction mode controlled piezoelectric transformer based PFC LED driver,” *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4841–4849, Oct. 2013.

[9] R. L. Lin *et al*., “Inductor-less piezoelectric transformer electronic ballast for linear fluorescent lamp,” in *Proc. IEEE Applied Power Electronics Conf.*, 2001, pp. 664–669.

[10] S. Bronstein and S. Ben-Yaakov, “Design considerations for achieving ZVS in a half bridge inverter that drives a piezoelectric transformer with no series inductor,” in *Proc. IEEE Applied Power Electronics Conf*., 2002, pp. 585–590.

[11] K. S. Meyer *et al*., “Parameterized analysis of zero voltage switching in resonant converters for optimal electrode layout of piezoelectric transformers,” in *Proc. IEEE Power Electronics Specialists Conf.*, 2008, pp. 2543–2548.

[12] M. Sanz *et al*., “Comparison of different alternatives to drive piezoelectric transformers,” in *Proc. IEEE Applied Power Electronics Conf.*, 2002, pp. 358–364.

[13] E. L. Horsley *et al*., “Analysis of zero voltage switching piezoelectric transformer based converters,” *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2471–2483, May 2012.

[14] Murata. (2014). *Ceramic Resonator* [Online]. Available: http://www.digikey.com.

[15] Y. Yuanmao *et al*., “A novel method for connecting multiple piezoelectric transformer converters and its circuit application,” *IEEE Trans. Power Electron.*, vol.

27, no. 4, pp. 1926–1935, Apr. 2012.

[16] V. A. Klymko et al., “Efficient preservation of discrete spectrum signals with multilayered piezoelectric transformer,” *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4382–4391, Aug. 2014.

[17] S. Kudva and R. Harjani, “Fully integrated on-chip dc-dc converter with a 450X output range,” *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1940–1951, Aug. 2011.

[18] M. Wens and M. Steyaert, “A fully integrated CMOS 800 mW four phase semiconstant on/off time step down converter,” *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 326–333, Feb. 2011.

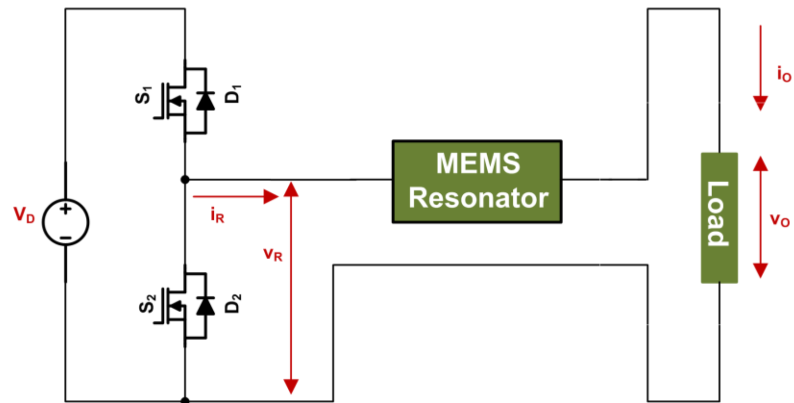
[19] P. Artillan *et al.*, “Integrated LC filter on silicon for DC-DC converter applications,” *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2319–2324, Aug. 2011.

[20] H. Jia *et al.*, “ Integration of monolithic buck converer and bondwire inductors with ferrite epoxy glob cores,” *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1627–1630, Jun. 2011.

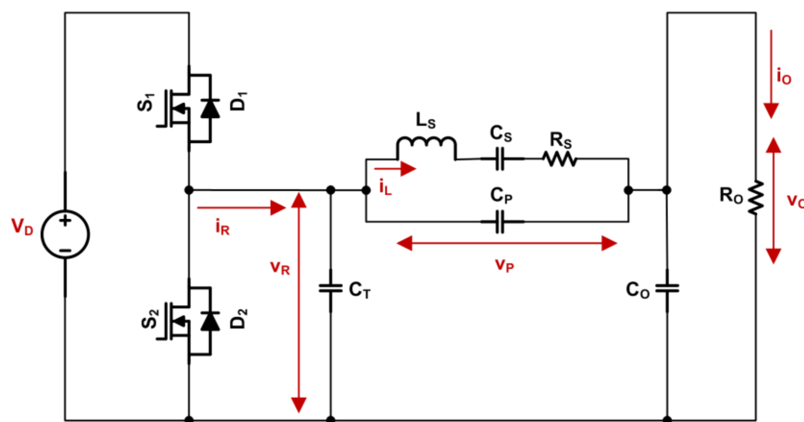
[21] R. Meere *et al.*, “Analysis of microinductor performance in a 20-100 MHZ DC/DC converter,” *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2212–2218, 2009.

[22] H. Bergveld *et al.*, “A 65 nm CMOS 100 MHz 87% efficient DC-DC down converter based on dual die system in package integration,” in *Proc. IEEE Energy Conversion Congress Expo*., 2009, pp. 3698–3705.

[23] S. Sugahara *et al.*, “90% high efficiency and 100 W/cm^3 high power density integrated DC-DC converter for cellular phones,” *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1994–2004, Apr. 2013.



(a)



(b)

Fig. 7.1: Resonator in power conversion (a) half-bridge series resonant converter replacing L-C resonant tank with MEMS microresonator on Si.
(b) microresonator replaced by the equivalent circuit model.

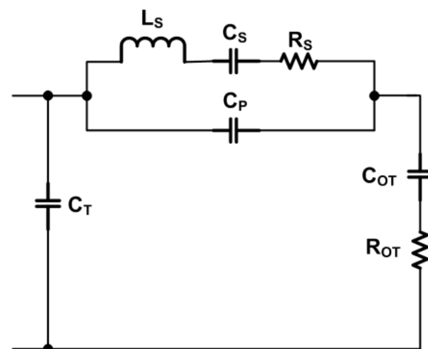
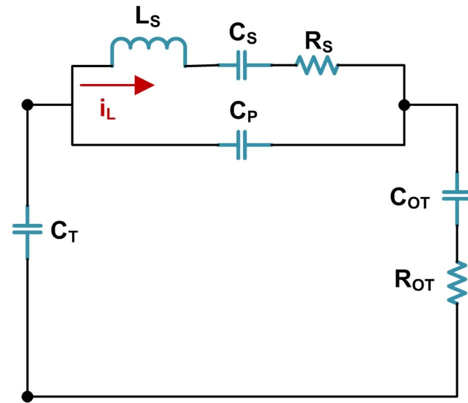
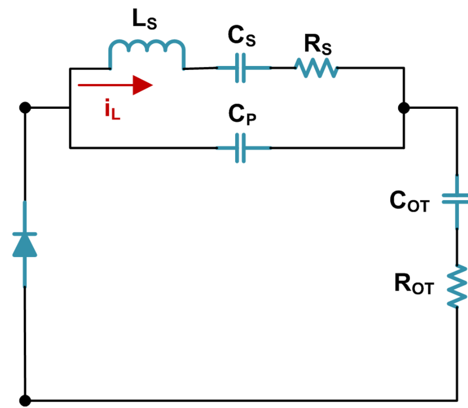


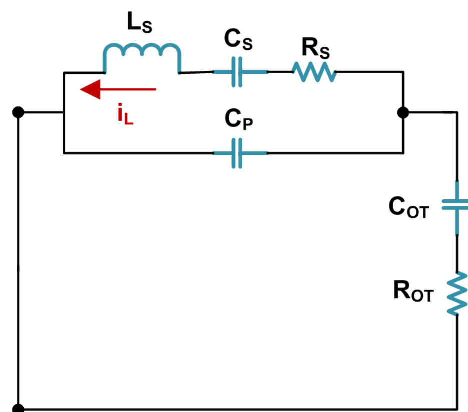
Fig. 7.2: Parallel to series load transformation of Fig. 7.1b.



(a)

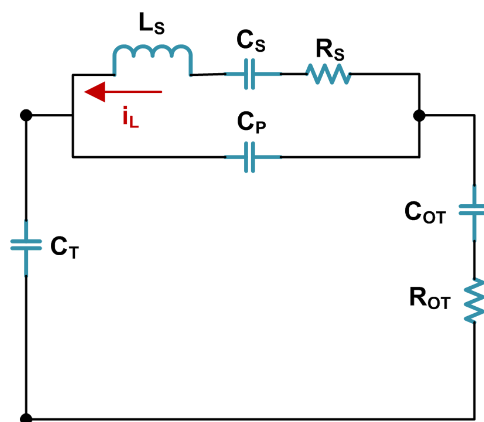


(b)

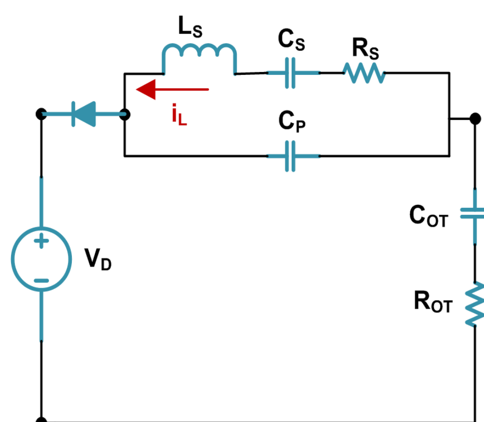


(c)

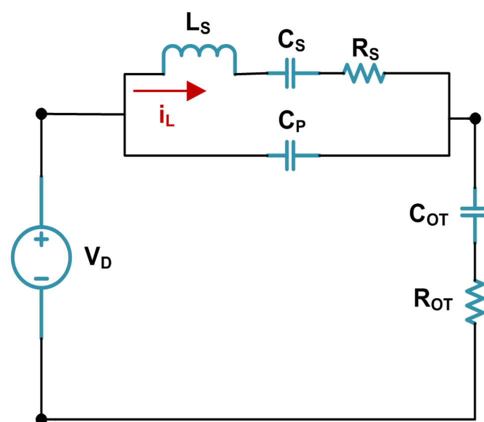
Fig. 7.3: Operating principles of MEMS resonator-based converter (a) stage 1, (b) stage 2, (c) stage 3, (d) stage 4, (e) stage 5, (f) stage 6.



(d)



(e)



(f)

Fig. 7.3: Continued

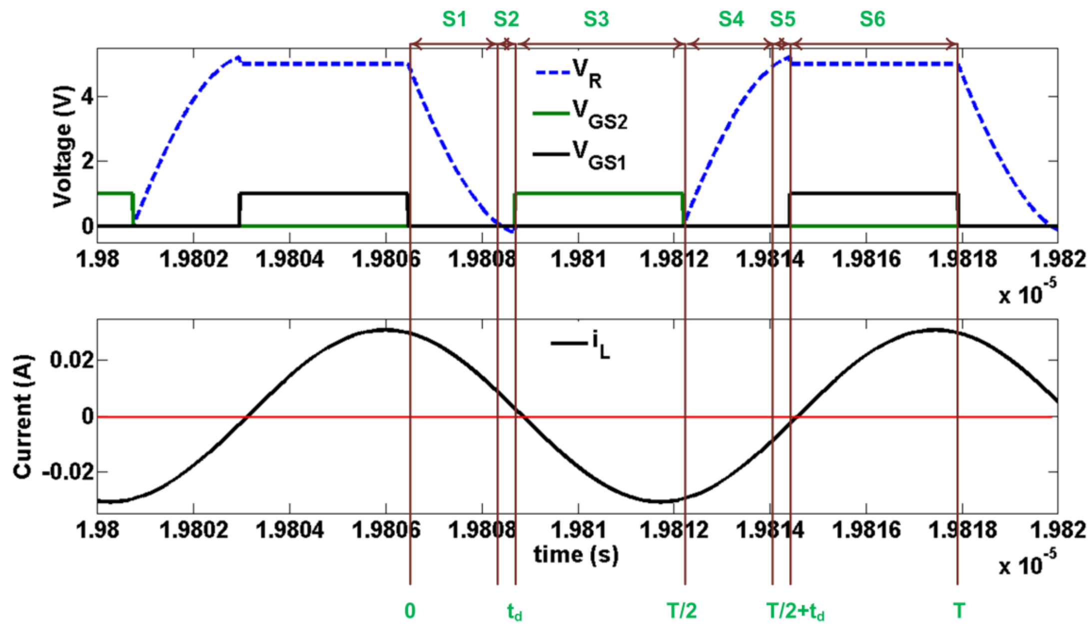


Fig. 7.4: PSIM simulation results of the MEMS resonator-based converter (Fig. 7.1b) when ZVS is achieved easily

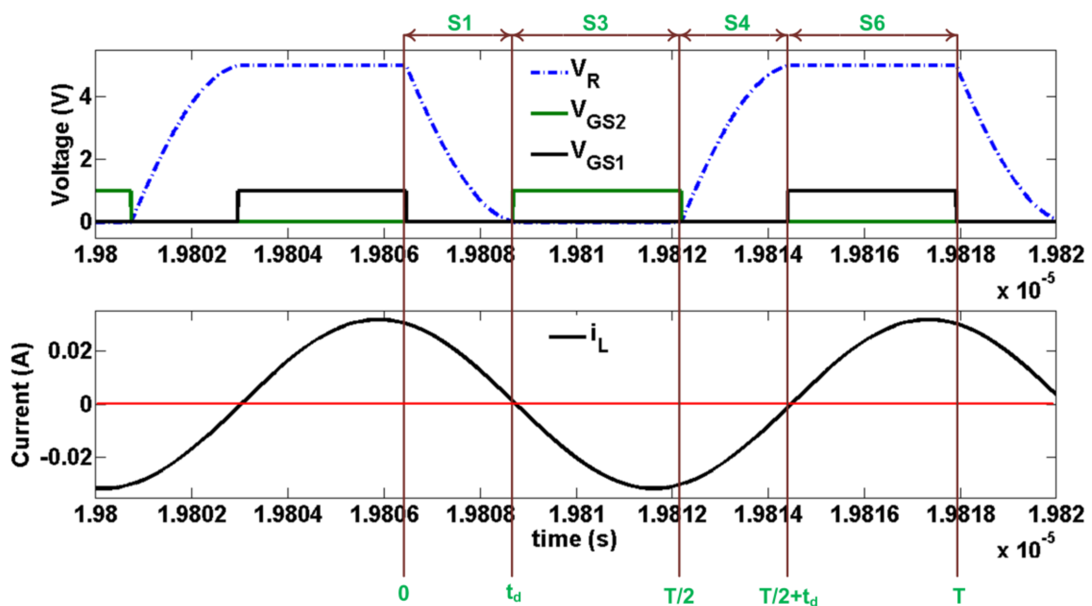


Fig. 7.5: PSIM simulation results of the MEMS resonator-based converter (Fig. 7.1b) when ZVS is just achieved (the voltage across C_T is approximately equal to 0 V at t_d).

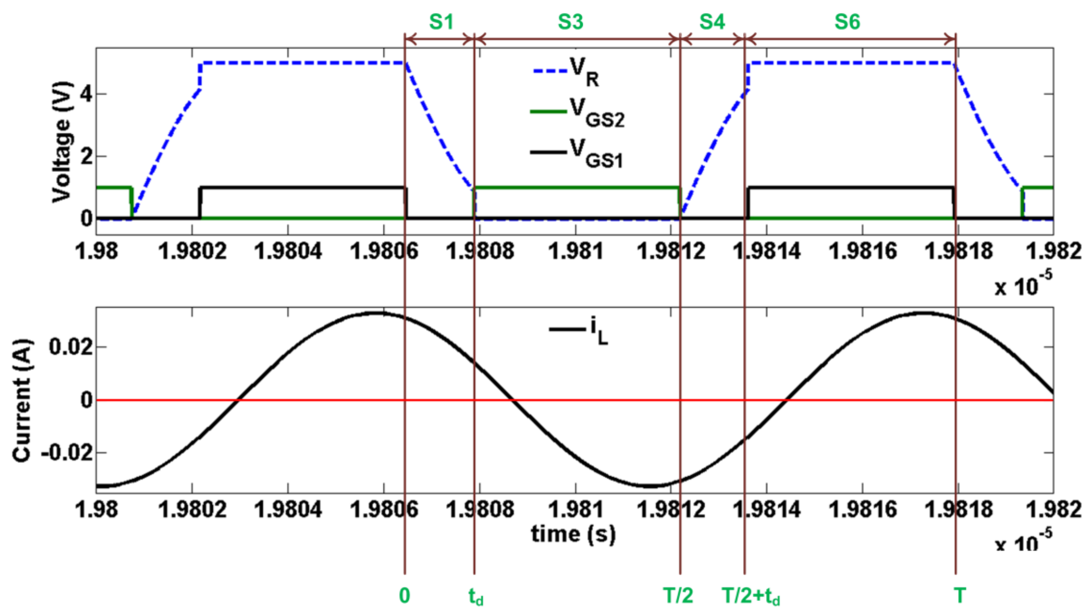
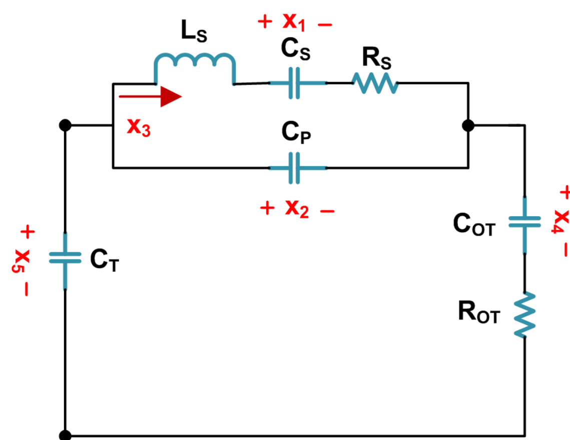
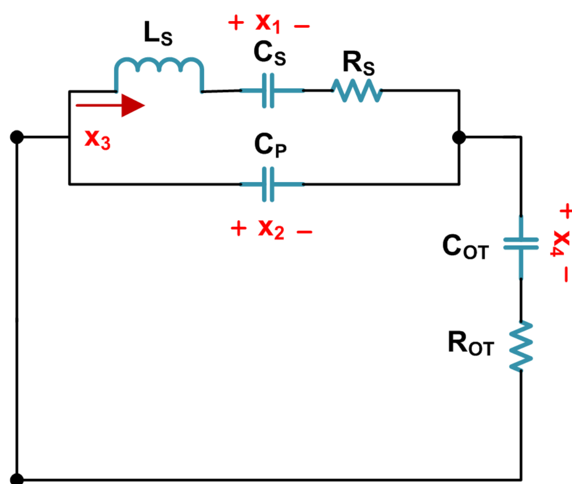


Fig. 7.6: PSIM simulation results of the MEMS resonator-based converter (Fig. 7.1b) when ZVS is not achieved (S_1 is turned on before the voltage across C_T reaches 0 V).



(a)



(b)

Fig. 7.7: State space analysis (a) stage 1 with corresponding state variables, (b) stage 3 with corresponding state variables.

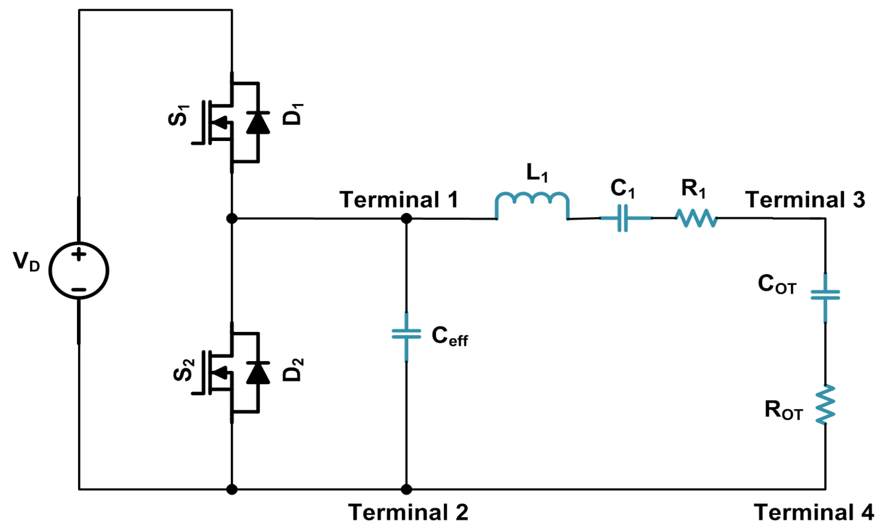
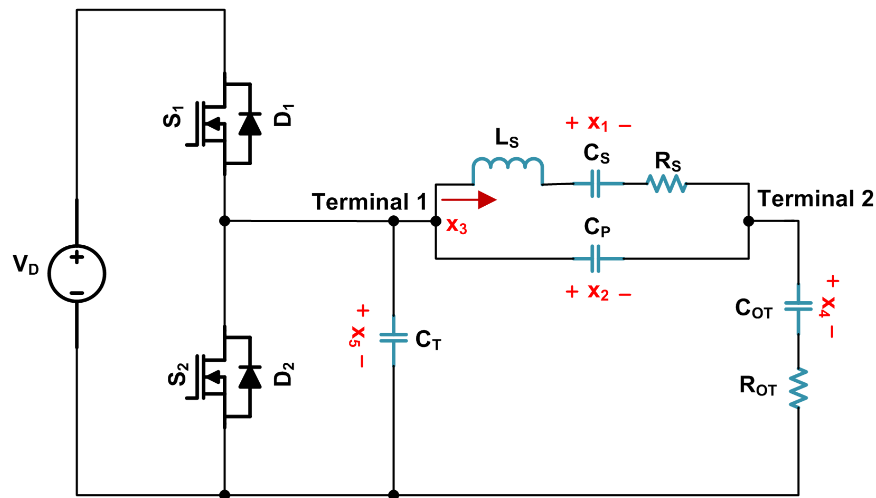
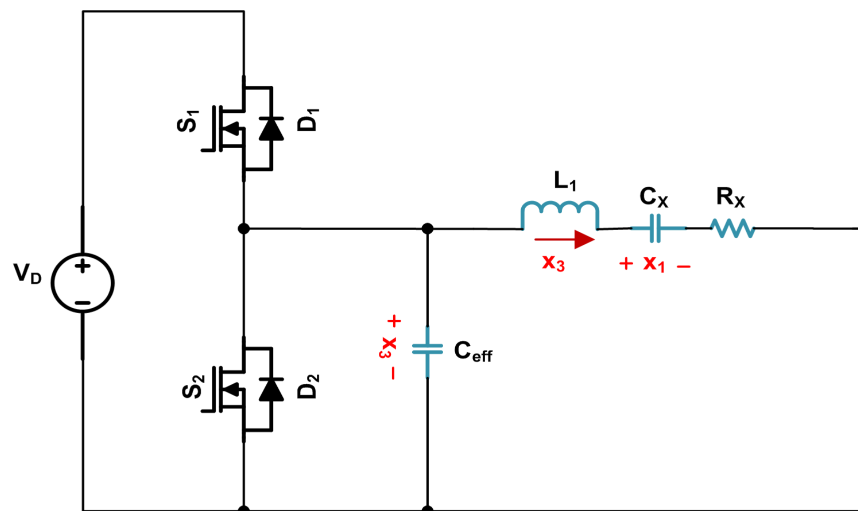


Fig. 7.8: Half-bridge AC output series resonant topology incorporating a four terminal PT with parallel to series transformed load 0.



(a)



(b)

Fig. 7.9: Comparison (a) half-bridge AC output series resonant topology incorporating a two terminal piezoelectric resonator with the state variables, (b) simplified circuit of Fig. 7.8 with the state variables.

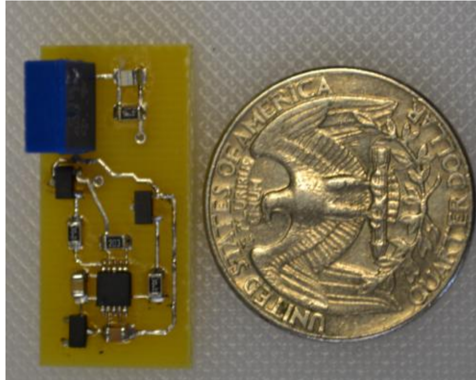


Fig. 7.10: Prototype of the 50 mW piezoceramic resonator-based series resonant converter for validating the model described in Section 7.1. The largest component is the piezocermic resonator (in blue).

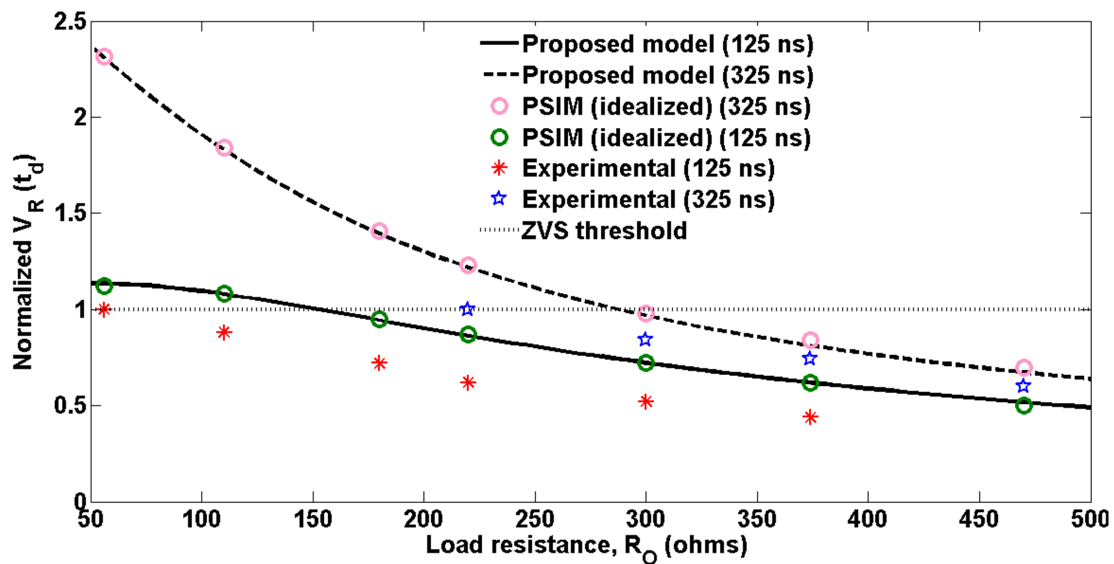
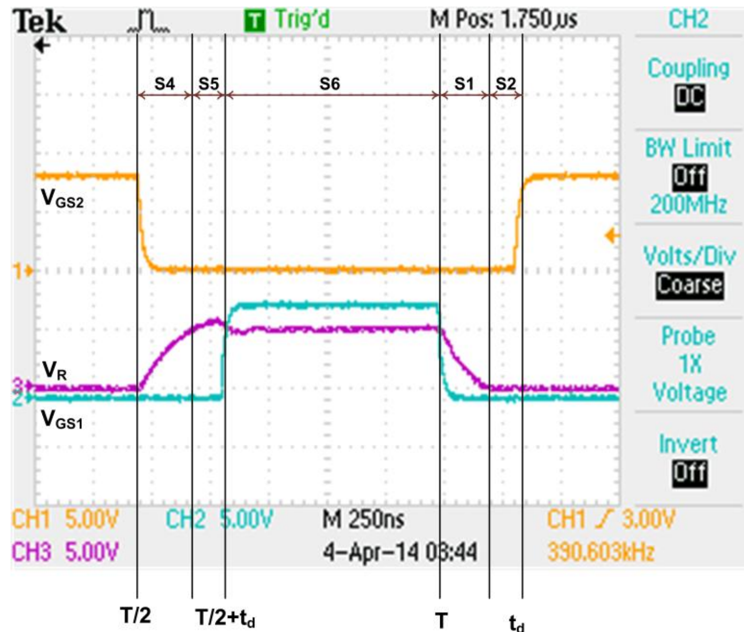
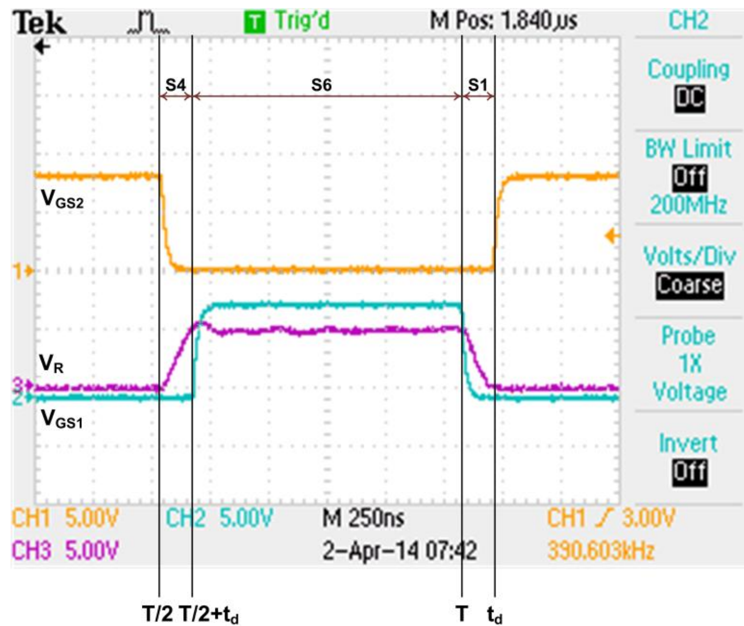


Fig. 7.11: $\overline{V}_R(t_d)$ vs. load resistance for the piezoceramic resonator-based resonant converter for two dead-time intervals (125 ns and 325 ns) with operating frequency of 390.6 kHz and DC link voltage of 5 V

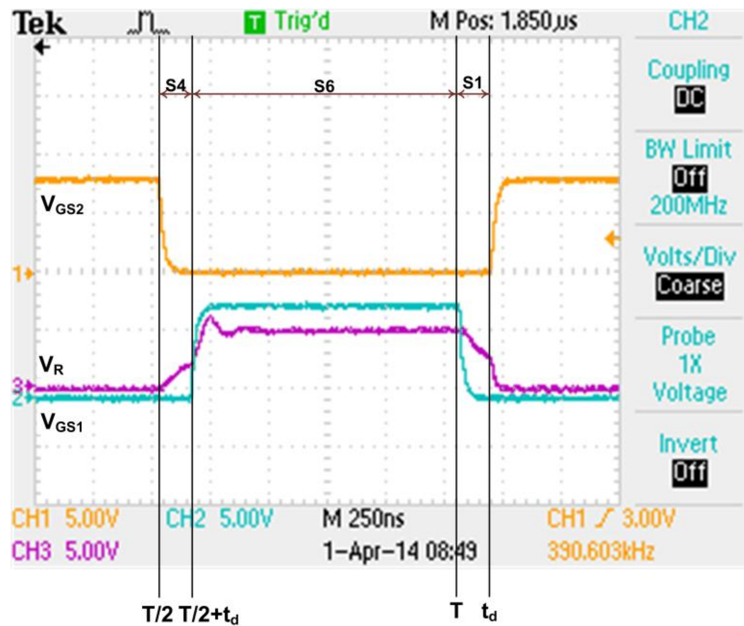


(a)



(b)

Fig. 7.12: Experimental waveforms of the piezoceramic resonator-based converter shown in Fig. 7.10, (a) ZVS condition met (similar to Fig. 7.4), (b) just on the point of achieving ZVS condition (similar to Fig. 7.5), (c) ZVS condition not met (similar to Fig. 7.6) for certain dead time intervals.



(c)

Fig. 7.12: Continued.

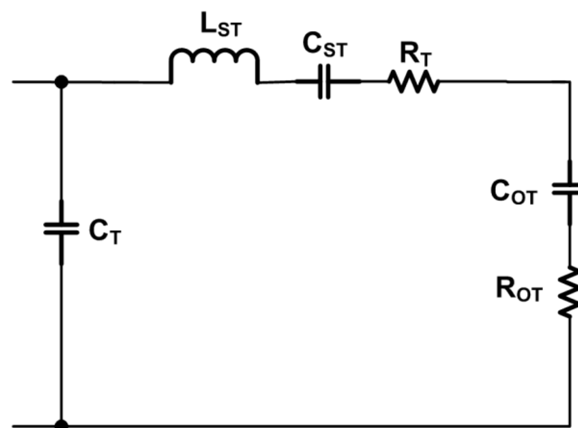


Fig. 7.13: Equivalent circuit for efficiency analysis derived from Fig. 7.2.

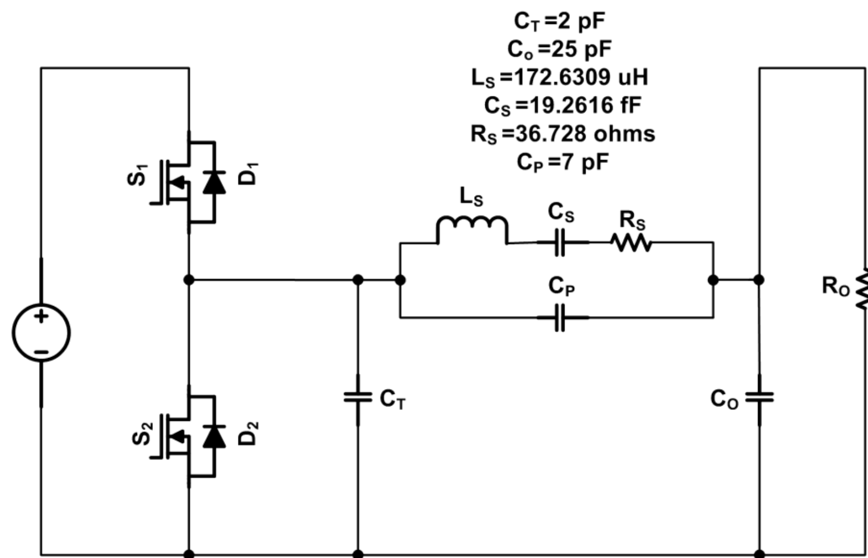
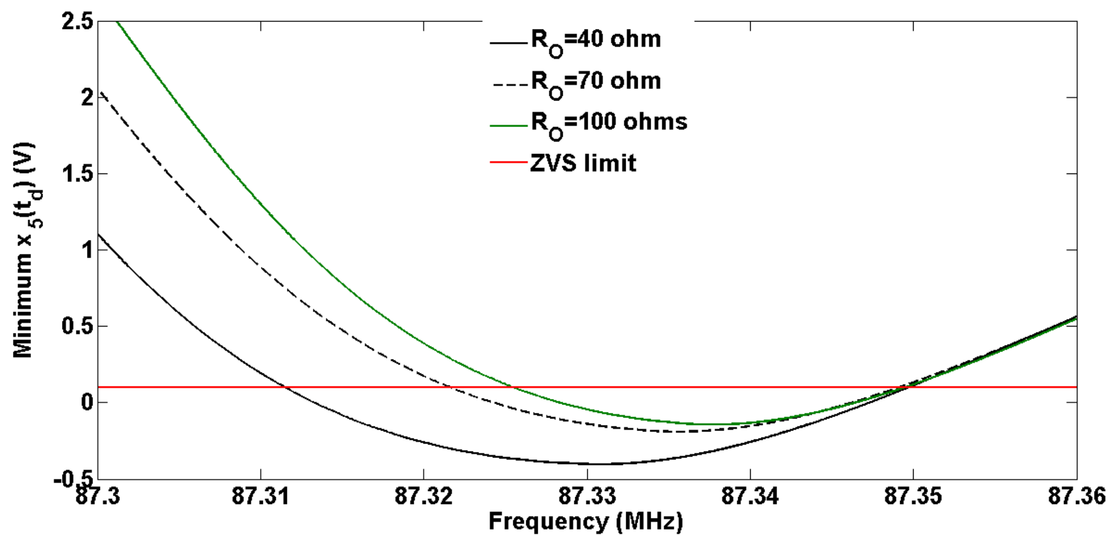
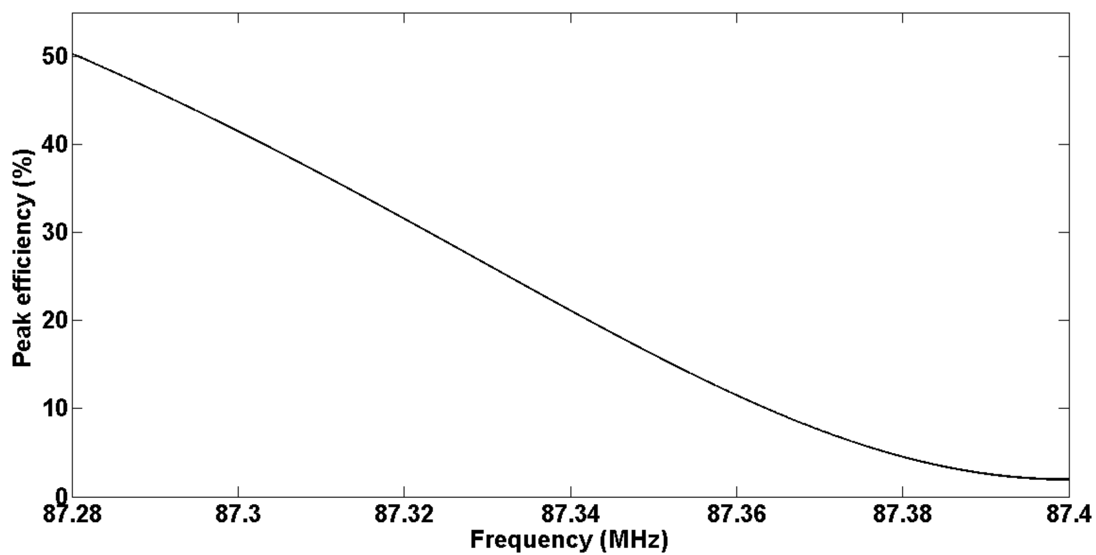


Fig. 7.14: Series resonant AC output topology used in obtaining the ZVS profile of the fabricated resonator



(a)

Fig. 7.15: Performance analysis of the fabricated MEMS resonator (a) ZVS profile using (Table 6.1). For a certain load resistance the ZVS region is under the red line. (b) peak efficiency (analysis from section 7.3) vs. frequency, obtained using the equivalent circuit parameters from Table 6.3.



(b)

Fig. 7.15: Continued.

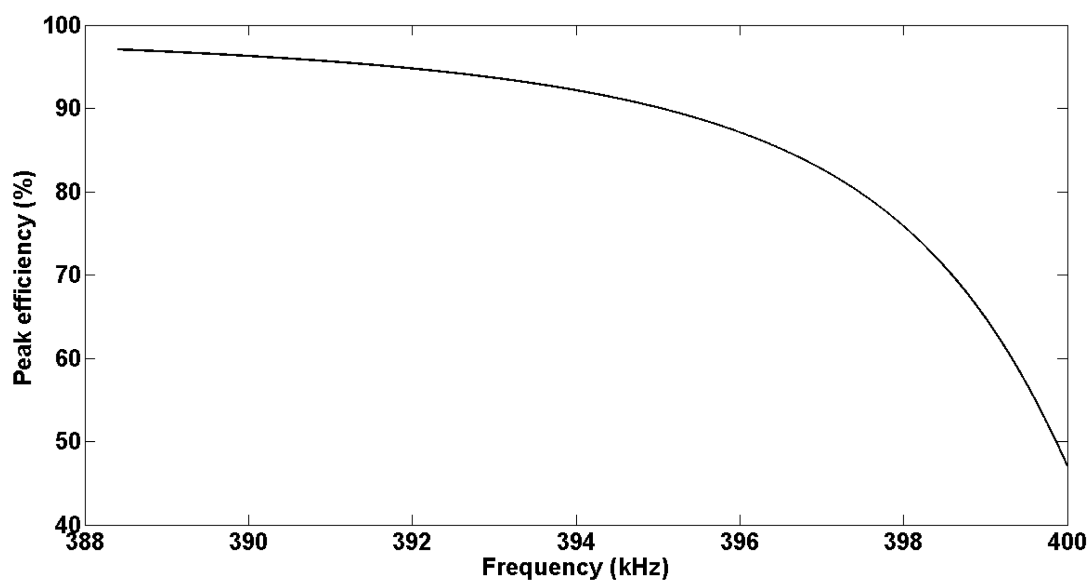


Fig. 7.16: Peak efficiency (analysis from section 7.3) vs. frequency for the piezoceramic resonator obtained using the equivalent circuit parameters from Table 7.1

Table 7.1: Equivalent electrical circuit model parameters of the piezoceramic resonator corresponding to Fig. 5.1

L_S	6.7041 mH
C_S	25.0462 pF
R_S	6.2 Ω
C_P	344.3647 pF

Table 7.2: Comparison of the PT-based converters with the microresonator-based converter in terms of efficiency and size of the piezoelectric device

	PT-based lamp ballast		PT-based LED driver		PT-based multilevel converter [14]	This work
	[7]	[9]	[32]	[16]		
Efficiency (%)	86	90	68	86	75-80	~50% (estimated)
Piezoelectric device size (mm^2)	345	705	314	216	629	0.11 (including the surrounding etched area)
Piezoelectric height (mm)	4.36	2	4	2.5	4.2	$2.4x10^{-3}$

Table 7.3: Comparison of the presented piezoelectric resonator-based converter with recently reported microinductor based converters

	On-chip air-core inductor		Copackaged microfabricated magnetic core inductor			Copackaged fabricated air core inductor	Copackaged on ferrite substrate inductor	This work
	[17]	[18]	[19]	[20]	[21]	[22]	[23]	
Operating frequency (MHz)	300	225	5	5	20-100	100	5	87.3
Inductor/ piezoelectric device size (mm^2)	0.25	2 (estimated)	9	20	7.48	1	5.76	0.11
Inductor/ piezoelectric device height (µm)	4	4	51	N/A	50	8	525	~2.5
Inductance density (nH/mm^2)	8	8 (estimated)	13	22.5	21	11	184	$1.5x10^6$
Efficiency (%)	74.5	58	45	52	78.5	87	90	~50 (estimeated)
$P_{out.\max}$(mW)	266	800	400	300	100	100	600	50 (estimated)

CHAPTER 8

CONCLUSIONS

Contour-mode piezoelectric MEMS resonators on Si with suitable characteristics (moderately low frequency and motional resistance) for implementation in a low-power converter in order to power autonomous microsystems have been described in this work. The acoustic coupling property of these devices makes them suitable for biomedical applications, and this dissertation has presented the detail processing steps to fabricate this contour mode device that has unique applications in power electronics. The feasibility of utilizing these devices in a series resonant converter has been performed through efficiency and ZVS analysis. The efficiency of the initial fabricated devices is reasonable, but could be improved by optimizing different geometries and dimensions of such MEMS resonators.

Presently, half-bridge gate driver ICs do not operate at frequencies beyond 20 MHz, much lower than the resonant frequency (87.28 MHz) of the MEMS resonator presented. As the research is in its very early stages, the ZVS model is verified experimentally using a non-MEMS piezoceramic resonator with similar characteristics to the presented MEMS resonator. As a future extension of the research, a CMOS IC incorporating series resonant converter featuring a high frequency half-bridge gate driver with a flip chip bonded MEMS resonator can be constructed.

The initial chapters of the dissertation discuss the feasibility of PV-powered autonomous microsystems by embedding the power converters on the same die of a PV cell. A CMOS compatible process has been described to integrate capacitors, MOS switches, resistors, and diodes with the PV cell. The process has been implemented and the devices have been characterized.

A study was performed to investigate the effect of light exposure on the surface electronics, and it capitalizes the embedded fabrication process to be used with the PV power system. The threshold voltage of the switches remains the same with dark and with light exposure, whereas the breakdown voltage was slightly decreased. In addition, the conductivity of the switches increased slightly due to extra carriers generated by the incident light.

The initial chapters of the dissertation mainly focus on the fabrication process to accommodate the PV cells and power converter modules on the same substrate. The most suitable circuit topology and necessary control schemes will be identified through this research in future.