Fabrication Processes and Experimental Validation of a Planar PV Power System with Monolithically Embedded Power Converters

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Abstract—**This paper summarizes the research outcome intended to identify the most suitable device architecture and its implementation for cell-level power conversion in a photovoltaic (PV) system. The fabrication process to accommodate the power conditioning unit with the PV cells using the same process run have been presented in this paper. Using this method, the entire converter can be embedded with the PV cells producing AC power directly from the solar cell strings. The initial phase of this project simulated various circuit components in the CMOS process, and the project outcome has been summarized in a previous publication by the authors. This paper presents the experimental results of the proposed process, and a simple chopper circuit has been constructed using the embedded MOSFETs and the PV cells. The circuit has been experimentally characterized, along with components. In addition to the process-related challenges and issues, this paper explains the justification of this integration by achieving higher reliability, portability and complete modular construction for PV-based energy harvesting units. To the knowledge of the authors, no attempt has been made to fabricate power converter components with PV cells in the same process run.**

I. INTRODUCTION

The widespread adoption of microelectronics worked as a motivating factor for installing millions of small-scale distributed sources. Conventional discrete electronic circuits may not be the most suitable for spreading the components over a large area in order to monitor and address the partial shading problems in a PV system. In addition, surface electronics could be used to address several major failures such as the partial shading, formation of hotspots, bypass diode failure, module cracking and arcing. Poor interconnection is a key reason for many of these failures. The use of large area electronics or Macro-electronics is a relatively recent idea, although significant work has been done to integrate the display driver circuitry on the same substrate with the display itself used in large screen TV monitors. Therefore, there exist many success stories in the literature in this regard [1]. On the other hand, power electronic components such power semiconductor switches, resistors, capacitors, inductors and other passive elements have been used in the form of discrete components on printed circuit boards (PCB) for several decades. However, the amount of work to integrate these components on the wafer level using custom fabrication processes is insignificant. Therefore integration of components in this form can significantly reduce space and weight compared to standard printed circuit board approaches.

Other than power electronics, several other research areas such as X ray imaging, solid state lighting with integrated driver circuitry, intelligent smart grid, medical application such as "sensitive skins" [2] etc require the use of planar electronics. Fabrication challenges in these areas have not been properly addressed using traditional Si CMOS micro-electronics. Several other reports have been found on the Department of Defense's (DOD) project of macro-electronics to improve the mission capability of unmanned aerial vehicles (UAVs). To address additional communication in UAV avionics, it needs to incorporate flexible plastic antennas with flexible active circuits such as low-noise amplifiers (LNAs), RF switches and digital control circuits. Some of the macro-electronics projects of NASA include solar sails (kilometer wide light membrane of solar cells) with integrated sensors for health monitoring and reshaping the sail. Therefore, it is beneficial to integrate sensors and control circuits with the membrane in order to reduce weight and achieve additional features.

II. CONVENTIONAL INTEGRATED PV MODULES

Lately, AC photovoltaic modules have been introduced with the power converter integrated at the back of the panel. [3], and the recent trend is to use the high temperature devices in the AC modules. However, the efficiency of the commercially available PV modules is still quite low (15%). Most of the losses are radiated as heat making the ambient temperature of the PV module very high (+ 70 ^{o}C). This incident puts a big hurdle to reach the ultimate goal of 25 years lifetime for the PV converters. Improving the design of heatsink and cooling mechanism can add to the reliability; however this will introduce additional cost. Some of the favorable features of the wide band gap materials such as GaN and SiC are – order of magnitude higher electrical field, and three to five times higher thermal conductivity, higher breakdown voltage, higher doping density and carrier lifetime. These properties contribute to the following reasoning: high Si – C bond strength facilitates towards higher breakdown voltage; due to high bandgap, higher temperature is needed to transfer carriers from valance to

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conduction band giving high-temperature withstanding capability. In addition, reduced carrier lifetime leads to faster switching capability [5]. However, the mass development of these devices is still limited by difficulties in crystal growth and material properties. The SiC wafers suffer from major impurities known as micro pipes. Significant amount of research was conducted to reduce the density of these defects from hundreds per cm^2 to only a few per cm^2 or even a few per wafer depending on the cost. SiC power diodes are available from Cree, Infineon for a decade.

III. Si or SiC/GaN: Choice of Materials

The efficiency and power density of the present inverters are already very high, and the reliability and cost are the major concerns. For low to medium voltage operation, devices with high breakdown voltage may not add a significant value. Slight increase in efficiency may not be attractive if the cost is very high. However, reliability at high temperature can be the decisive factor only if the SiC/GaN devices can overcome the prevalent cost issues [6]. SiC/GaN devices seem to be more suitable in renewable energy sectors or in harsh environment like in the space provided the slight increase in efficiency and high temperature operation can be justified as cost increases. For low power DC-DC converters, the scenario is almost the same as with the inverters. Other than slight increase in efficiency and power density, SiC/GaN cannot offer any other favorable features compared to those of Si devices. However, for high power/voltage DC-DC converters such as in accelerators or pulsed power converters for medical systems where a high output voltage is required, SiC/GaN devices can offer a big improvement. In addition, the recent adoption of micro/nano grid would be highly unrealistic without the high voltage, high temperature and low foot-print capability offered by the SiC/GaN devices. Therefore, it is apparent that SiC/GaN can go a long way for high power and high voltage operation even considering the higher cost.

In the embedded PV research, the converters are supposed to handle low power as well as low voltage. For low voltage applications, the higher cost incurred by the SiC or GaN devices may not be justified although other advantages are present. Moreover, the technology to fabricate defect free SiC/GaN is still not mature, and therefore, it is a natural choice to investigate the integration capability of Si devices as they use a very mature technology.

IV. Embedded Power Converter for PV Application

The idea of macro-electronics can be introduced in the design of power converters especially the ones used with renewable energy sources. A hybrid system can be designed by integrating the power converter circuit with the same wafer used to build the PV cells. Unfortunately, no significant work can be traced in the literature on this application of Macro-electronics. In this paper, experimental characteristics of different components of a typical power electronic converter fabricated with PV cells in the same process have been provided. Discussions on the challenges involved in this process are also given.

A group of PV cells connected to an integrated low power converter can address several issues with great authority. The various attractive features of this cell level power conversion would be:

- The reduction in amount of wiring, soldering.
- Reduced losses in the circuit by integrating electronics to the closer proximity of the source.
- Reduced maintenance due to reduced overall system complexity.
- Integrated electronics can provide real time information about the degradation, damage and potential catastrophic failure, most importantly partial shading phenomenon.
- Maximum power point tracking using reduced number of sensors.

V. Existing Monolithic Power Converter Solutions

The concept of an on-die power conversion unit is prevalent in microprocessors. However, the power handling capability of these converters is relatively small, and the same concept could be used in order to design relatively larger sized converters for photovoltaic applications. Although dc-dc converters have been monolithically fabricated for low-power applications, no attempts have been made to use them in the embedded fashion for PV power generation. In the CMOS process, a linear regulator (LR) could be considered as an excellent candidate because of magnetic-element-free operation. However, linear regulators suffer from an inferior efficiency profile, and these designs do not achieve dynamic voltage regulation. In order to overcome this limited efficiency barrier, switched-capacitor (SC) dc-dc converters have been proposed [7] [8]. The major limitation of many SC converters is the inability to produce the necessary variable conversion ratio (CR). Reference [9] presents an improved SC dc-dc converter with controllable CR, which was implemented using multiple pumping capacitors.

VI. Architecture of the Proposed Integration

The architecture of the proposed AC solar cell is shown in Figure 1 - the PV cells producing DC are connected to the embedded full-bridge inverters in a cascaded fashion (multi-level inverter). The voltage stress on each device will depend on the voltage of the PV cells (which is usually low); therefore, switches fabricated in low voltage CMOS process will be sufficient to withstand these voltages.

VII. Fabrication

Power converter circuits either use capacitors or inductors to transfer energy. Due to the fabrication complexity involved with inductors [10] and substantial development of on die Si-capacitors [10]-[12], SC circuits are considered to be the most suitable candidate for embedded PV power converter. Switched capacitor converters are also being used in the PV converters [13] [14] in the recent days. The feasibility of maximum power point tracking (MPPT) using switched capacitor converter is described in [13], and a low power SC DC-DC converter is used to charge a battery is presented in [14], a CMOS compatible process was proposed by the authors to fabricate converter components along with

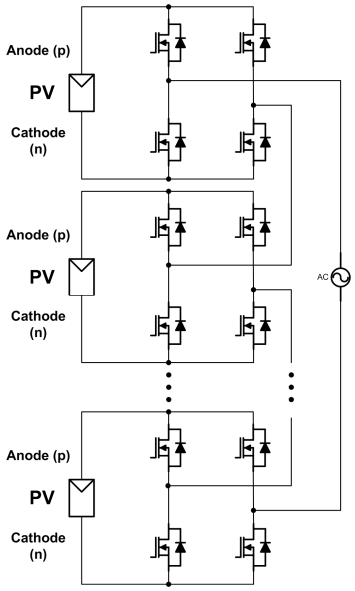


Figure 1: Architecture of the proposed integration [15]

the PV cells on the same die (Table 1). If the converter is integrated only for a few cells, converters constructed from CMOS switches could easily withstand the low voltage and current stress. Moreover, fabrication of several low power converters will not be an issue as the process is compatible with standard CMOS process, and the feasibility of the implementation of these low power converters can be found in [15]. Therefore, a multilevel architecture shown in Figure 1 seems to be the ideal choice to generate ac output, and an SC boost circuit could be used to achieve any intermediate voltage boosting.

VIII. Experimental Results/Device Characterization

TABLE 1: PROCESSING STEPS TO INTEGRATE CMOS DEVICES WITH PV CELLS

1.	Using an Oxide mask, Boron diffusion (doping density about $2x10^{17}$ cm^{-3}) through ion implantation (120 keV) is carried out to create 0.8 µm deep p-type body region (p-well) as well as anode region for PV (Figure 2a).
2.	Second oxide mask blocked the region for PV cell and opened up area for active region (Figure 2b)
3.	10 nm of gate oxide is grown thermally. 1000 nm of poly-silicon is deposited by LPCVD process. This poly-silicon layer was patterned to open areas for source and drain (third mask). The remaining poly layer act as gate as well as one electrode of the capacitor (Figure 2c)
4.	Ion implantation is carried out to form n+ source region, and n+ drain region of the MOSFET (Phosphorus doping of $1x10^{20}$ cm^{-3}, 80 keV) (Figure 2c). The poly layer also gets doped to reduce its resistivity.
5.	A 500 nm thick inter-metal oxide layer is deposited by LPCVD process. The fourth mask is used to open windows in the inter-metal dielectric film for contacts. A Ti/Al layer (0.4-0.8 µm) is deposited by sputtering. Patterning of Al (fifth lithographic step) is done to separate gate, capacitor's upper and lower electrodes, source, drain, and emitter (of solar cell).
6.	Next mask opens up the area for bond pads, and the final mask is used to pattern them. In this way, six pads are created for six terminals - gate, capacitor's upper and lower electrodes, source, drain, and emitter (of solar cell).
7.	A metal stack is deposited on the back surface to create the contact for the base of solar cell. A metal stack consists of a thin Ti film, a thin Ni barrier layer, and a thick Al layer. This stack functions as a heat sink for the entire structure also.

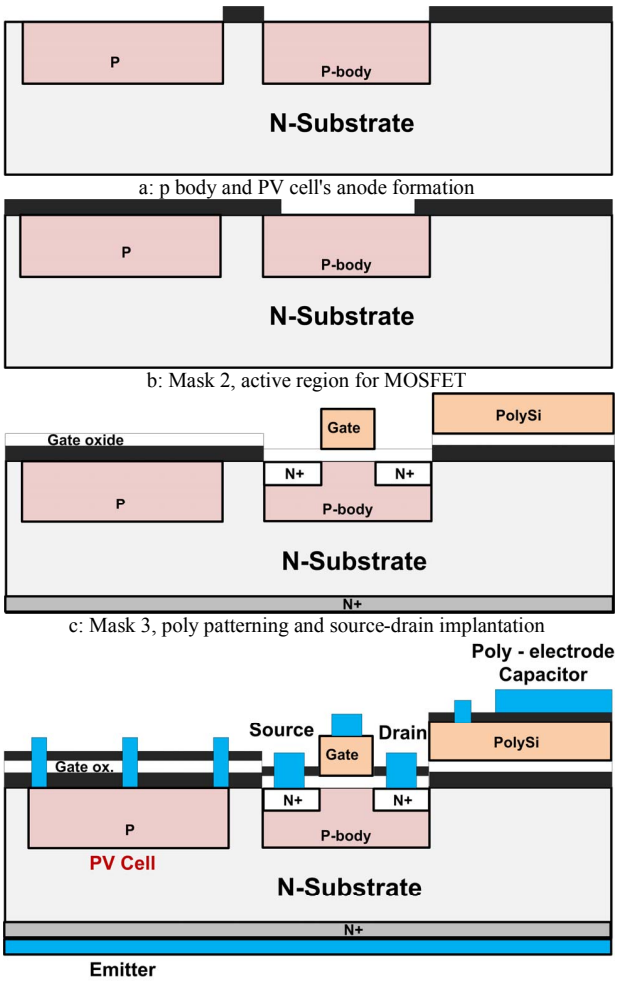


Figure 2: (a-c) Key processing steps for fabricating MOSFETs, Capacitor s with the PV cells (Cross-sections are not drawn to the scale)

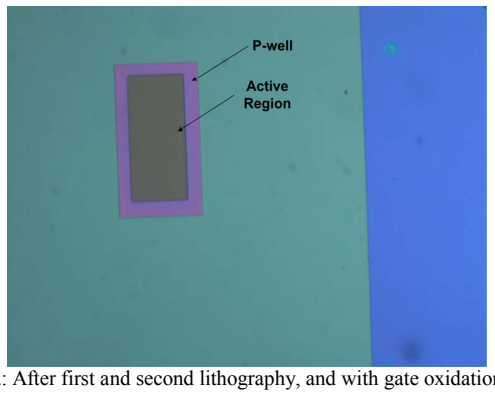
The proposed process integrating the PV cells with the converter components resembles the fabrication process of an NMOS in a CMOS process. Therefore, commercial process vendors like MOSIS or X-FAB should be the best choice to implement the proposed process. Interestingly, the process is based on creating isolated *p*-wells for PV cells and converter components, and commercial foundries do not fabricate devices built from *p*-wells. They can fabricate devices created from *n*-wells due to inherent material property of Si. In Si, electrons tend to move deeper and faster than holes. If a *p*-well is created before the *n*-doping is done, there is a possibility that the *n*-doped layer can move deeper than the *p*-well depth, shorting out *n*-doped layer with the *n*-substrate. Therefore, the purpose of creating the *p*-well will go in vain in this case. In order to avoid this phenomenon, it is a common practice to use *n*-well and *p*-substrate for CMOS process. Biasing is also a favorable feature for this structure. However, if a *p*-substrate and an *n*-well are used, the switching devices have to be PMOS, which is not viable for power circuits. Again, on *p*-substrate, NMOS devices can be fabricated without any kind of wells. However, *p* substrate is

a terminal of the PV cell, which in this case will be attached with the body of the NMOS obstructing the normal circuit operation. Therefore, *p*-well on *n*-substrate was chosen as the most suitable option for the proposed fabrication.

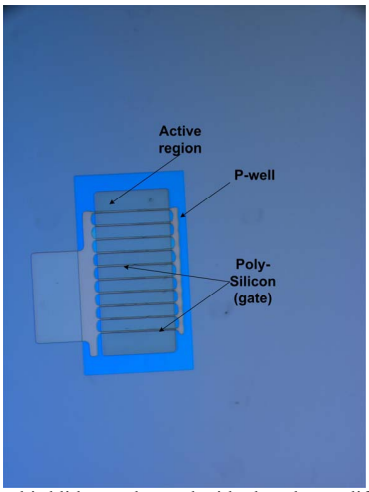
Due to the unavailability of a commercial foundry process (discussed in the previous section), the most favorable option was to develop the proposed process by the authors themselves. Authors' own institutional foundry (University of Utah's Nanofab Lab) was the best option in this regard. Because the authors were directly involved in the process development, it was possible to take microscopic pictures of the devices in different stages of the proposed process. These pictures are shown in Figure 3. Figure 4 shows the final arrangement having the converter circuit components – NMOS switch, capacitor, diode, and resistor. In the completed prototype, the presence of the switches, diodes, resistors, etc. are indistinguishable because they are very small compared to the PV cells and the capacitors. Capacitors were designed to cover a large area so that adequate capacitance can be achieved for the converter circuit. Careful inspection of the NMOS switch (Figure 3c) reveals that several parallel fingers were required to increase the current rating. The logic NMOS switches are designed to handle a small amount of current in normal operating conditions. These switches are designed to be used in a converter circuit, and they should have a certain current-draining capability without becoming excessively warm. In this case, the device temperature will not significantly rise because the current will spread through multiple fingers. Depending on the rating of the low-power converter, the current rating can be calculated, hence the required number of fingers. Even though these switches can be designed to carry decent current, the process is still a low-voltage process (the breakdown voltage of the switches is smaller than 10 V). Therefore, the number of fingers should be increased as much as possible to reduce the thermal stress, although this action will not significantly increase gate capacitance (high gate capacitance increases gate drivers' complexity) because of the use of this low voltage process.

Figure 5 shows various device characteristics (experimental) fabricated in the proposed process. The fabricated diode showed no leakage current and the forward voltage was approximately 0.7 V (Figure 5a). The University of Utah's Nanofab lab is not a semiconductor quality foundry. Therefore, the furnaces used for oxidation, diffusion, drive-in, and annealing had a good amount of metal contamination. Oxide contamination was a very big challenge during early days of transistors, and this is why bipolar switches (BJT) were the first practical transistors because of their low sensitivity to oxide contamination. As the semiconductor foundry was able to grow good quality oxide, the MOS devices became prevalent.

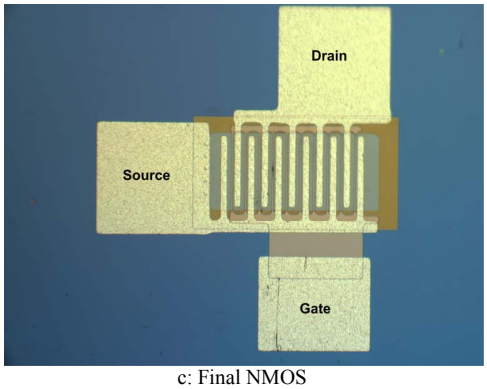
In order to reduce the effect of oxide non-uniformity, thicker gate oxide (about 100 nm) was used in the fabrication. This is why the integrated NMOS had a very high threshold voltage, approximately 45 V (Figure 5b). The breakdown/blocking voltage of the MOS switch was approximately 6 V which can be seen in Figure 5c (low voltage process). Finally, the I-V characteristics of the first MOS switch fabricated in the same process with PV cells are



a: After first and second lithography, and with gate oxidation



b: After third lithography, and with phosphorus diffusion



c: Final NMOS

Figure 3: (a-c) Microscopic snapshot of the NMOS switch in different steps of the process.

shown in Figure 5d, and the PV cell characteristics are shown in Figure 6.

The fill factor (FF) of the fabricated cells was found to be approximately 60% while conducting the experiment. The PV cell characteristics at high light intensity showed less FF due to the set up used for this measurement (Figure 7). The PV cells were placed on top of an aluminum foil; therefore, the probe made contact with the bottom of the cell via the aluminum foil. The high current generated at this high illumination had to pass through the thin probes used for measuring the I/V characteristics. This combination increased the series resistance compared to the value found with less illumination. Therefore, this higher series resistance

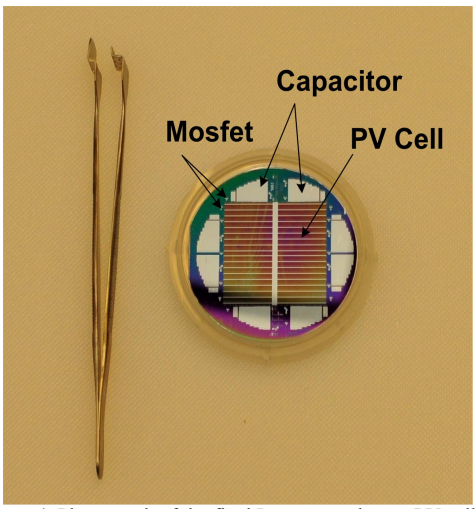


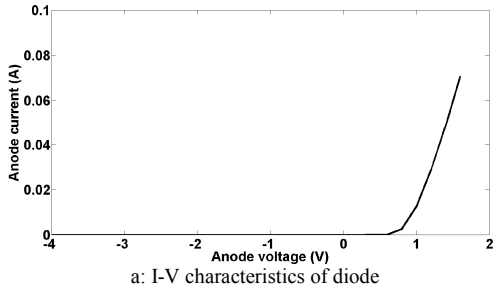
Figure 4: Photograph of the final Prototype where a PV cell is fabricated in the same process with MOS switches and capacitors.

contributed to the low FF at high illumination, which will not be a significant factor in reality because thicker wires will be used for interconnections.

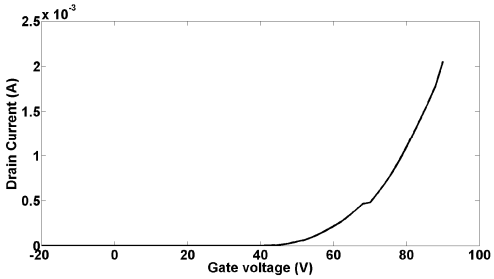
The next challenge was to construct a practical converter circuit using these devices. In order to prove the same wafer/die concept, a very simple chopper circuit shown in Figure 8 was implemented. Various devices used in this circuit were characterized using a Keithley 4200-SCS semiconductor characterization system. However, an appropriate circuit packaging is essential prior to building this converter. The choice of appropriate packaging was limited, because the switches were on the same wafer as the PV cells making the size of the entire device larger than available semiconductor packages. In addition, the back contact is an integral part of the solar cell, and the proposed integration needed a connection between the back contact and an available pin in the package. As an initial solution, the entire wafer was attached to a center drilled PCB using conductive adhesives. MEI wedge wire-bonding was used to create the connection between the bond-pads of the switches and pads on the PCB for external connections. A positive gate pulse activates the NMOS, and the switches V_{DS} drop was about 25 mV due to the finite on resistance of the MOSFET. A low gate signal deactivated the MOSFET, and the open circuit voltage becomes irradiation dependent, which in this case was 260 mV (Figure 9). The operation of this circuit indicates that the MOS switches properly function even they are exposed to illumination. This observation thus concludes that surface electronics may be viable to fabricate the entire converter on the same wafer/substrate having the PV cells. Authors are working on making an H-bridge inverter on PV cell wafer at the present time using the processes described previously.

IX. Challenges of the Proposed Integration

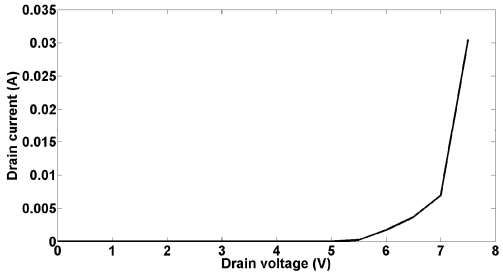
There exist numerous technological challenges in this integration. The biggest issue is the cost. The process proposed in this paper is based on Si, and the present research trend in PV is to avoid Si in order to optimize the material cost. The cost of fabrication process is also a big hurdle for an embedded PV power converter. Present commercial PV



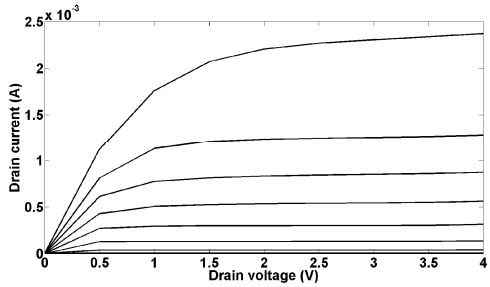
a: I-V characteristics of diode



b: Threshold voltage characteristics of NMOS



c: Break-down voltage characteristics of NMOS



d:I-V characteristics of NMOS

Figure 5: Experimental characteristics of diode and NMOS switch fabricated on the same die/substrate of a PV cell

manufacturers do not use any lithography. However, integration of electronics is not possible without lithography as precision is a key for micro-electronics. The screen-printing technology can be applied here; however, screen-printing introduces a good amount of series resistance, which will degrade the performance of the circuits. Again, CMOS compatible fabrication processes do not offer significant capacitance and sufficient capacitance is necessary even for low-power converters. Very high switching frequency can compensate this, at the cost of higher switching loss. Therefore, optimization will be required to implement the proposed concept.

Ambient high temperature of the solar cells can be detrimental to the integrated circuits. However, the low power converters employed in this integration will cause low

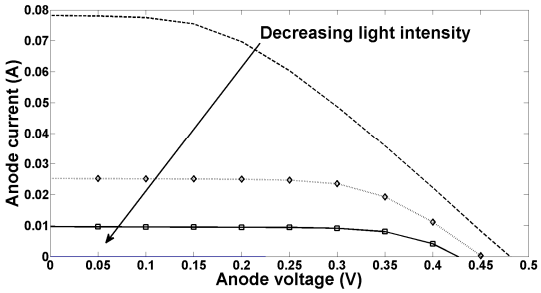


Figure 6: Experimental I-V characteristics of the PV cell.

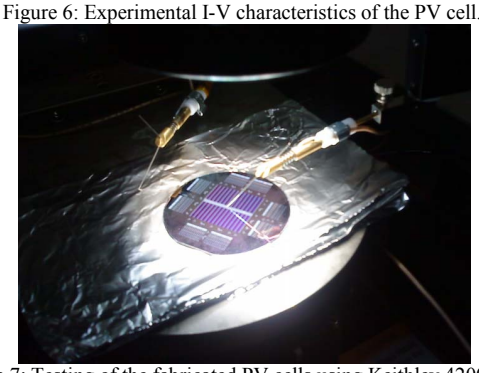


Figure 7: Testing of the fabricated PV cells using Keithley 4200 SCS.

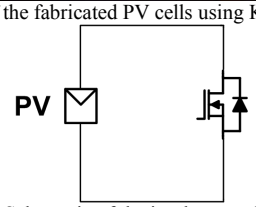


Figure 8: Schematic of the implemented circuit.

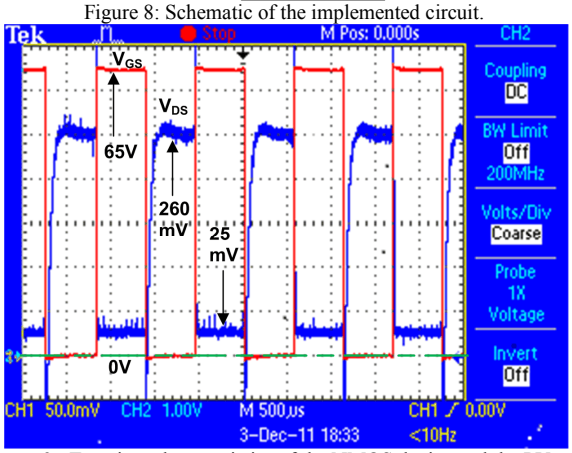


Figure 9: Transient characteristics of the NMOS device and the PV cell located on the same substrate (V_{GS} and V_{DS} are not on the same scale).

current to flow through the transistors; therefore, heat generated by the electronics themselves will be lower compared to that of conventional AC module inverters. Reference [16] shows the temperature of the module around the year using data recorded in various places of the USA. According to the results presented in that article, the PV module temperature is less than 60°C for 95% of the operating hours and less than 70°C for 99% of the operating hours. Most of the commercially available transistors are designed to perform in the temperature range higher than that. As long as the device's own generated heat lies within a safe range, the high ambient temperature should not be a reason for circuit failure. In the conventional module-integrated inverters, the transistors become warm because of high power conversion, the PV module's ambient temperature may become higher than 80°C, and this elevated temperature is primarily responsible for reduced lifespan of the converters. Again, the electrolytic capacitors are vulnerable to high-temperature situations compared to other electronics, due to the materials and the construction of the electrolytic capacitors. Si capacitors of the embedded power converter should have the high reliability same as the capacitors used in micro-processors, which will come with a high initial cost. Therefore, the reliability issue related to high ambient temperature is supposed to be less critical in the embedded converter because of the inclusion of Si capacitors and low-power converters.

X. Features of the Proposed Integration

For the conventional central inverter scheme, several modules are connected in series. Shading caused by the dirt, debris, or even a small amount of shade from tree branches or a chimney can significantly reduce the energy-harvesting because this shading limits the energy produced from the other un-shaded modules as well. The AC module addresses the partial shading phenomenon in module level. Therefore, the shading problem of one module does not affect the others. Present best estimates show that, an AC module can increase the energy yield of 12% compared to that of the central inverter scheme [17]. On a single module, a large number of cells are series-connected, and shading one of these cells can reduce the energy harvesting of all the series-connected cells. If several small power converters are used instead of one power converter for a module, the partial shading phenomenon can be addressed more conveniently, harvesting more power than one AC module. Several (10-20 converters for a 200 Wp module) converters will only be practical, if those are fabricated with the PV cells in an embedded fashion.

Another advantage of cell-level converters is the enhancement of module efficiency. In general, the module level efficiency is much smaller than the cell-level efficiency because of the mismatch of cells in a module. Presently, there is no available technique that can address this inherited fabrication phenomenon. However, cell-level converters can address this issue in the same way the AC module addresses the module level mismatch incurred in the central inverter configuration. Using an embedded converter, cell mismatch phenomenon can be addressed by increasing the module efficiency close to the cell efficiency.

XI. Conclusions and Future Work

In this paper, features and challenges involved with the embedded power converters for solar cells have been discussed. Experimental characteristics of different power electronic converter components and a simple circuit on the same Si substrate/wafer of a PV cell has been provided in this paper. A CMOS compatible fabrication process has been proposed to implement this idea for the first time. Cell level power processing will be able to address the issues of partial shading more appropriately, therefore, enhancing the energy harvesting capability of each cell. Moreover, the higher system reliability can be achieved because all the components

will be fabricated on the same Si substrate. Developing a new process is a long-term work, and due to early nature of this research, only a chopper circuit has been fabricated until today. At this time the control signal will be provided externally, which in future will be integrated with the rest of the power processing unit. This paper mainly focuses on the fabrication process to accommodate the PV cells and power converter modules on the same substrate. The most suitable circuit topology and necessary control schemes yet to be identified through this research. Authors strongly believe that using the proposed process, the power converter circuits and necessary control circuits can be embedded, and required research plans to achieve this target are in place.

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