Analog Decoding of Product Codes

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Abstract — **A method is presented for analog soft-decision decoding of block product codes (block turbo codes). Extrinsic information is exchanged as analog signals between component row and column decoders. The component MAP decoders use low-power analog computation in subthreshold CMOS circuits to implement the sum-product algorithm. An example decoder design is presented for a $(16,11)^2$ Hamming code.**

Several authors have proposed analog circuits for soft decoding [1,2], and have produced designs which apply the concept to simple codes [3,4]. Suggestions have also been made to extend analog decoding to larger turbo-style codes. We propose to apply the analog approach to block product codes. Analog decoder designs for block codes are well established, and can be used as component decoders in larger designs.

As described in [5], a block product code has a two-dimensional structure. Information is encoded in rows and columns, creating sets of row and column parity checks, and a block of checks-on-checks. Soft-in/soft-out component decoders can be used to decode the rows and columns individually. Extrinsic information produced by the row decoders is forwarded to the column decoders, and so on, producing an iterative decoding arrangement.

An alternative algorithm is derived from the product code's factor graph. Each bit is shared between a row code and a column code. The two component factor graphs may be joined by an "equal node," which indicates equality among its edges, as shown in Figure 1. The entire structure is then decoded by message passing under the sum-product algorithm [6]. The node labeled 'y' in Figure 1 is a channel observation, 'u' is the coded bit (a place-holder in this graph), and 'c' represents the channel model.

Existing analog decoder designs are easily connected through a circuit implementation of the equal node. Figure 2 presents an example current-mode subthreshold CMOS design for an equal node based on the methodology of [1]. This circuit can be used to interconnect other current-mode sum-product circuits. Implementations of equal-node and other basic sum-product analog cicuits are detailed in [7].

A complete product decoder circuit is built from an array of component row and column decoders with an equal node circuit at each bit position. Because the equal-node connections are all local, the resulting circuit layouts are regular and compact. An example design for a $(16,11)^2$ Hamming decoder has about 51,000 transistors and has a simulated power consumption of 1mW, at a throughput of 1Mbit/s.

In addition to their simple decoder structure, product codes have a well understood code structure compared to other turbo-style codes. This allows use of importance sampling techniques [8] for circuit performance verification. Under importance sampling, it becomes feasible to include more accurate analog circuit models in decoder simulations.

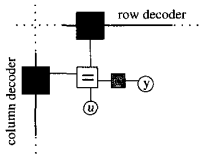

Fig. 1: Component factor graphs are connected via an equal node.

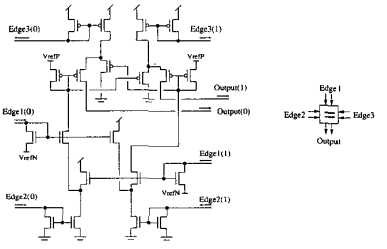

Fig. 2: Circuit for equal node implementation

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