The Path Programmable Logic (PPL) User's Manual

by

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ABSTRACT

This manual describes the primitive NMOS Path Programmable Logic cells currently in use at the University of Utah. It contains detailed descriptions, schematics and composite layouts of all cells. Also included are PPL programming rules as well as the layout design rules for each cell set.

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List of Figures

GENERAL PATH-PROGRAMMABLE LOGIC THEORY

1. GENERAL PATH-PROGRAMMABLE LOGIC THEORY

Path-Programmable Logic (PPL) is a descendant of the Storage/Logic Array (SLA). The basic theory of Path-Programmable Logic is very similar and is treated in great detail in Smith's PhD thesis.

The theory of the PPL cell set is very similar to the theory of standard PLA circuits. In the PPL, however, the AND and OR planes are superimposed one on top of the other. By doing this the space required to implement a circuit can be reduced by about a factor of two compared with the standard PLA implementation. The purpose of this cell set is to allow a designer to design a circuit at a logical level instead of at the transistor level. By using this level of design the time required to design an IC can be reduced greatly while the size of the circuit is increased only slightly. For the purposes of this manual, only the operation of the NMOS PPL will be described.

- AND PLANE -The AND plane is composed of rows which become 'true' when they sense the AND condition of a combination of signals on a set of columns, thereby allowing the row to go high. The function of the cells making up the AND plane will be described later.

- OR PLANE -The OR plane is composed of columns which contain two wires (left and right). When a wire is pulled low then the wire is 'true'. For normal usage the left wire in the column is used as the '0' wire and the right wire is used as the "1" wire. An OR condition is formed on a column wire when a true row pulls the column wire low.

  Normally the '1' wire is pulled low. A '01' inverter can then be used on the column to generate the complement of the OR condition. In this way, either the OR condition or its complement can be detected by a row. Without an explicit connection being made between the 2 column wires through the use of an inverter, pass transistor, or ohmic contact the column wires are independent of one another.

The cells are divided into six major categories:

1. PRIMITIVE ROW CELLS - These include the cells that occupy a single row cell, the smallest increment of space available in the PPL array. These include the simple combinational elements and ohmic contacts.

2. COMPLEX ROW CELLS - This category is made up from the storage elements (latches and flip flops) and the pass transistors. These cells all take up more than one row cell location.

3. PULL-UP CELLS - These include three sizes of column pull-ups and one row pull-up. They are used as loads on the row and column wires.

GENERAL PATH-PROGRAMMABLE LOGIC THEORY

4. INTERCONNECT CELLS - In this cell set, the row and column interconnects are placed BETWEEN the cells. In addition to these interconnect cells this also includes the row and column break cells that are used for graphical purposes in the circuit design on the CV machine.

5. BUSSING CELLS - These are cells that must be placed around the perimeter of the active PPL area to distribute power, ground and the clocks to the PPL array.

6. PAD CELLS - Which include input-protection, output-protection, Vdd, GND, input, and output pads. All of the pad cells contain a portion of the scribe lane which goes around the perimeter of the chip.

2. QUICK REFERENCES

This chapter is designed to be used as a quick reference for general PPL design. It contains no detailed information about the cells. For more information about each cell see the individual chapters. The cells which have internal pull-ups have an asterisk (*) inside the graphics.

Cell : 0 / #

Row(s) : 1

Column(s) : 1

Cell : 1 / #

Row(s) : 1

Column(s) : 1

Cell : S / #

Row(s) : 1

Column(s) : 1

Cell : S2 / #

Row(s) : 1

Column(s) : 1

Cell : R / #

Row(s) : 1

Column(s) : 1

Cell : R2 / #

Row(s) : 1

Column(s) : 1

QUICK REFERENCES

Cell : PLUS / #

Row(s) : 1

Column(s) : 1

Cell : BLK / #

Row(s) : 1

Column(s) : 1

Cell : OCL / #

Row(s) : 1

Column(s) : 1

Cell : OCR / #

Row(s) : 1

Column(s) : 1

Cell : OCB / #

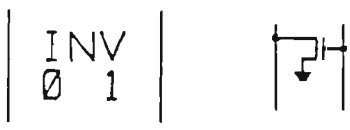
Row(s) : 1

Column(s) : 1

Cell : INV01 / #

Row(s) : 1

Column(s) : 1

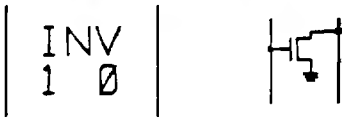


QUICK REFERENCES

Cell : INV10 / #

Row(s) : 1

Column(s) : 1



Cell : SICUINV / #

Row(s) : 3

Column(s) : 1

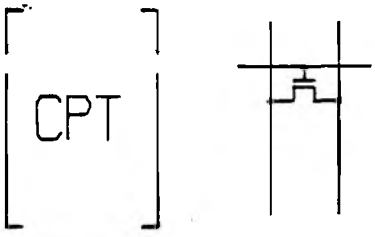
Placement - Row: Even

Cell : CPT / #

Row(s) : 2

Column(s) : 1

Placement - Row: Even

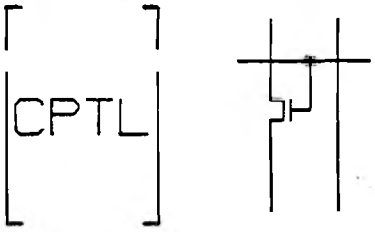


Cell : CPTL / #

Row(s) : 2

Column(s) : 1

Placement - Row: Odd



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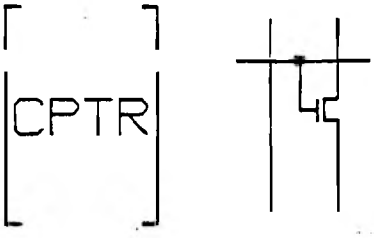
Column(s) : 1

Placement - Row: Odd

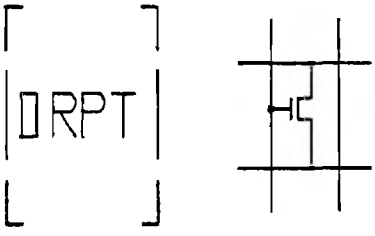


Cell : RPT1 / #

Row(s) : 2

Column(s) : 1

Placement - Row: Even



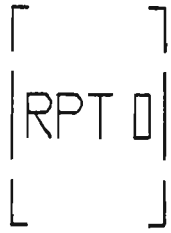
QUICK REFERENCES

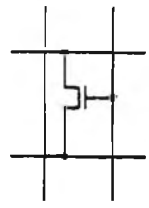
Cell : RPT2 / #

Row(s) : 2

Column(s) : 1

Placement - Row: Even





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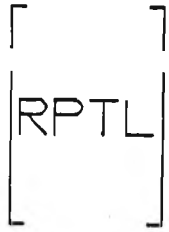
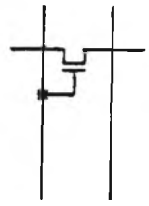
Row(s) : 2

Column(s) : 1

Placement - Row: Even



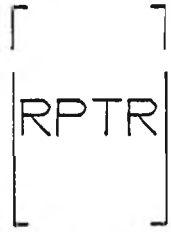


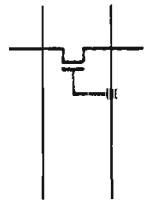
Cell : RPTR / #

Row(s) : 2

Column(s) : 1

Placement - Row: Even





Cell : LATCH2 / #

Row(s) : 3

Column(s) : 1

Placement - Row: Even

Cell : LATCH / #

Row(s) : 3

Column(s) : 2

Placement - Row: Even

Column: Odd

QUICK REFERENCES

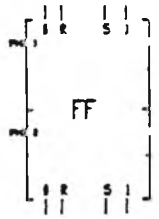
Cell : FF / #

Row(s) : 4

Column(s) : 2

Placement - Row: Even

Column: Odd



Cell : FFC / #

Row(s) : 5

Column(s) : 2

Placement - Row: Odd

Column: Odd

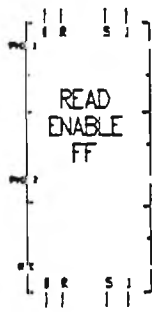
Cell : FFR / #

Row(s) : 6

Column(s) : 2

Placement - Row: Even

Column: Odd



Cell : FFW / #

Row(s) : 5

Column(s) : 2

Placement - Row: Even

Column: Odd

QUICK REFERENCES

Cell : FFRW / #

Row(s) : 7

Column(s) : 2

Placement - Row: Odd

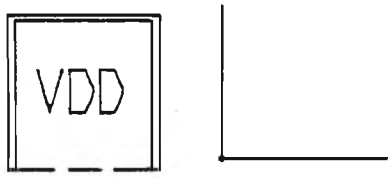
Column: Odd

Cell : VBUS / #

Row(s) : 1

Column(s) : 1

Placement - Row: Even

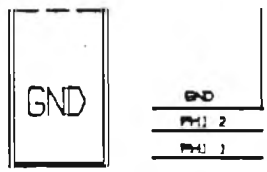


Cell : GBUS / #

Row(s) : 2

Column(s) : 1

Placement - Row: Odd

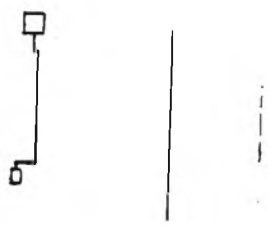


Cell : VJR / #

Row(s) : 1

Column(s) : 1

Placement - Row: Even



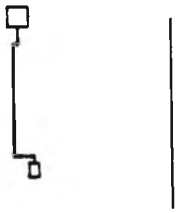
QUICK REFERENCES

Cell : VJL / #

Row(s) : 1

Column(s) : 1

Placement - Row: Even

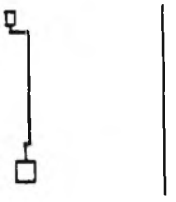


Cell : GJR / #

Row(s) : 2

Column(s) : 1

Placement - Row: Odd

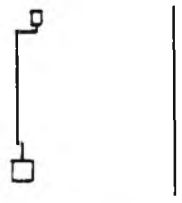


Cell : GJL / #

Row(s) : 2

Column(s) : 1

Placement - Row: Odd

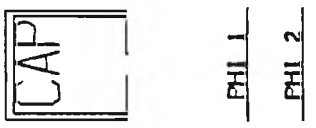


Cell : LCAP / #

Row(s) : 1

Column(s) : 1

Placement - Column: Even



Cell : RCAP / #

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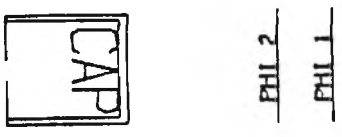
Column(s) : 1

Placement - Column: Odd

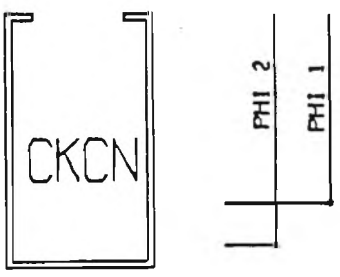


Cell : CKCN / #

Row(s) : 2

Column(s) : 1

Placement - Row: Odd



QUICK REFERENCES

Cell : PH1LCN / #

Row(s) : 1

Column(s) : 1

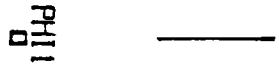
Placement - Column: Even

Cell : PH1RCN / #

Row(s) : 1

Column(s) : 1

Placement - Column: Odd

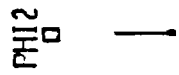


Cell : PH2LCN / #

Row(s) : 1

Column(s) : 1

Placement - Column: Even



Cell : PH2RCN / #

Row(s) : 1

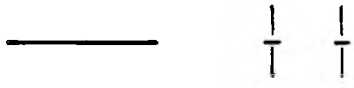
Column(s) : 1

Placement - Column: Odd

Cell : CBRK / #

Row(s) : 1

Column(s) : 1



Cell : RCBK / #

Row(s) : 1

Column(s) : 1

QUICK REFERENCES

Cell : LCBK / #

Row(s) : 1

Column(s) : 1

Cell : RBRK / #

Row(s) : 1

Column(s) : 1

Cell : CCN / #

Row(s) : 1

Column(s) : 1

Cell : CCL / #

Row(s) : 1

Column(s) : 1

Cell : CCR / #

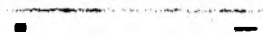
Row(s) : 1

Column(s) : 1

Cell : RCN / #

Row(s) : 1

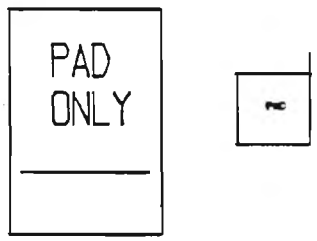
Column(s) : 1



QUICK REFERENCES

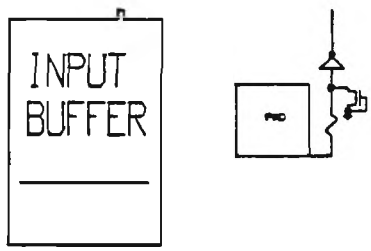
Cell : BLKPAD / #

SIZE : 2



Cell : IBUFPAD / #

SIZE : 2



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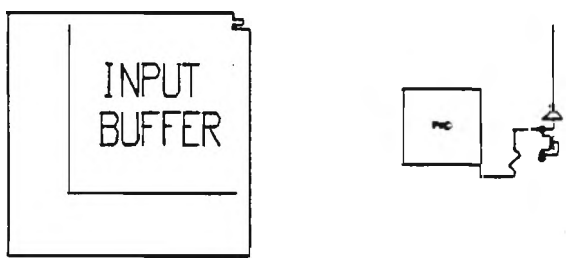
SIZE : 2



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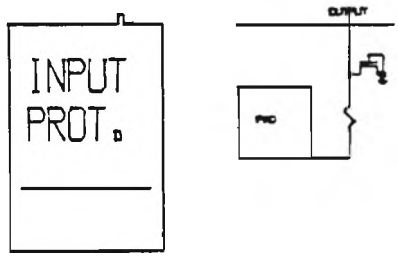
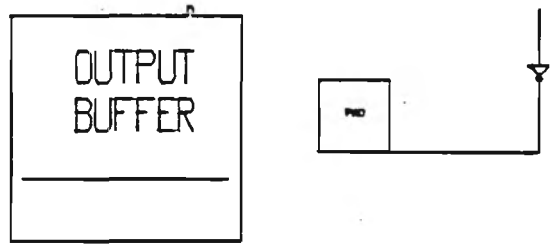


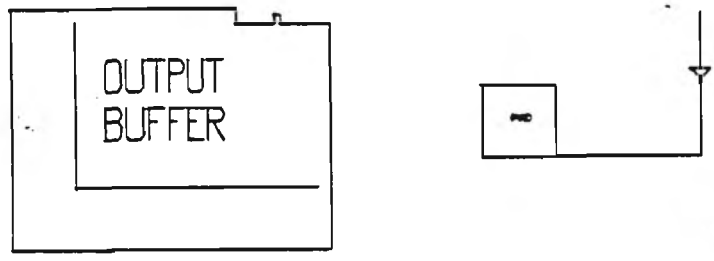
Cell : OBUFPAD / #

SIZE : 3



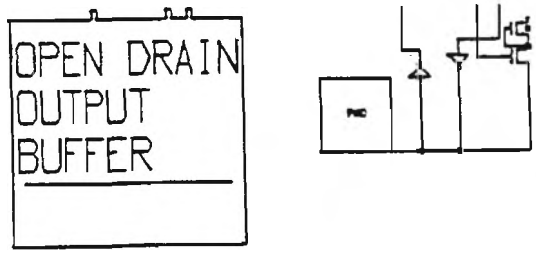
Cell : COBUFPAD / #

SIZE : 3



Cell : OCBUFPAD / #

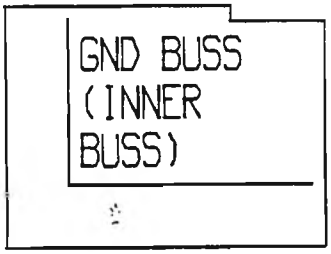
SIZE : 3



QUICK REFERENCES

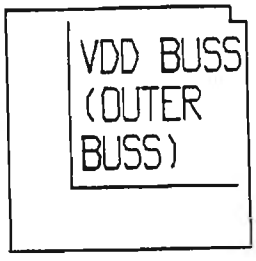
Cell : GNDPAD / #

SIZE : 3



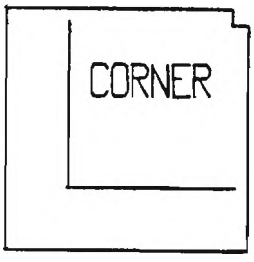
Cell : VDDPAD / #

SIZE : 2



Cell : CORNERPAD / #

SIZE : 2



Cell : FILLPAD / #

SIZE : 1

3. PRIMITIVE CELLS

The primitive cells consist of the following:

- Row detection cells: S,S2,R,R2,PLUS(+).
- Column detection cells: 1,0.
- OHMic contact cells: OCL(*),OCR(#),OCB(@).
- Inverter cells: INV01,INV10.

Some of the primitive cells are actually the same cell, as far as the schematic and composite are concerned, but since they perform different logical functions they are given different names.

PRIMITIVE CELLS

Cell Name - S

Function - set a flip-flop or latch.

Placement Restrictions - Column : Odd
Under or Over: FF,FFR,FFW,FFRW,LATCH,FFC

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .5 X .25 mill. or 12 X 6 micron.

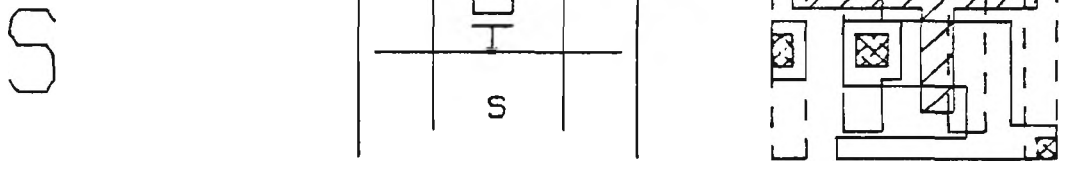


Figure 3-1: S CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - S2

Function - set a two wire latch.

Placement Restrictions - Under or Over : LATCH2

Size Column : 1
Row : 1

CIF Number -

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .5 X .25 mill. or 12 X 6 micron.

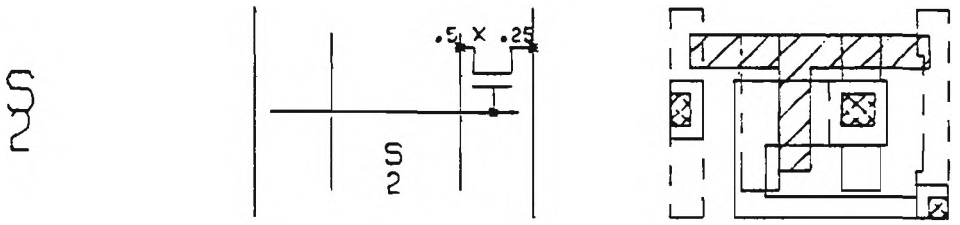


Figure 3-2: S2 CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - R

Function - Reset a flip flop or latch

Placement Restrictions - Column : Even
Under or Over: FF,FFR,FFW,FFRW,LATCH,FFC

Size Column : 1
Row : 1

CIF Number -

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .5 X .25 mill. or 12 X 6 micron.

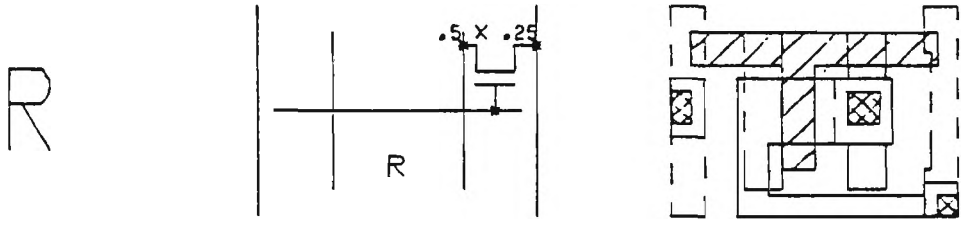


Figure 3-3: R CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - R2

Function - Reset a two wire latch

Placement Restrictions - Under or Over : LATCH2

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .5 X .25 mill. or 12 X 6 micron.

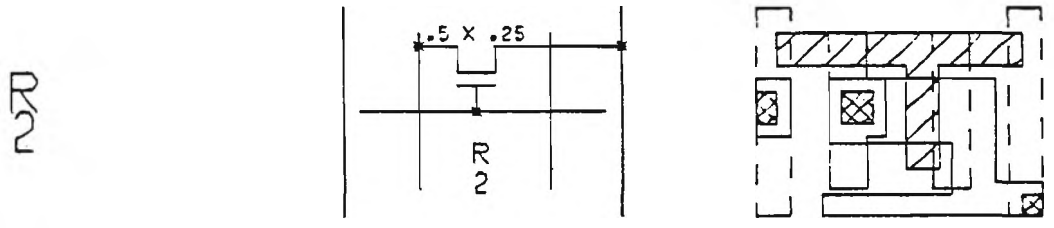


Figure 3-4: R2 CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - PLUS

Function - Transfer row signal to right column wire.

Placement Restrictions - Under or Over : No flip-flop or latch

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .5 X .25 mill. or 12 X 6 micron.

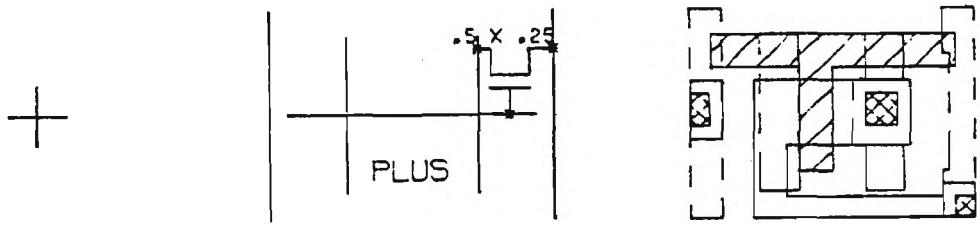


Figure 3-5: PLUS CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - 1

Function - Sense a true on the right column wire.

Placement Restrictions - None

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .5 X .25 mill. or 12 X 6 micron.

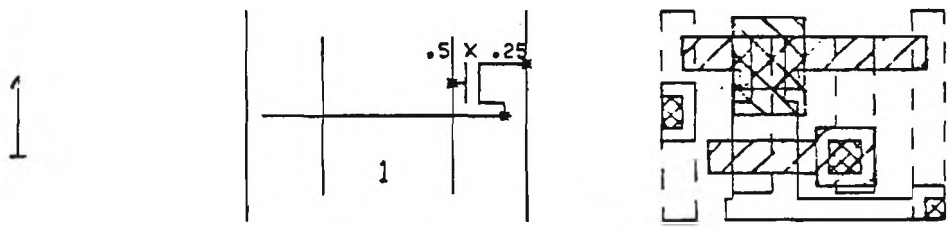


Figure 3-6: 1 CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - 0

Function - Sense a true on the left column wire.

Placement Restrictions - None

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .5 X .25 mill. or 12 X 6 micron.

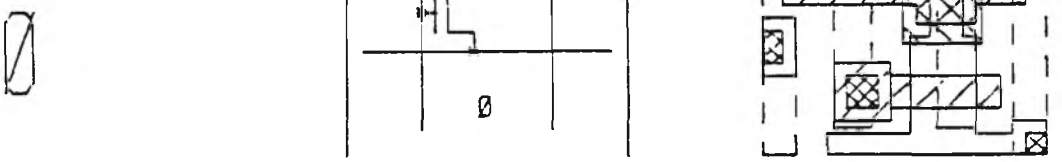


Figure 3-7: 0 CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - BLK

Function - Pass row and column wires.

Placement Restrictions - Where ever there is no other active cell.

Size Row : 1
Column : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

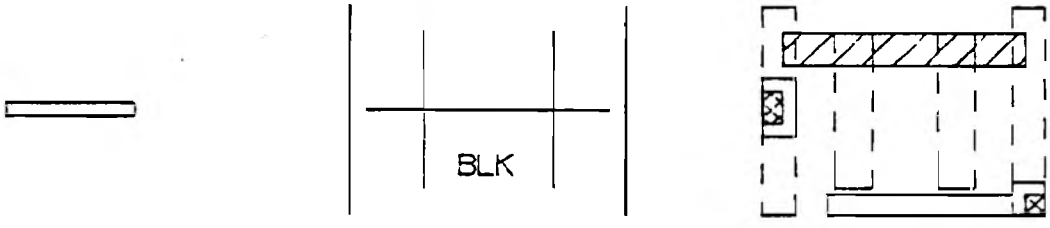


Figure 3-8: BLK CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - OCL

Function - Connect row to left column wire.

Placement Restrictions - None

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

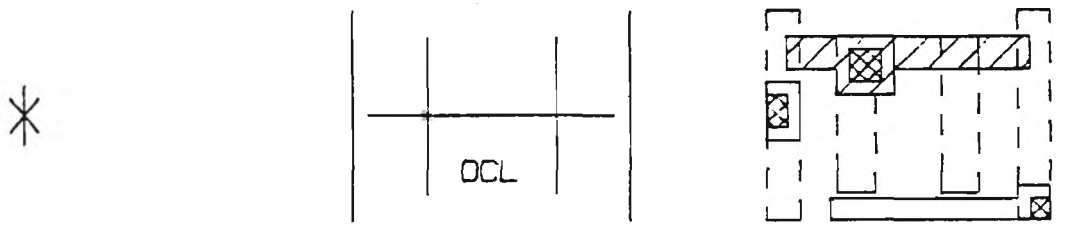


Figure 3-9: OCL CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - OCR

Function - Connect row to right column wire.

Placement Restrictions - None

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

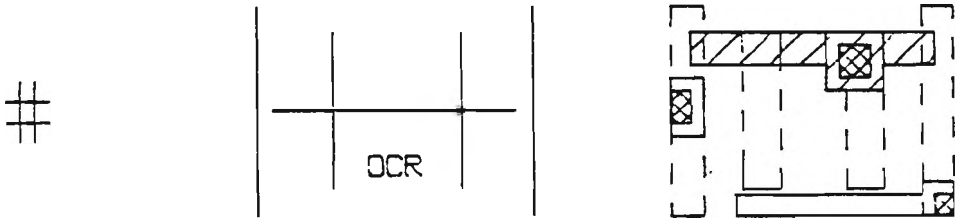


Figure 3-10: OCR CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - OCB

Function - Connect row to both column wires.

Placement Restrictions - None

CIF Number -

Size Column : 1
Row : 1

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

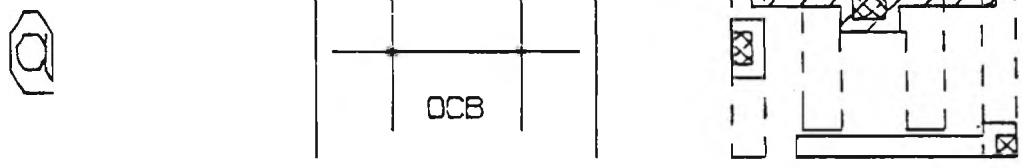


Figure 3-11: OCB CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - INV01

Function - Pull the left column wire low when the right wire is high.

Placement Restrictions - None

CIF Number -

Size Column : 1
Row : 1

Row capacitance - Row wire is not passed through this cell.

Left Col Capacitance -

Right Col Capacitance -

Row Resistance - Row wire is not passed through this cell.

Transistor size - .5 X .25 mill. or 12 X 6 micron.

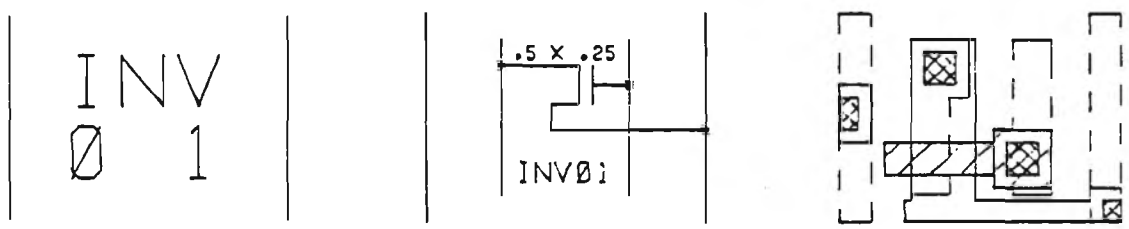


Figure 3-12: INV01 CELL GRAPHICS, SCHEMATIC AND COMPOSITE

PRIMITIVE CELLS

Cell Name - INV10

Function - Pull the right column wire low when the left one is high.

Placement Restrictions - None

CIF Number -

Size Column : 1
Row : 1

Row capacitance - Row wire is not passed through this cell.

Left Col Capacitance -

Right Col Capacitance -

Row Resistance - Row wire is not passed through this cell.

Transistor size - .5 X .25 mill. or 12 X 6 micron.

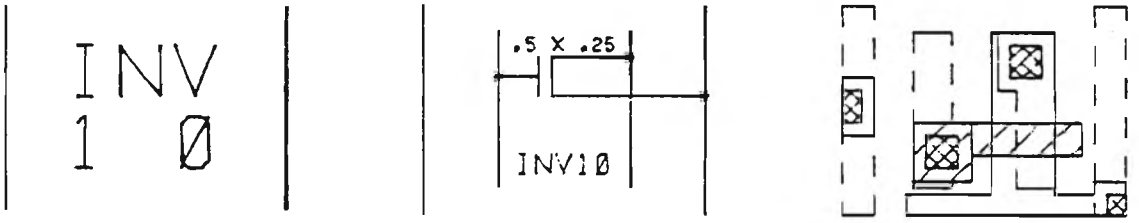


Figure 3-13: INV10 CELL GRAPHICS, SCHEMATIC AND COMPOSITE

4. COMPLEX ROW CELLS

The complex row cells include all flip flops, latches, pass transistors, and any other cell which occupies more than one row cell location. These cells include:

- Special inverter: SICUINV
- Pass transistor cells: CPT,CPTL,CPTR,RPT1,RPT2,RPTL,RPTR.
- Latch cells: LATCH2,LATCH.
- Flip flop cells: FF,FFC,FFR,FFW,FFRW.

The flip flops and latches present some special problems that should be taken into account:

- The latches have internal loads; therefore, no loads should be placed on their input or output wires.
- The flip flops have open collector outputs and so should have the CP2L and CP2R loads placed on the 1 and 0 wires. In the case of flip flops to form a buss, only one load should be placed on each of the 2 wires. The loads internal to the flip flop for the S and R wires are isolated from the rest of the PPL when PHI1 is off and so the CP3L and CP3R cells should be placed on the S and R wires to make them work correctly.

COMPLEX ROW CELLS

Cell Name - SICUINV

Function - Same as INV01 but with internal pull-ups.

Placement Restrictions - Row : Even

CIF Number -

Size Column : 1
Row : 1

Row capacitance - Row wire is not passed through this cell.

Left Col Capacitance -

Right Col Capacitance -

Row Resistance - Row wire is not passed through this cell.

Transistor size - enhancement= .5 X .25 mill. or 12 X 6 micron.
depletion= .25 X .5 mill. or 6 X 12 micron.

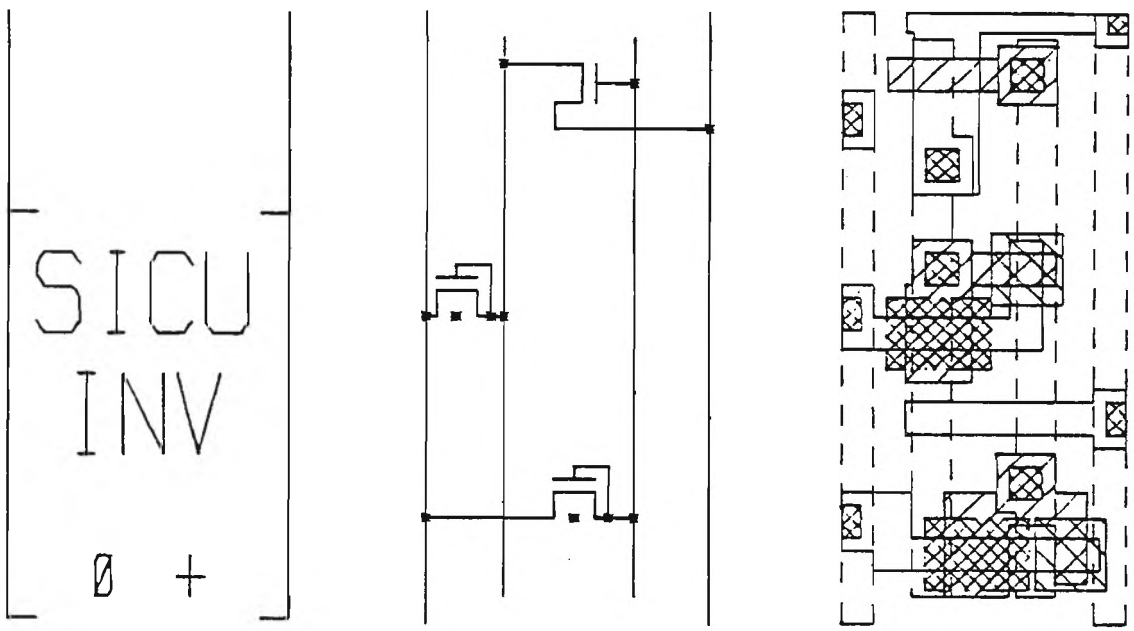


Figure 4-1: SICUINV CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - CPT

Function - Connect the column wires when the row is high.

Placement Restrictions - Row : Even

CIF Number -

Size Column : 1
Row : 2

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - 2.4 X .25 mill. or 50 X 6 micron.

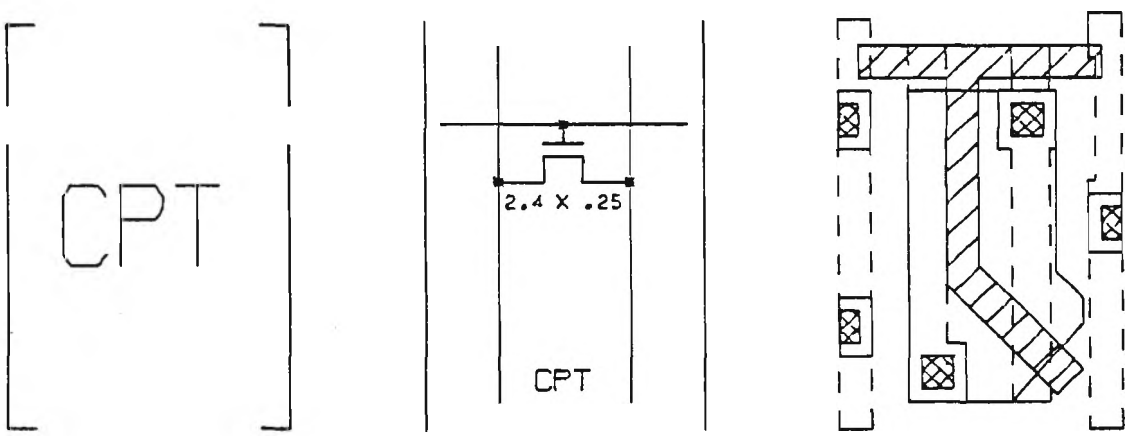


Figure 4-2: CPT CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - CPTL

Function - This cell places a pass-transistor in the left column wire which is activated when the row is high.

Placement Restrictions - Row : Odd

CIF Number -

Size Column : 1
Row : 2

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - 1.35 X .25 mill. or 32 X 6 micron.

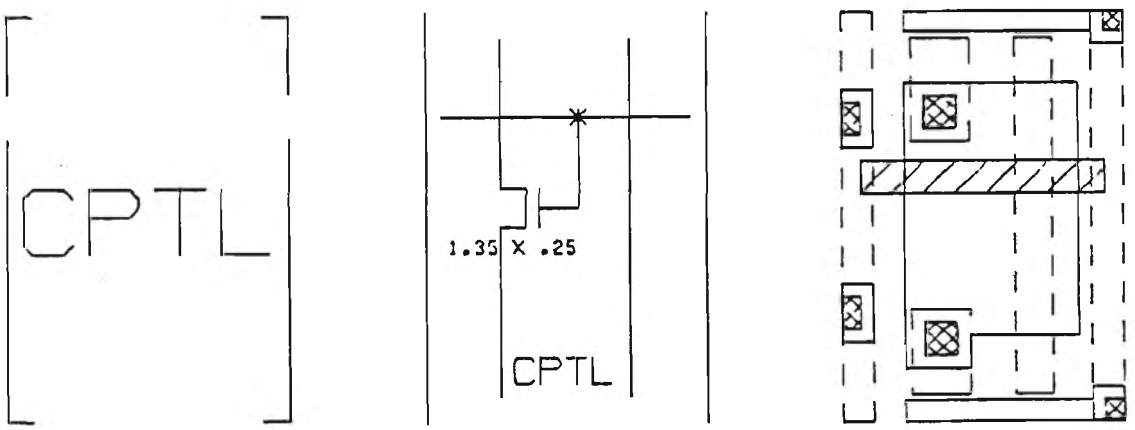


Figure 4-3: CPTL CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - CPTR

Function - This cell places a pass-transistor in the right column wire which is activated when the row is high.

Placement Restrictions - Row : Odd

CIF Number -

Size Column : 1
Row : 2

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - 1.35 X .25 mill. or 32 X 6 micron.

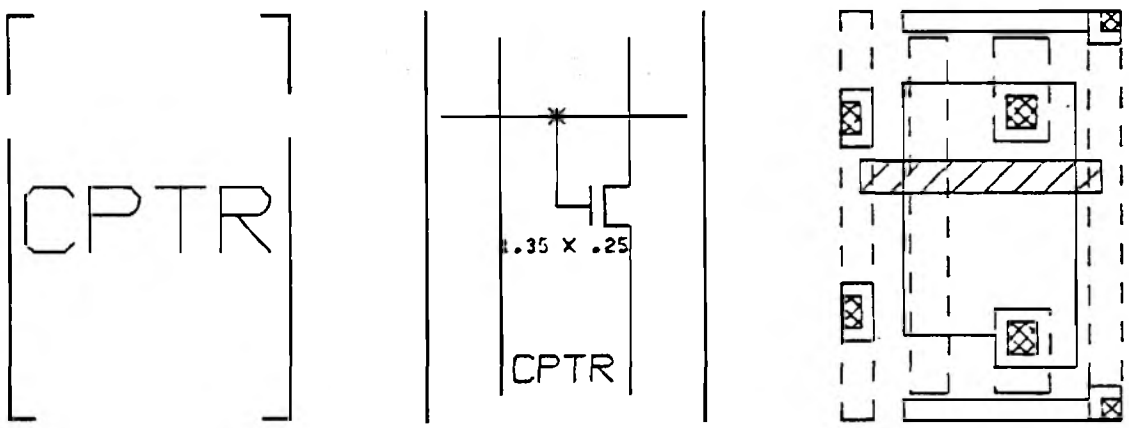


Figure 4-4: CPTR CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - RPT1

Function - Connect two row wires when left column wire is high.

Placement Restrictions - Row : Even

CIF Number -

Size Column : 1
Row : 2

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .9 X .25 mill. or 22 X 6 micron.

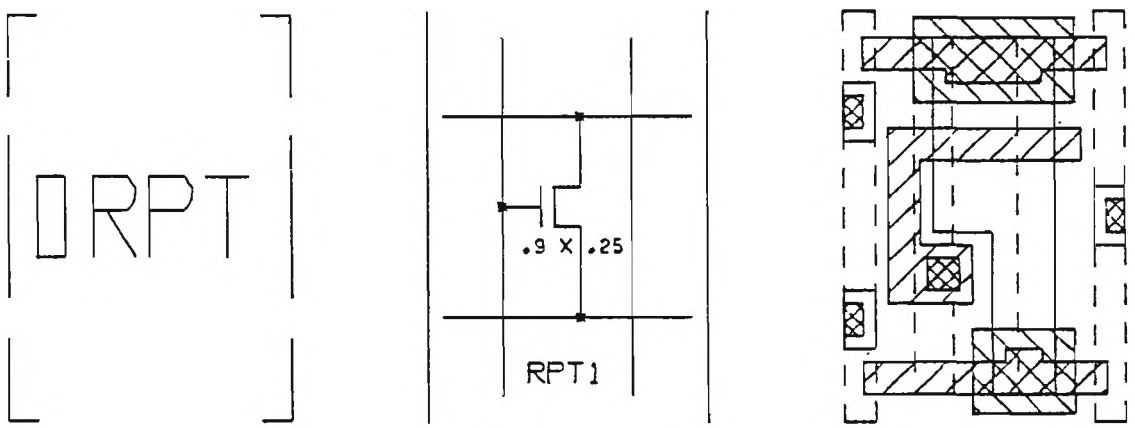


Figure 4-5: RPT1 CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - RPT2

Function - Connect two row wires when the right column wire is high.

Placement Restrictions - Row : Even

CIF Number -

Size Column : 1
Row : 2

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - .9 X .25 mill. or 22 X 6 micron.

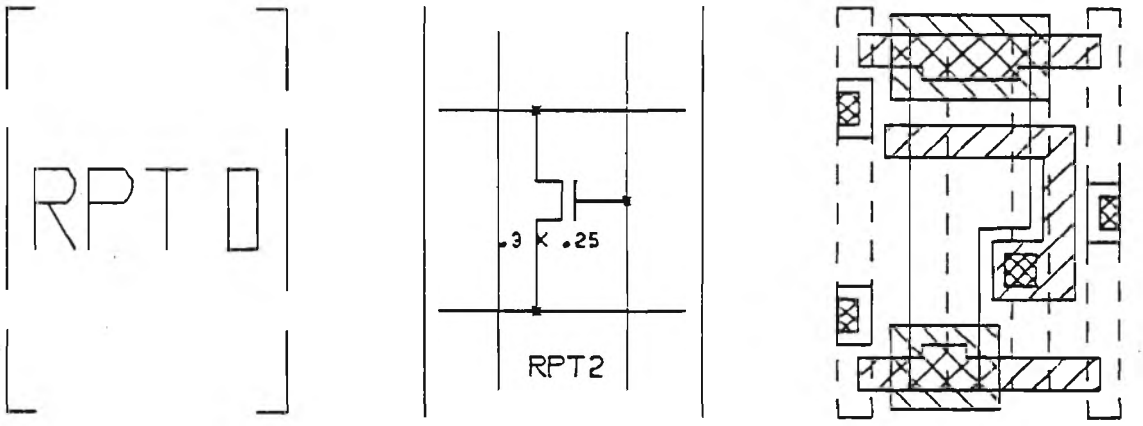


Figure 4-6: RPT2 CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - RPTR

Function - Insert a pass transistor in an odd row which is activated when the right column wire is high.

Placement Restrictions - Row : Even

CIF Number -

Size Column : 1
Row : 2

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - 1.4 X .25 mill. or 32 X 6 micron.

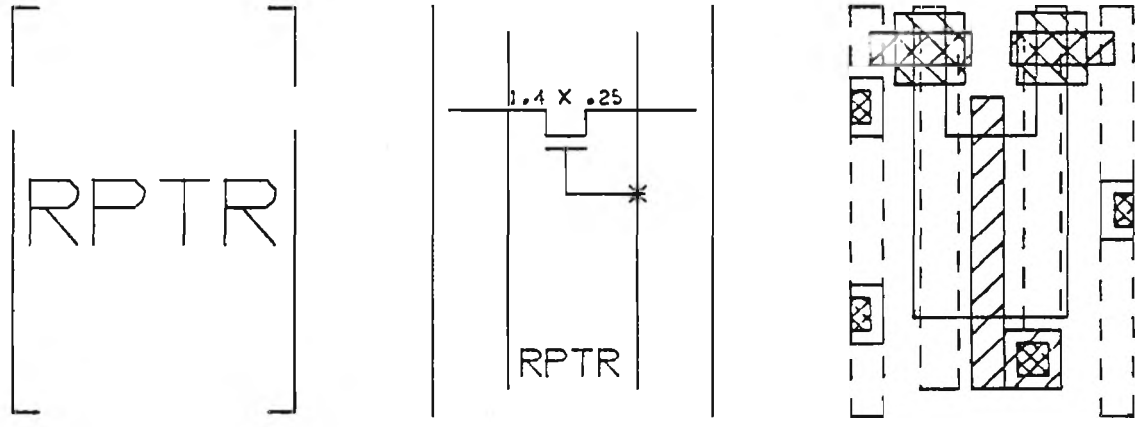


Figure 4-7: RPTR CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - RPTL

Function - Insert a pass-transistor in an odd row which is activated when the left column wire is high.

Placement Restrictions - Row : Even

CIF Number -

Size Column : 1
Row : 2

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor size - 1.4 X .25 mill. or 32 X 6 micron.

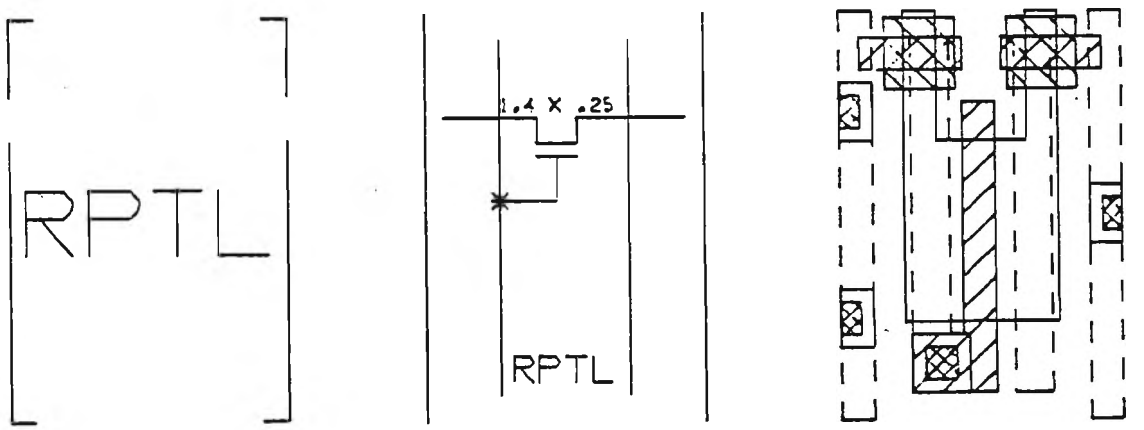


Figure 4-8: RPTL CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - LATCH2

Function - 2 wire asynchronous latch.

Placement Restrictions - Row : Even

CIF Number -

Size Column : 1
Row : 3

Row capacitance - Row wires are not passed through this cell.

Left Col Capacitance -

Right Col Capacitance -

Row Resistance - Row wires are not passed through this cell.

Transistor sizes - pull-ups= .25 X .5 mill. or 6 X 12 micron.
enhancement= .5 X .25 mill. or 12 X 6 micron.

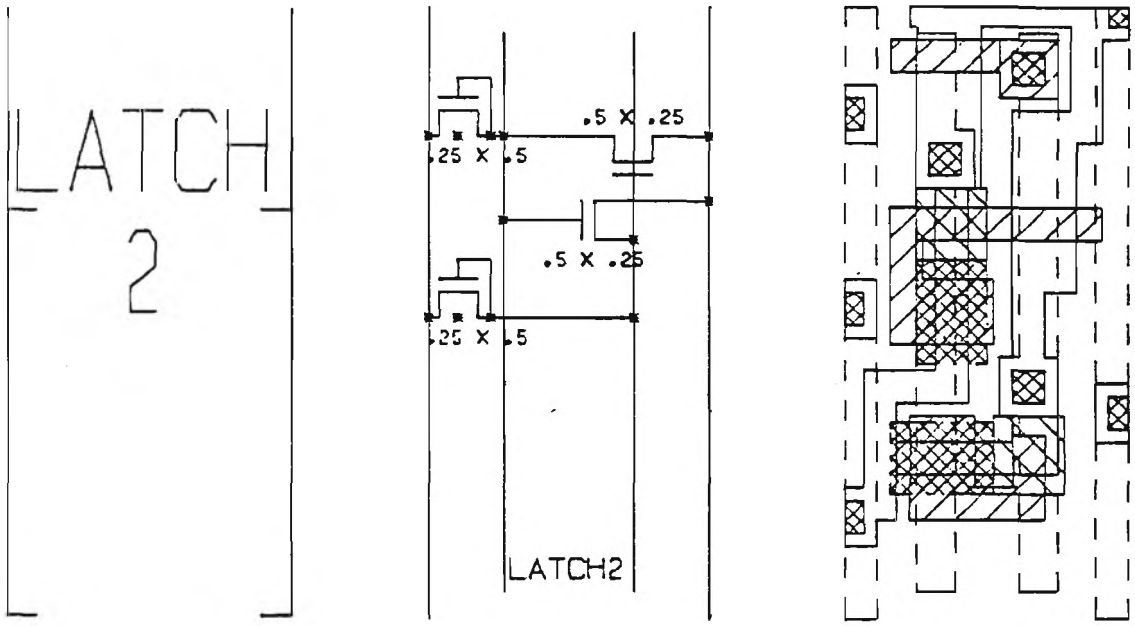


Figure 4-9: LATCH2 CELL GRAPHICS , SCHEMATIC AND COMPOSITE

COMPLEX ROW CELLS

Cell Name - LATCH

Function - Asynchronous S-R latch

Placement Restrictions - Column : Odd
Row : Even

CIF Number -

Size Column : 2
Row : 3

Row capacitance - Row wires are not passed through this cell.

Left Col Capacitance -

Right Col Capacitance -

Row Resistance - Row wires are not passed through this cell.

Transistor sizes - Q1=Q2=Q3=Q4=.25 X .5 mill. or 6 X 12 micron.
Q5=Q6=Q7=Q8=.5 X .25 mill. or 12 X 6 micron.

Graphics - Figure 4-10 on page 40

Schematic - Figure 4-11 on page 40

Composite - Figure 4-12 on page 41

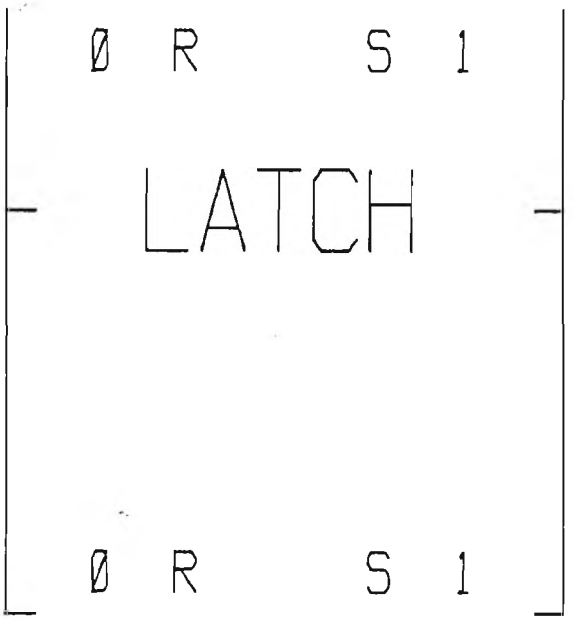


Figure 4-10: LATCH CELL GRAPHICS

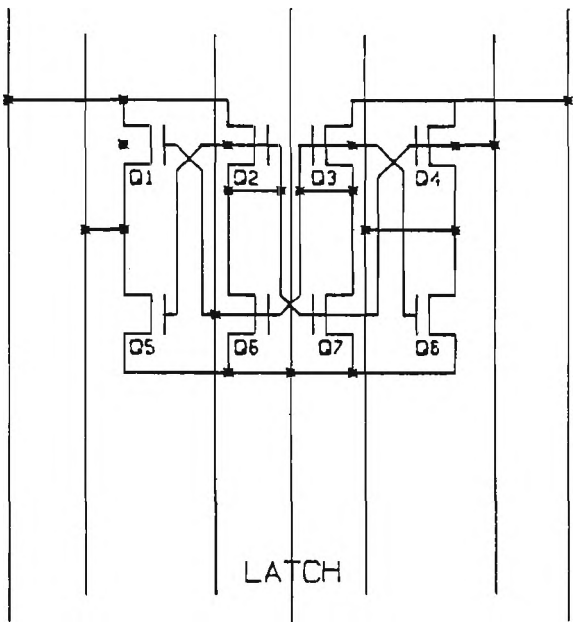


Figure 4-11: LATCH CELL SCHEMATIC

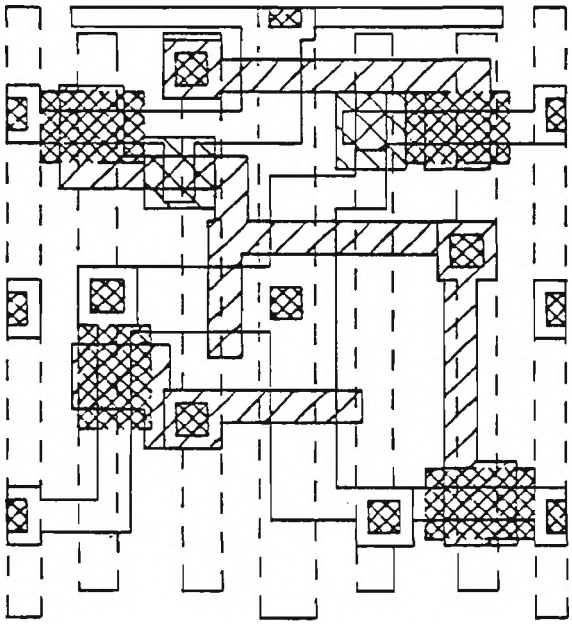


Figure 4-12: LATCH CELL COMPOSITE

COMPLEX ROW CELLS

Cell Name - FF

Function - Syncronous 2 phase Flip-Flop.

Placement Restrictions - Column : Odd
Row : Even

CIF Number -

Size Column : 2
Row : 4

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor sizes - Q1=Q2=Q9=Q10= .5 X .25 mill. or 12 X 6 micron.
Q3=Q4=Q7=Q8= .25 X .25 mill. or 6 X 6 micron.
Q5=Q6= .25 X 2 mill. or 6 X 30 micron.

Graphics - Figure 4-13 on page 43

Schematic - Figure 4-14 on page 44

Composite - Figure 4-15 on page 45

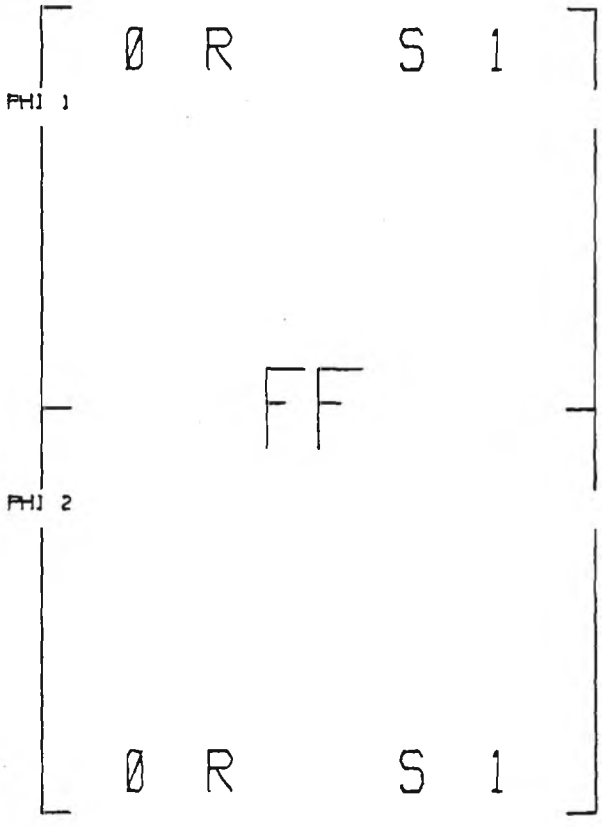


Figure 4-13: FF CELL GRAPHICS

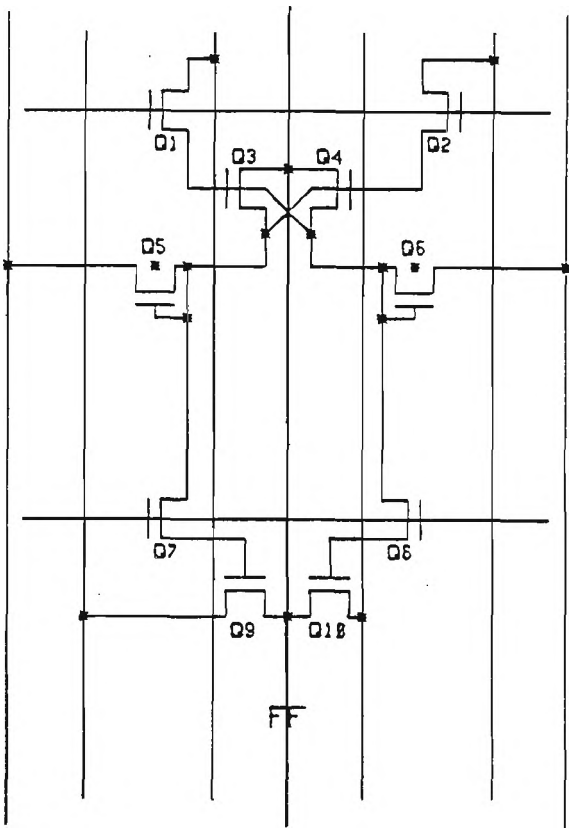


Figure 4-14: FF CELL SCHEMATIC

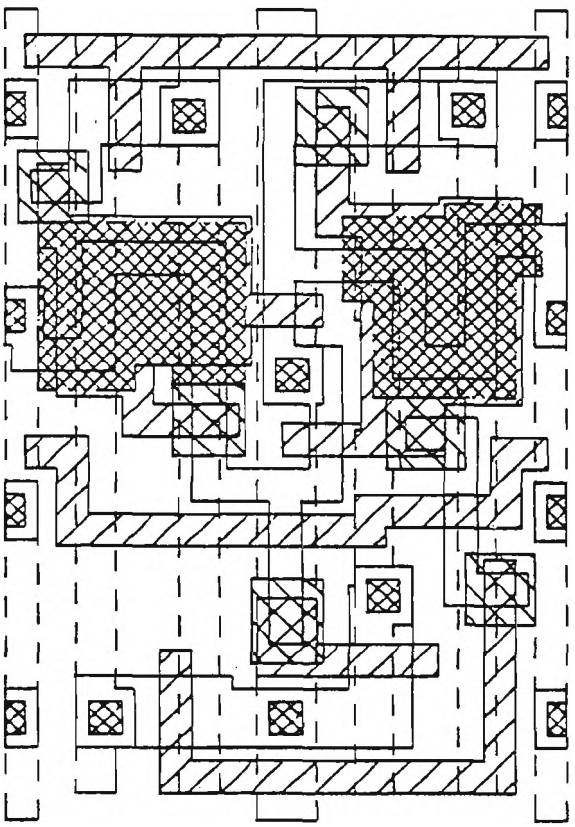


Figure 4-15: FF CELL COMPOSITE

COMPLEX ROW CELLS

Cell Name - FFC

Function - Flip-Flop with asynchronous clear.

Placement Restrictions - Column : Odd
Row : Odd

CIF Number -

Size Column : 2
Row : 5

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor sizes - Q1=Q2=Q10=Q11= .5 X .25 mill. or 12 X 6 micron.
Q3=Q4=Q7=Q8=Q9= .25 X .25 mill. or 6 X 6 micron.
Q5=Q6= .25 X 2 mill. or 6 X 30 micron.

Graphics - Figure 4-16 on page 47

Schematic - Figure 4-17 on page 48

Composite - Figure 4-18 on page 49

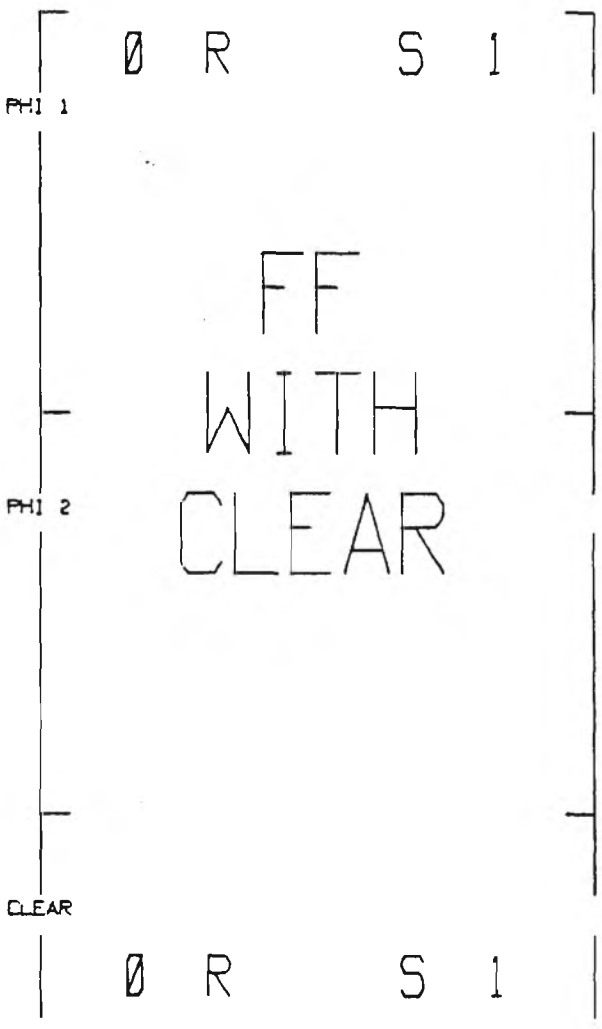


Figure 4-16: FFC CELL GRAPHICS

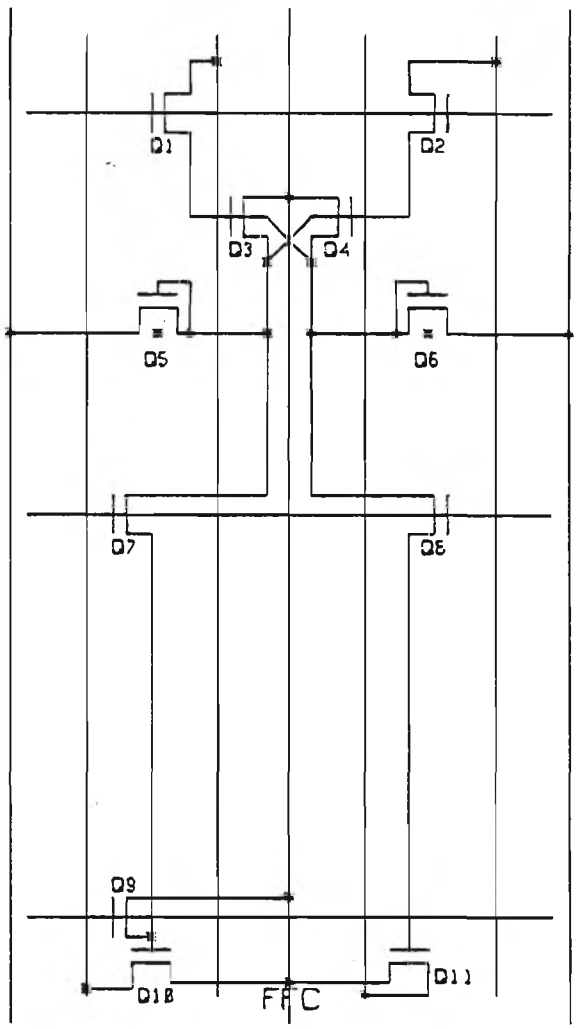


Figure 4-17: FFC CELL SCHEMATIC

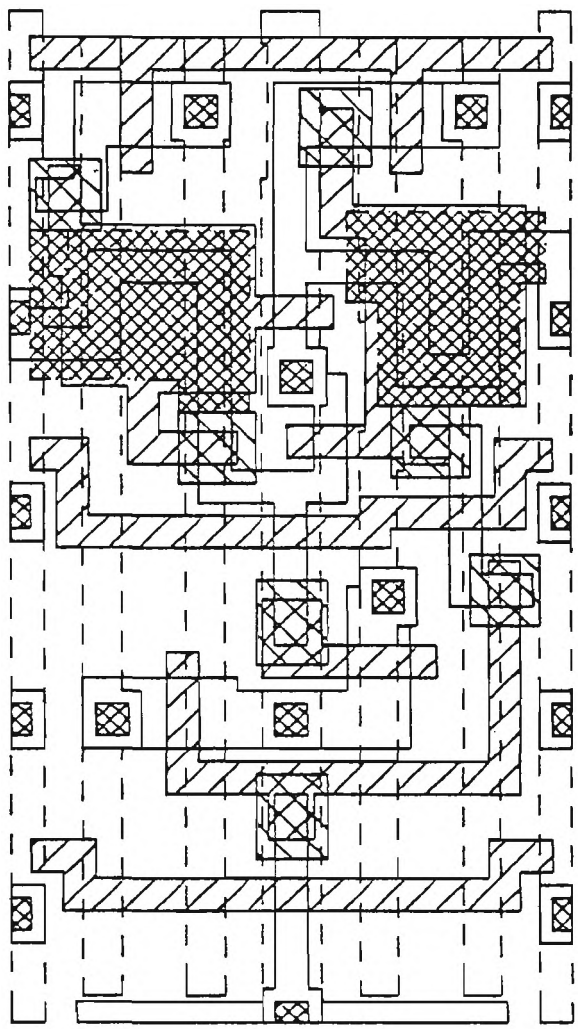


Figure 4-18: FFC CELL COMPOSITE

COMPLEX ROW CELLS

Cell Name - FFR

Function - Flip-Flop with read enable.

Placement Restrictions - Column : Odd
Row : Even

CIF Number -

Size Column : 2
Row : 6

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor sizes - Q1=Q2= .5 X .25 mill. or 12 X 6 micron.
Q3=Q4=Q7=Q8= .25 X .25 mill. or 6 X 6 micron.
Q9=Q10=Q11=Q12= 1 X .25 mill. or 24 X 6 micron.
Q5=Q6= .25 X 2 mill. or 6 X 30 micron.

Graphics - Figure 4-19 on page 51

Schematic - Figure 4-20 on page 52

Composite - Figure 4-21 on page 53

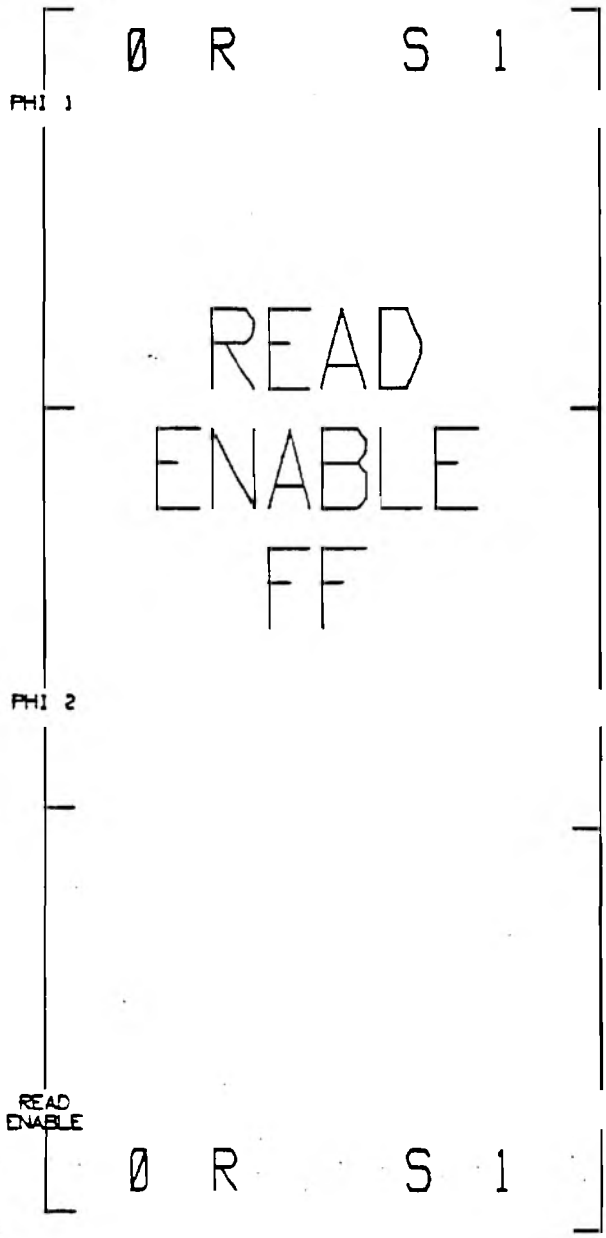


Figure 4-19: FFR CELL GRAPHICS

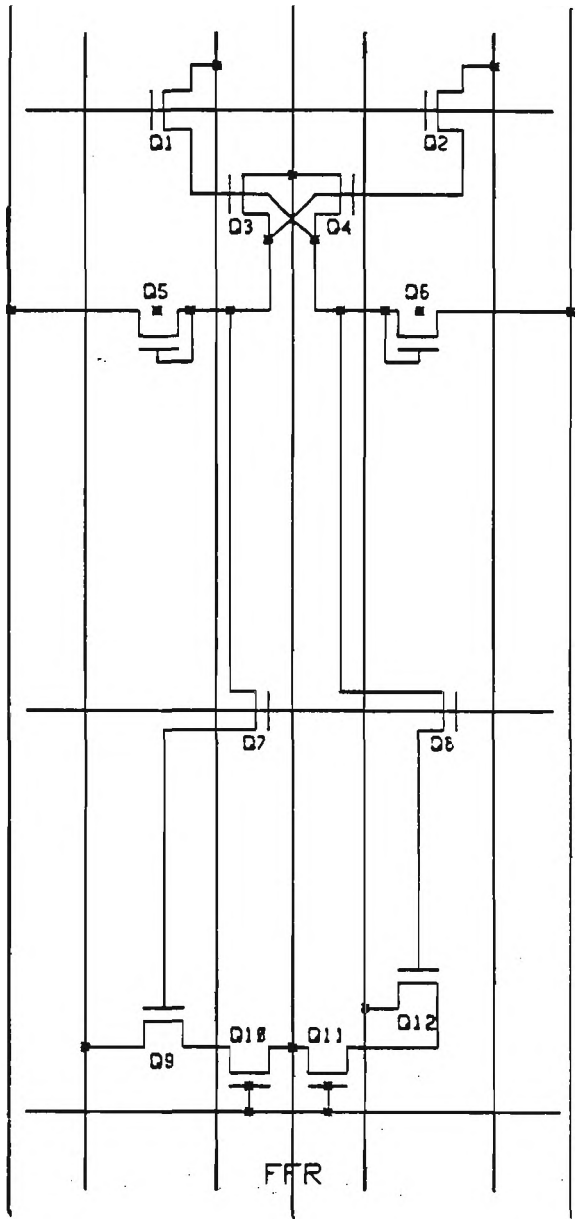


Figure 4-20: FFR CELL SCHEMATIC

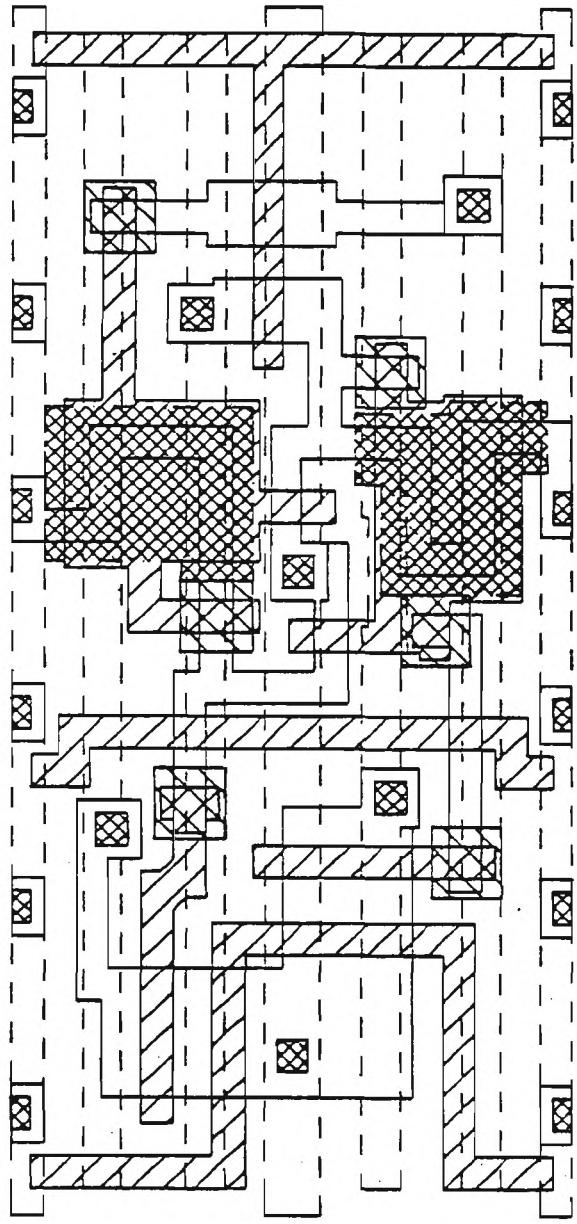


Figure 4-21: FFR CELL COMPOSITE

COMPLEX ROW CELLS

Cell Name - FFW

Function - Flip-flop with write enable.

Placement Restrictions - Column : Odd
Row : Even

CIF Number -

Size Column : 2
Row : 5

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transitor sizes - Q1=Q2=Q3=Q4= 1 X .25 mill. or 24 X 6 micron.
Q5=Q6=Q9=Q10= .25 X .25 mill. or 6 X 6 micron.
Q7=Q8= .25 X 2 mill. or 6 X 30 micron.
Q11=Q12= .5 X .25 mill. or 12 X 6 micron.

Graphics - Figure 4-22 on page 55

Schematic - Figure 4-23 on page 56

Composite - Figure 4-24 on page 57

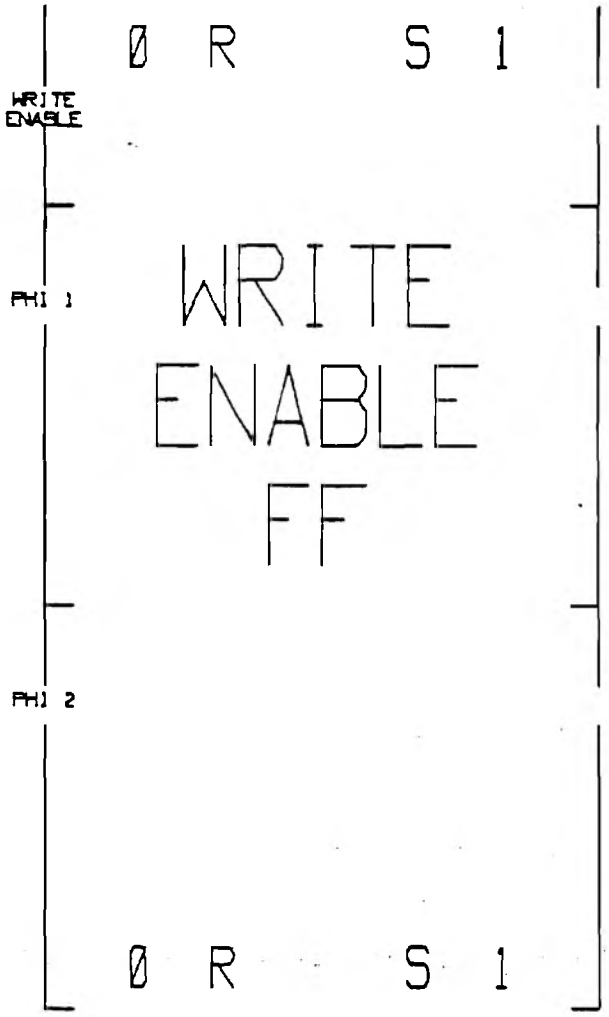


Figure 4-22: FFW CELL GRAPHICS

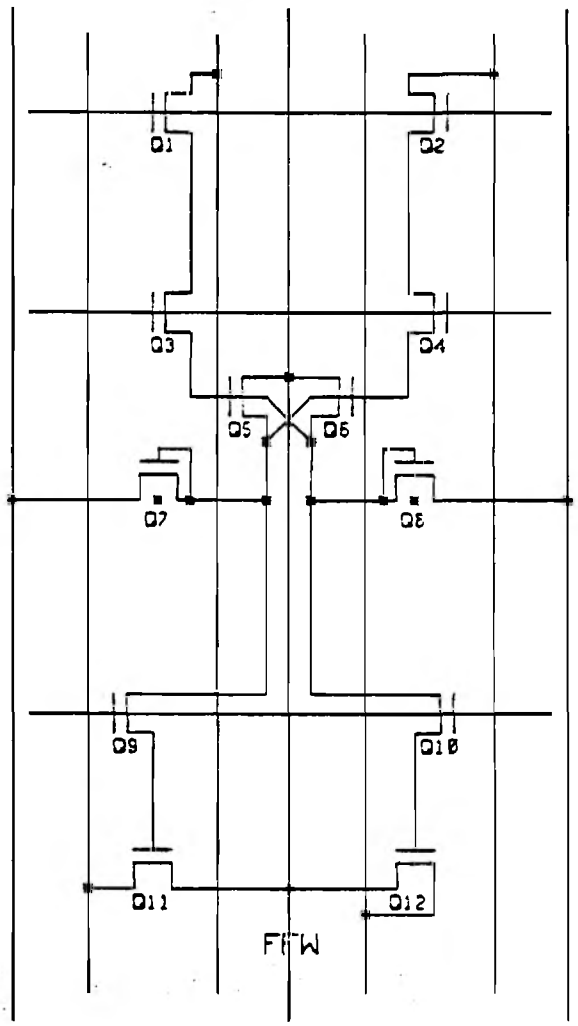


Figure 4-23: FFW CELL SCHEMATIC

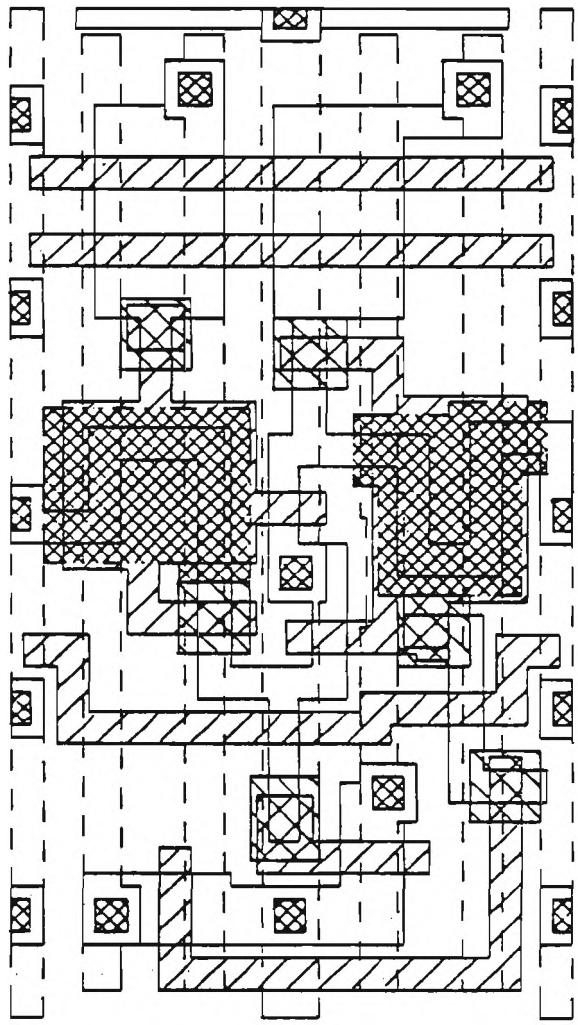


Figure 4-24: FFW CELL COMPOSITE

COMPLEX ROW CELLS

Cell Name - FFRW

Function - Flip-flop with both read and write enables.

Placement Restrictions - Column : Odd
Row : Odd

CIF Number -

Size Column : 2
Row : 7

Row capacitance -

Left Col Capacitance -

Right Col Capacitance -

Row Resistance -

Transistor sizes - Q1=Q2=Q3=Q4= 1 X .25 mill. or 24 X 6 micron.
Q5=Q6=Q9=Q10= .25 X .25 mill. or 6 X 6 micron.
Q7=Q8= .25 X 2 mill. or 6 X 30 micron.
Q11=Q12=Q13=Q14= 1 X .25 mill. or 24 X 6 micron.

Graphics - Figure 4-25 on page 59

Schematic - Figure 4-26 on page 60

Composite - Figure 4-27 on page 61

INTERCONNECT CELLS

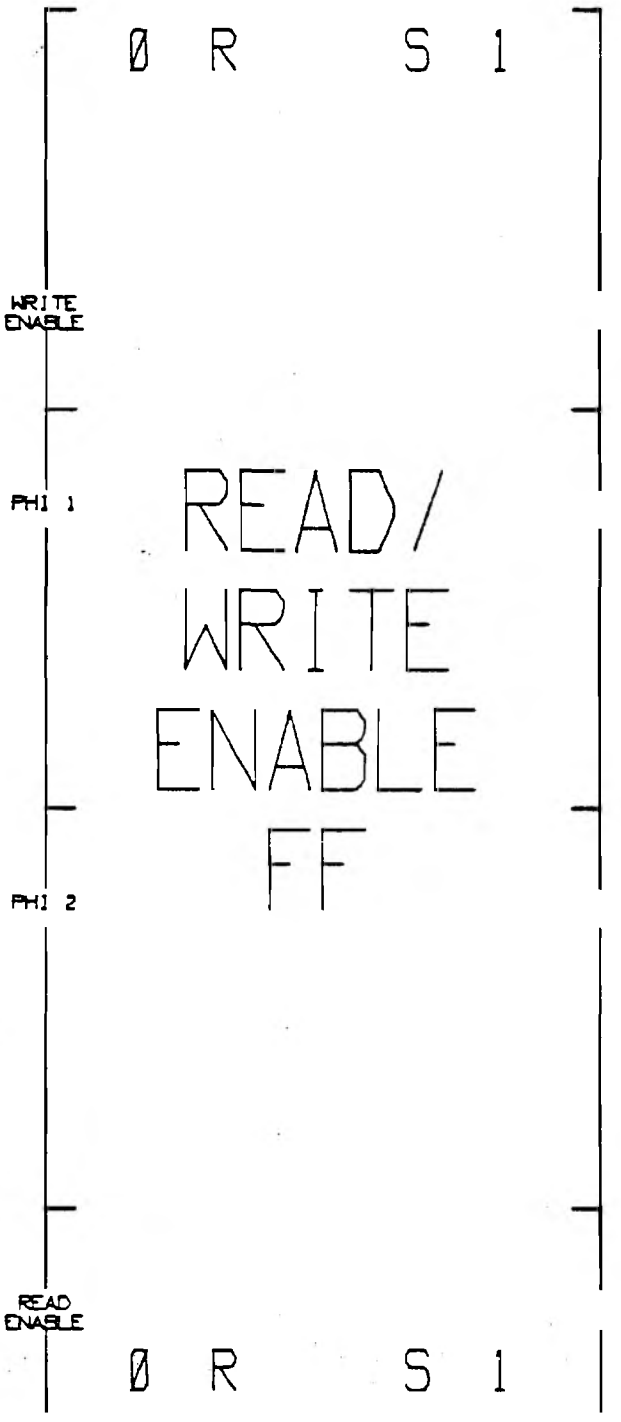


Figure 4-25: FFRW CELL GRAPHICS

INTERCONNECT CELLS

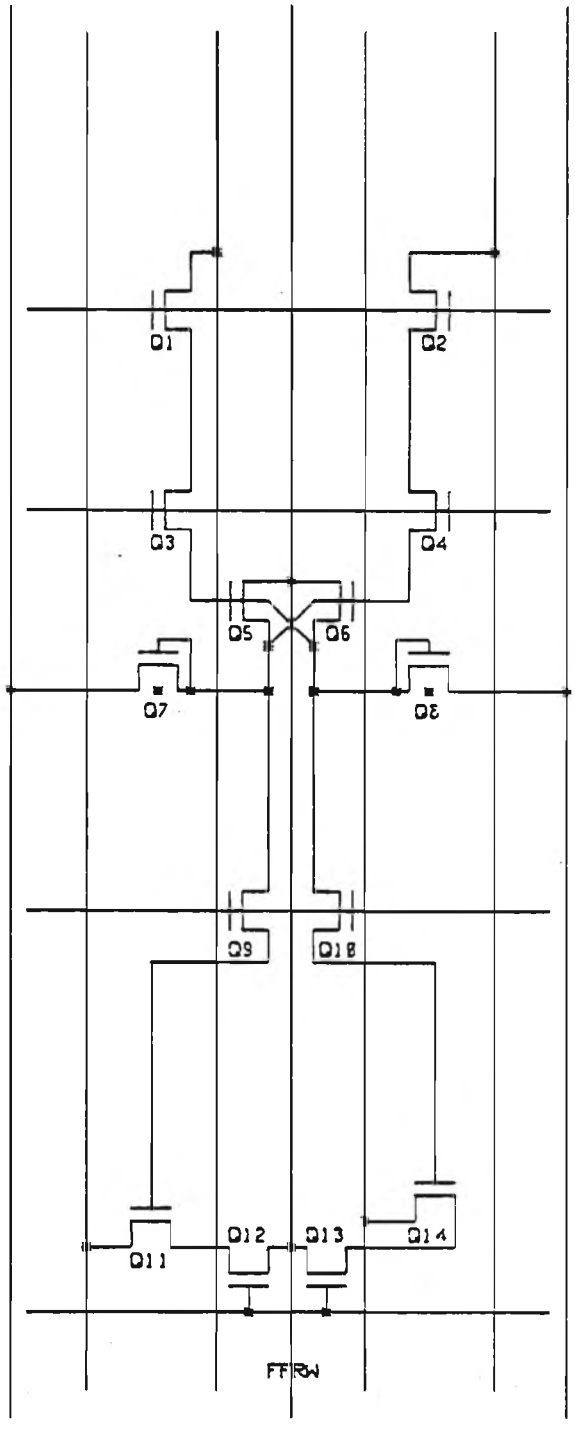


Figure 4-26: FFRW CELL SCHEMATIC

INTERCONNECT CELLS

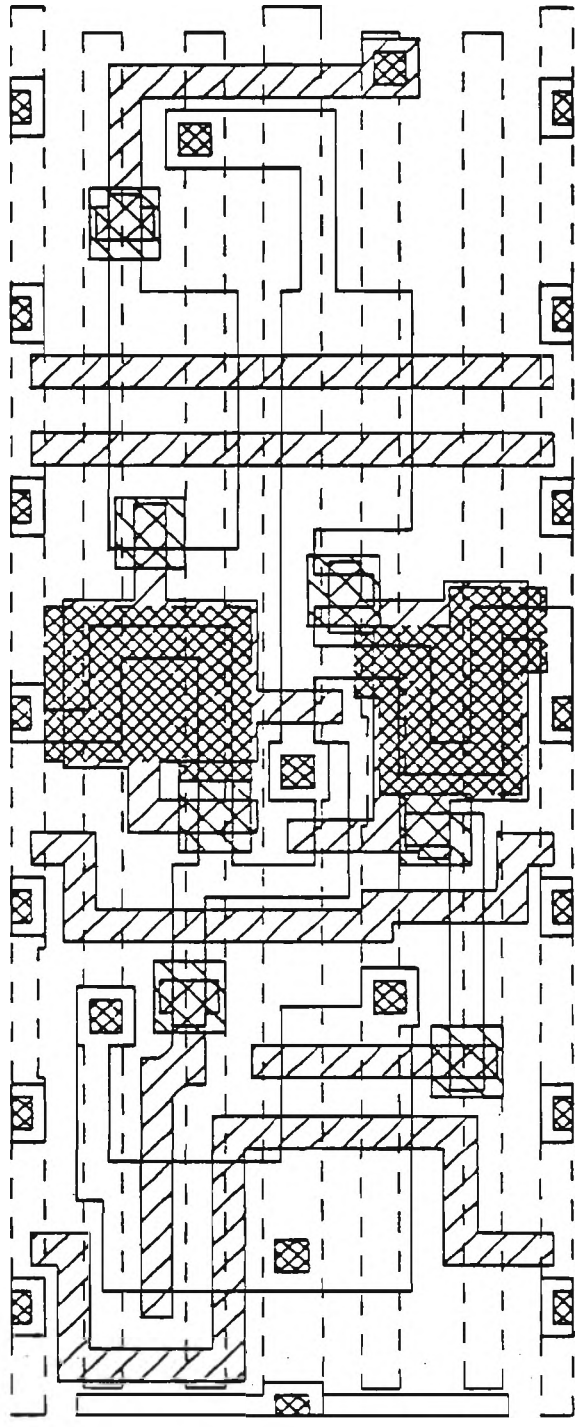


Figure 4-27: FFRW CELL COMPOSITE

5. INTERCONNECT CELLS

In the current PPL design system, all row cell interconnections have to be explicitly made by the insertion of these cells. A set of break cells are also included to be an aid to the designer in doing the PPL layout. These break cells perform no actual function however, and in order for the circuit to operate correctly all column and row connections must be explicitly inserted between the each cell where a connection is desired.

Included in these cells are:

- Column break cells: RCBK,LCBK,CBRK.
- Column connect cells: CCR,CCL,CCN.
- Row break cell: RBRK.
- Row connect cell: RCN.
- Clock connection cells: PH1LCN,PH1RCN,PH2LCN,PH2RCN.

Cell Name - CCR

Function - Connect right column wire between two row cells.

Cell Size Row : .5
Column : .5

Placement Restrictions Row : None
Column : Between

CIF number -

Figure 5-1: CCR CELL GRAPHICS AND SCHEMATIC

INTERCONNECT CELLS

Cell Name - CCL

Function - Connect left column wire between row cells.

Cell Size Row : .5
Column : .5

Placement Restrictions Row : None
Column : Between

CIF number -

Figure 5-2: CCL CELL GRAPHICS AND SCHEMATIC

INTERCONNECT CELLS

Cell Name - CCN

Function - Connect both column wires between row cells.

Cell Size Row : .5
Column : .5

Placement Restrictions Row : None
Column : Between

CIF number -

Figure 5-3: CCN CELL GRAPHICS AND SCHEMATIC

INTERCONNECT CELLS

Cell Name - RCN

Function - Connect row wire between adjacent row cells.

Cell Size Row : .5
Column : .5

Placement Restrictions Row : Between
Column : None

CIF Number -

Figure 5-4: RCN CELL GRAPHICS AND SCHEMATIC

INTERCONNECT CELLS

Cell Name - RCBK

Function - Indicate where right column wire is to be broken.

Cell Size Row : .5
Column : .5

Placement Restrictions - Between any two columns

Figure 5-5: RCBK CELL GRAPHICS

INTERCONNECT CELLS

Cell Name - LCBK

Function - Indicate where left column wire is to be broken.

Cell Size Row : .5
Column : .5

Placement Restrictions - Between any two columns

Figure 5-6: LCBK CELL GRAPHICS

INTERCONNECT CELLS

Cell Name - CBRK

Function - Indicate where both column wires are to be broken.

Cell Size Row : .5
Column : .5

Placement Restrictions - Between any two columns

Figure 5-7: CBRK CELL GRAPHICS

INTERCONNECT CELLS

Cell Name - RBRK

Function - Indicate where row is to be broken. (not a physical cell.)

Cell Size Row : .5
Column : .5

Placement Restrictions - Between any two rows

Figure 5-8: RBRK CELL GRAPHICS

INTERCONNECT CELLS

Cell Name - PH1LCN

Function - Connect PHI 1 clock to left side of circuit.

Placement Restrictions - Column : Even
Row : None
To side of : Where needed

CIF Number -

Size Column : 1
Row : 1

Cell capacitance -

Cell Resistance -

Figure 5-9: PH1LCN CELL GRAPHICS , SCHEMATIC AND COMPOSITE

INTERCONNECT CELLS

Cell Name - PH1RCN

Function - Connect PHI 1 clock to right side of circuit.

Placement Restrictions - Column : Odd
Row : None
To side of : Where needed

CIF Number -

Size Column : 1
Row : 1

Cell capacitance -

Cell Resistance -

Figure 5-10: PH1RCN CELL GRAPHICS , SCHEMATIC AND COMPOSITE

INTERCONNECT CELLS

Cell Name - PH2LCN

Function - Connect PHI 2 clock to left side of circuit.

Placement Restrictions - Column : Even
Row : None
To side of : Where needed

CIF Number -

Size Column : 1
Row : 1

Cell capacitance -

Cell Resistance -

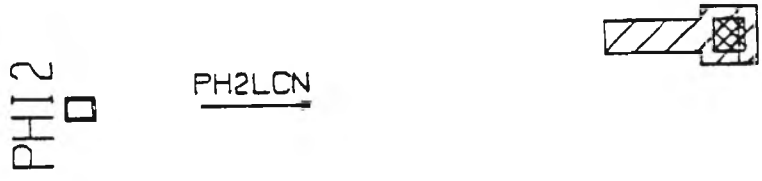


Figure 5-11: PH2LCN CELL GRAPHICS , SCHEMATIC AND COMPOSITE

INTERCONNECT CELLS

Cell Name - PH2RCN

Function - Connect PHI 2 clock to right side of circuit.

Placement Restrictions - Column : Odd
Row : None
To side of : Where needed

CIF Number -

Size Column : 1
Row : 1

Cell capacitance -

Cell Resistance -

Figure 5-12: PH2RCN CELL GRAPHICS , SCHEMATIC AND COMPOSITE

6. PULL-UP CELLS

The load cells contained here are required for proper operation of the PPL. Care should be taken that the conventional 4:1 and 8:1 ratios are observed between pullups and pulldowns where non-standard usage of the loads is concerned.

Cell Name - RPU

Function - Pull up a row wire.

Cell Size Row : 1
Column : 1

Placement Restrictions Row : None
Column : None
Under Or Over : Anything

Transitor Size Metric : 6 X 12 u
English : .25 X .5 mill

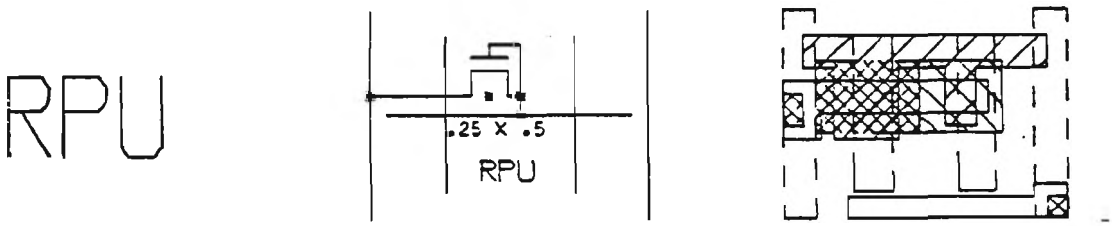


Figure 6-1: RPU CELL GRAPHICS , SCHEMATIC AND COMPOSITE

PULL-UP CELLS

Cell Name - CP1L

Function - Pull up left column wire on a column with no flip-flops or latches.

Cell Size Row : 1
Column : 1

Placement Restrictions Row : None
Column : None
Under Or Over : No flip-flop or latch

Transitor Size Metric : 6 X 12 u
English : .25 X .5 mill

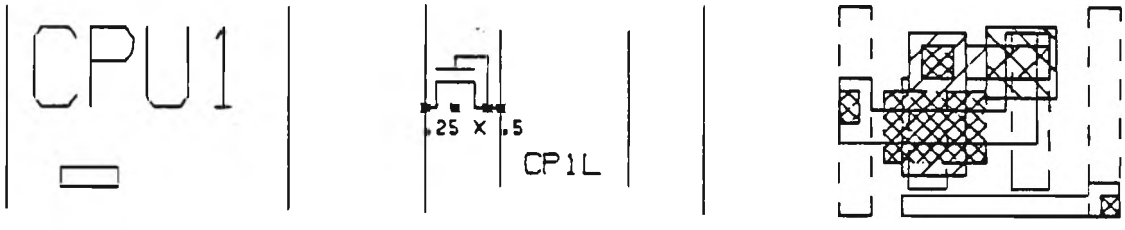


Figure 6-2: CP1L CELL GRAPHICS , SCHEMATIC AND COMPOSITE

PULL-UP CELLS

Cell Name - CP1R

Function - Pull up right column wire on a column with no flip-flops or latches.

Cell Size - Row : 1
Column : 1

Placement Restrictions Row : None
Column : None
Under Or Over : No flip-flop or latch

Transitor Size Metric : 6 X 12 u
English : .25 X .5 mill

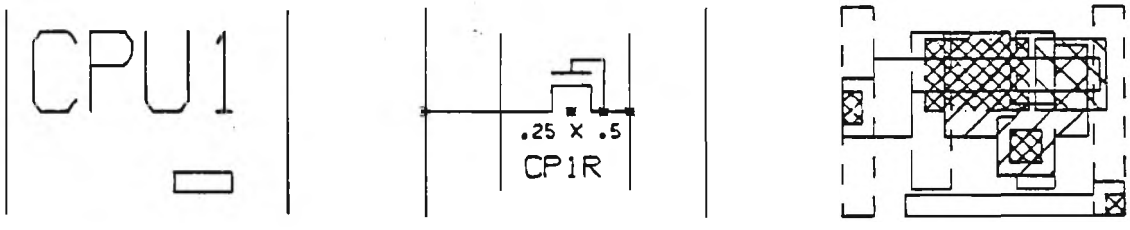


Figure 6-3: CP1R CELL GRAPHICS , SCHEMATIC AND COMPOSITE

PULL-UP CELLS

Cell Name - CP2L

Function - Pull up 0 column wire of a flip-flop.

Cell Size Row : 1
Column : 1

Placement Restrictions Row : None
Column : Odd
Under Or Over : (FF,FFR,FFW,FFRW,FFC)

Transitor Size Metric : 6 X 24 u
English : .25 X 1.0 mill

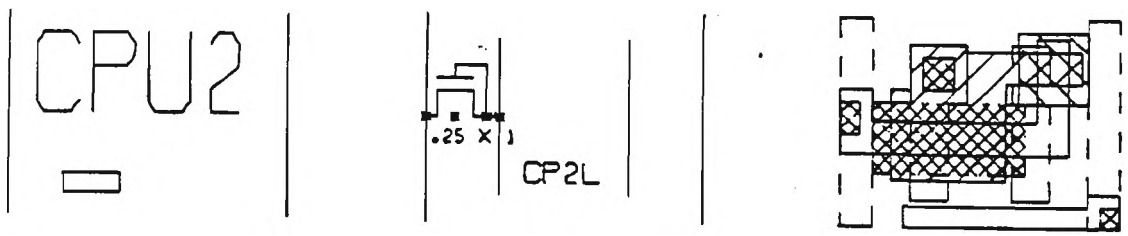


Figure 6-4: CP2L CELL GRAPHICS , SCHEMATIC AND COMPOSITE

PULL-UP CELLS

Cell Name - CP2R

Function - Pull up the 1 column wire of a flip-flop.

Cell Size Row : 1
Column : 1

Placement Restrictions Row : None
Column : Even
Under Or Over : (FF,FFR,FFW,FFRW,FFC)

Transitor Size Metric : 6 X 24 u
English : .25 X 1.0 mill

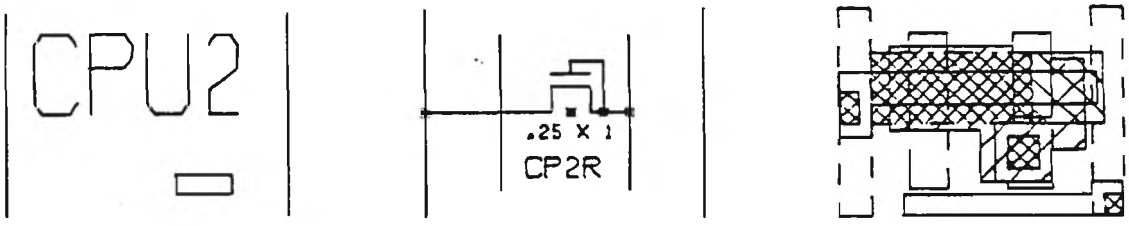


Figure 6-5: CP2R CELL GRAPHICS , SCHEMATIC AND COMPOSITE

PULL-UP CELLS

Cell Name - CP3L

Function - Pull up the S column wire of a flip-flop.

Cell Size Row : 2
Column : 1

Placement Restrictions Row : Even
Column : Even
Under Or Over : (FF,FFR,FFW,FFRW,FFC)

Transitor Size Metric : 6 X 48 u
English : .25 X 2.0 mill

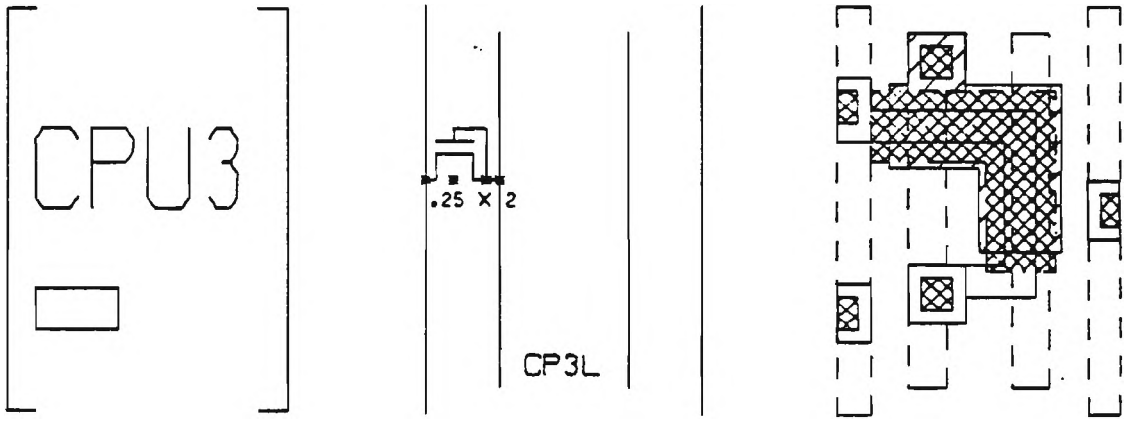


Figure 6-6: CP3L CELL GRAPHICS , SCHEMATIC AND COMPOSITE

PULL-UP CELLS

Cell Name - CP3R

Function - Pull up the R column wire of a flip-flop.

Cell Size Row : 2
Column : 1

Placement Restrictions Row : Even
Column : Odd
Under Or Over : (FF,FFR,FFW,FFRW,FFC)

Transitor Size Metric : 6 X 48 u
English : .25 X 2.0 mill

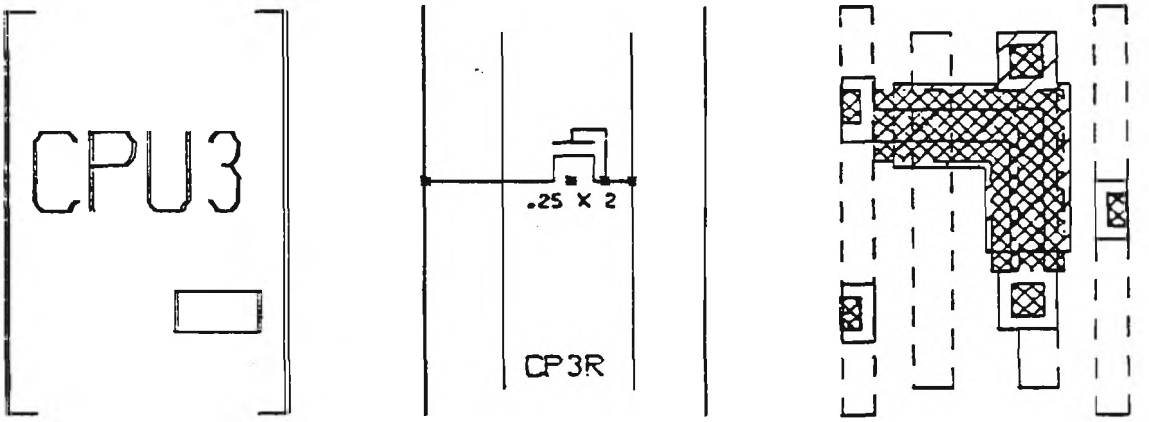


Figure 6-7: CP3R CELL GRAPHICS , SCHEMATIC AND COMPOSITE

7. BUSSING CELLS

The bussing cells include:

- BUSS cells: VBUS,GBUS,RCAP,LCAP,CKCN.

- BUSS jumper cells: VJR,VJL,GJR,GJL.

These cells are used to supply power, ground, and clocks to the PPL circuit. They are also used to output and input signals to/from the PPL circuit. These cells must be placed around the perimeter of the PPL in order for it to operate correctly.

The VBUS and its associated jumpers must be placed along the top of the array, the GBUS and its jumpers go on the bottom. The LCAP and RCAP cells go on the left and right sides of the array respectively. The CKCN cell is used to take the clock signals carried in the LCAP and RCAP cells route them under the GBUS cell. In this way the clock can be supplied to both sides of the circuit. Do not use the CKCN cell anywhere other than the lower left and right corners of the circuit - leave the upper left and right corners empty. A sample circuit is shown at the end of this manual.

BUSSING CELLS

Cell Name - VBUS

Function - Supply Vdd to circuit

Placement Restrictions - Column : None
Row : Even
Over : Complete circuit

CIF Number -

Size Row : 2
Column : 1

Cell capacitance -

Cell resistance -

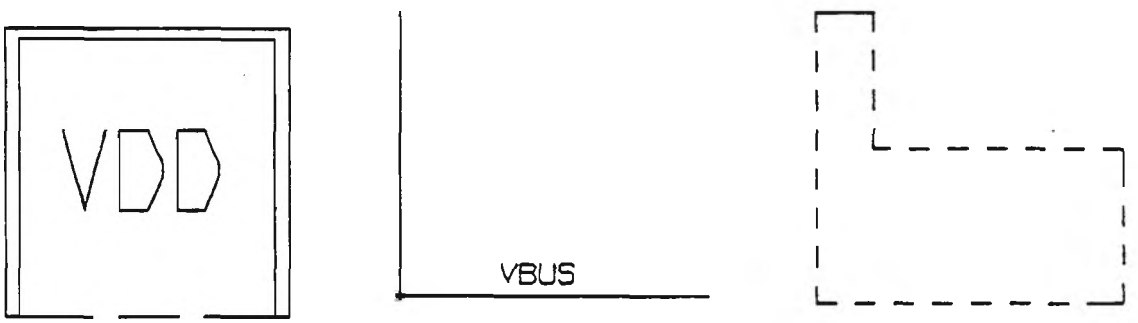


Figure 7-1: VBUS CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - GBUS

Function - Supply ground to the circuit, and chanel clock wires across the circuit.

Placement Restrictions - Column : None
Row : Odd
Under : Complete circuit

CIF Number -

Size Column : 1
Row : 2

Cell capacitance -

Cell resistance -

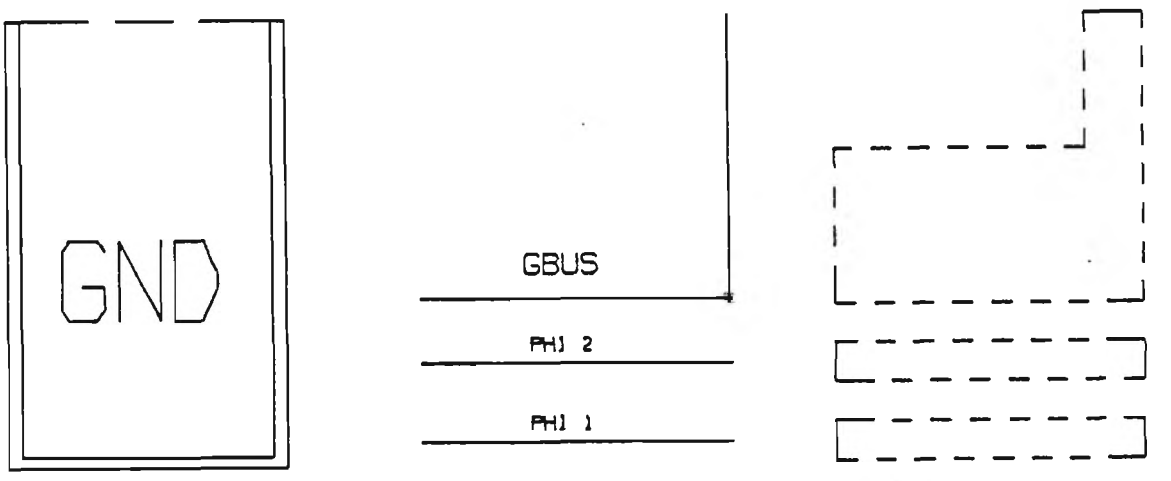


Figure 7-2: GBUS CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - CKCN

Function - Connect side clock wires to clock wires in GBUS

Placement Restrictions - Lower left and right corners

CIF Number -

Size Column : 1
Row : 2

Cell capacitance -

Cell resistance -

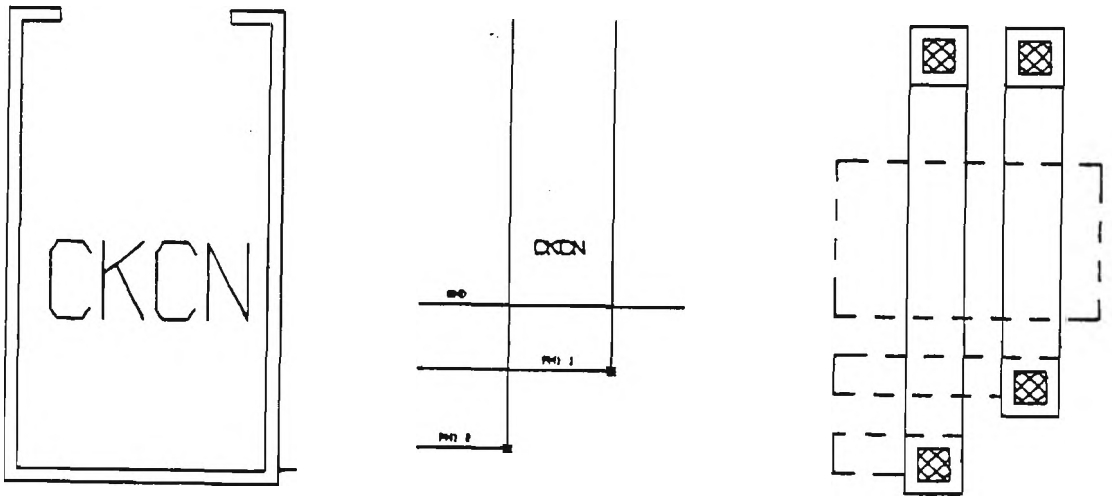


Figure 7-3: CKCN CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - VJR

Function - Extend right column wire beyond VBUS for connection to pad.

Placement Restrictions - Column : None
Row : Even
Over : Where needed

CIF Number -

Size Column : 1
Row : 2

Cell capacitance -

Cell Resistance -

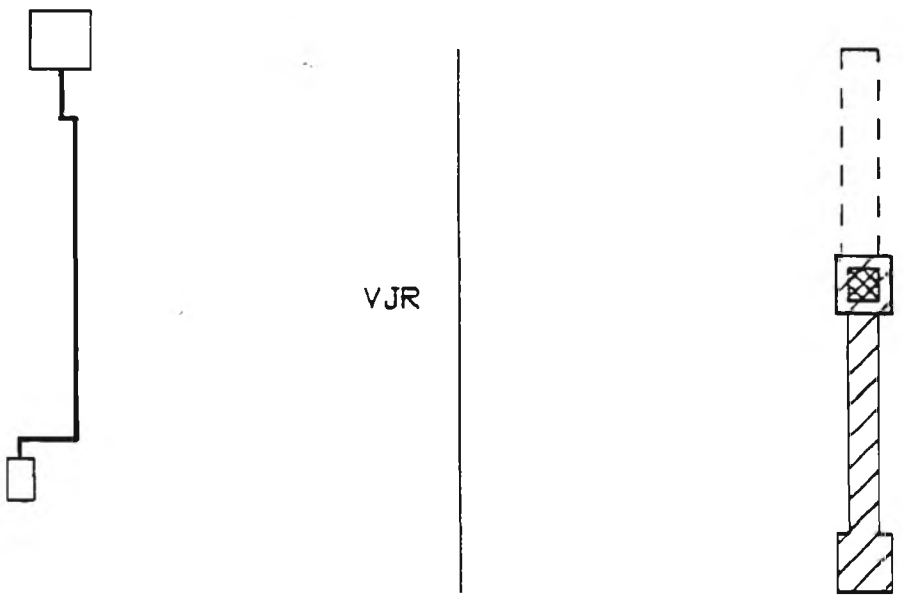


Figure 7-4: VJR CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - VJL

Function - Extend left column wire past VBUS for connection to pad.

Placement Restrictions - Column : None
Row : Even
Over : Where needed

CIF Number -

Size Column : 1
Row : 2

Cell capacitance -

Cell Resistance -

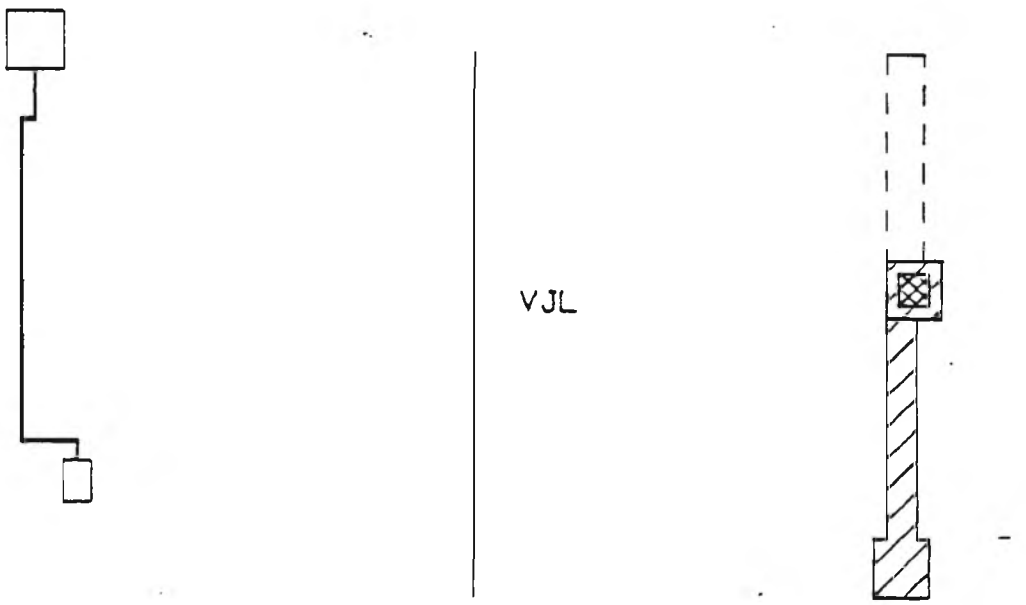


Figure 7-5: VJL CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - GJR

Function - Extend right column wire past GBUS for conection to pad.

Placement Restrictions - Column : None
Row : Odd
Under : Where needed

CIF Number -

Size Column : 1
Row : 2

Cell capacitance -

Cell resistance -

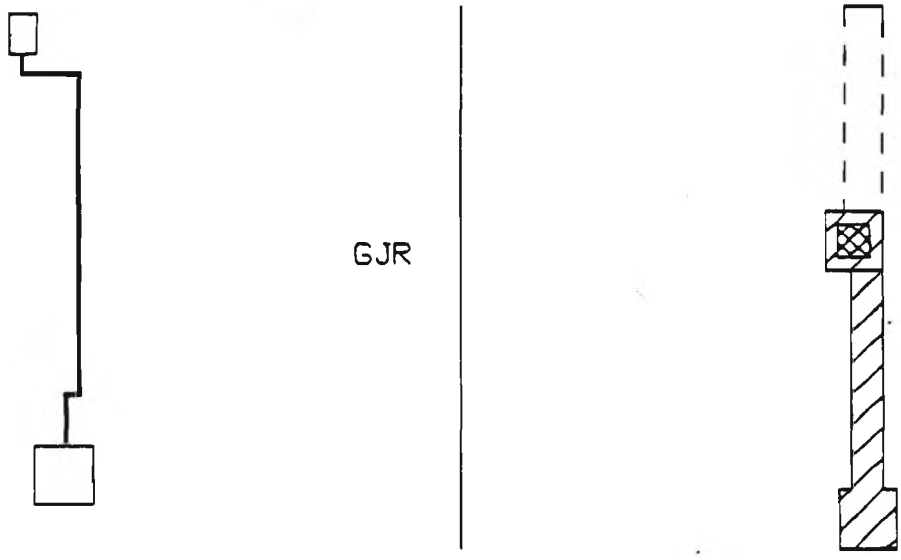


Figure 7-6: GJR CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - GJL

Function - Extend left column wire past GBUS for connection to pad.

Placement Restrictions - Column : None
Row : Odd
Under : Where needed

CIF Number -

Size Column : 1
Row : 2

Cell capacitance -

Cell resistance -

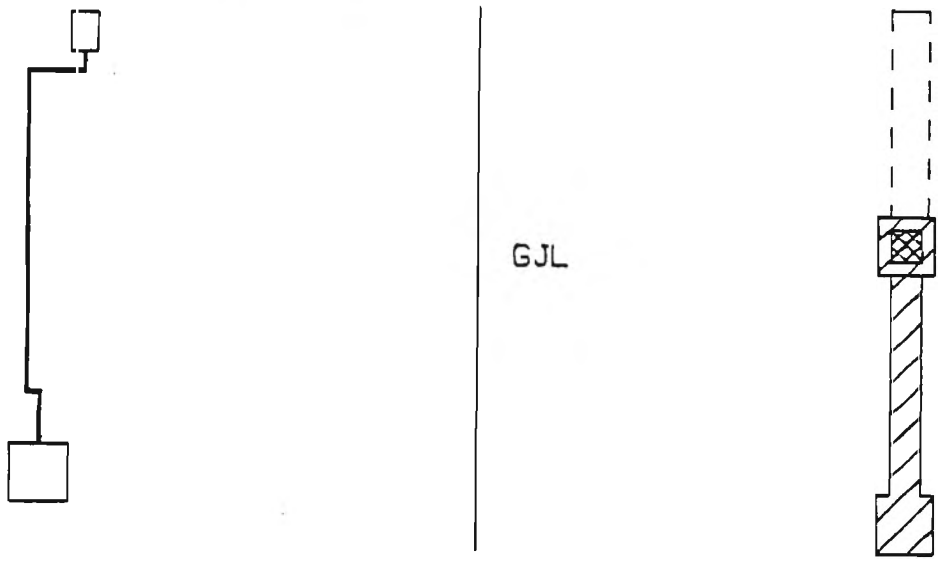


Figure 7-7: GJL CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - LCAP

Function - Supply clocks to right edge of circuit.

Placement Restrictions - Column : Even
Row : None
To side of : Complete circuit

CIF Number -

Size Column : 1
Row : 1

Cell capacitance -

Cell resistance -

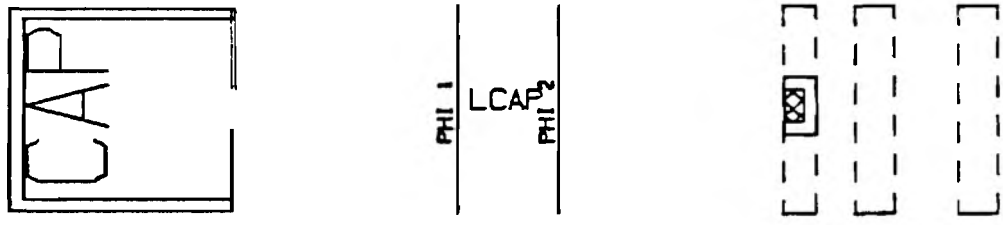


Figure 7-8: LCAP CELL GRAPHICS , SCHEMATIC AND COMPOSITE

BUSSING CELLS

Cell Name - RCAP

Function - Supply clocks to right edge of circuit.

Placement Restrictions - Column : Odd
Row : None
To side of : Complete circuit

CIF Number -

Size Column : 1
Row : 1

Cell capacitance -

Cell Resistance -

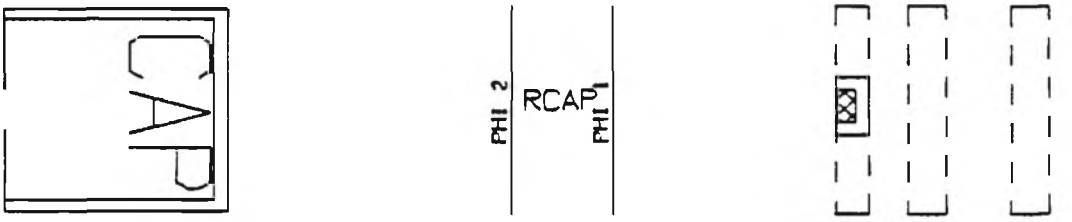


Figure 7-9: RCAP CELL GRAPHICS , SCHEMATIC AND COMPOSITE

8. PAD CELLS

The pad cells are intended to provide the connection from the PPL circuit to the external world and to define the boundary of the die which contains the circuit.

The cells are all a multiple of 6 mills in width with their origin in the middle of the pad, their left edge 3 mills from the origin and their right edge 3, 9 or 15 mills from the origin. At the top of each cell is a section of VDD and Ground buss, and at the bottom is a section of 5 mill wide scribe line. The top of the cell is about 7 mills from the origin and the bottom is 8 or 9 mills from the orign depending on the amount of overlap with the scribe line of the next die that is desired (1 or 2 mills).

Corner cells differ from the other Pad Cells in that they have scribe line on both the bottom and left sides. The distance from the origin to the left edge of a corner cell is 8 or 9 mills and the distance to the top is 9. The right edge is at a distance of 9 or 15 mills.

Pad cells are inserted on a 3 mill grid. The bottom and bottom left corner of the die are formed from Pad Cells inserted with A=0. The right edge and right bottom corner require A=90, the top and top right corner, A=180, and the left and top left corner, A=270.

The Pad cells consist of:

1. Input pads: BLKPAD, IPROPAD, IBUFPAD, and CIBUFPAD.

2. Output pads: BLKPAD, OBUFPAD, and COBUFPAD

3. Input and Output pads: OCBUFPAD

4. Power pads: VDDPAD and GNDPAD.

5. Fill pads: FILLPAD and CORNERPAD.

PAD CELLS

Cell Name - BLKPAD

Function - This cell consists of a pad with a metal leader. It may be used for either input or output were buffering and/or protection are not required.

Width - 12 mils

Placement Restrictions - Edge

CIF Number -

Graphics - Figure 8-1 on page 93

Schematic - Figure 8-2 on page 94

Composite - Figure 8-3 on page 95

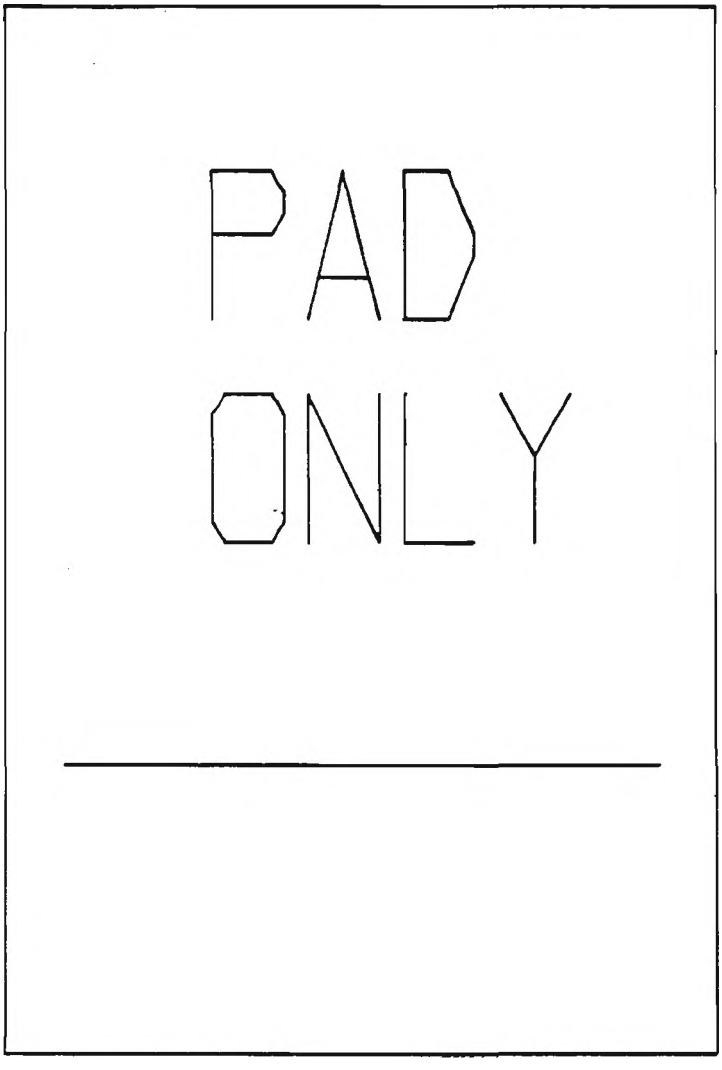


Figure 8-1: BLKPAD CELL GRAPHICS

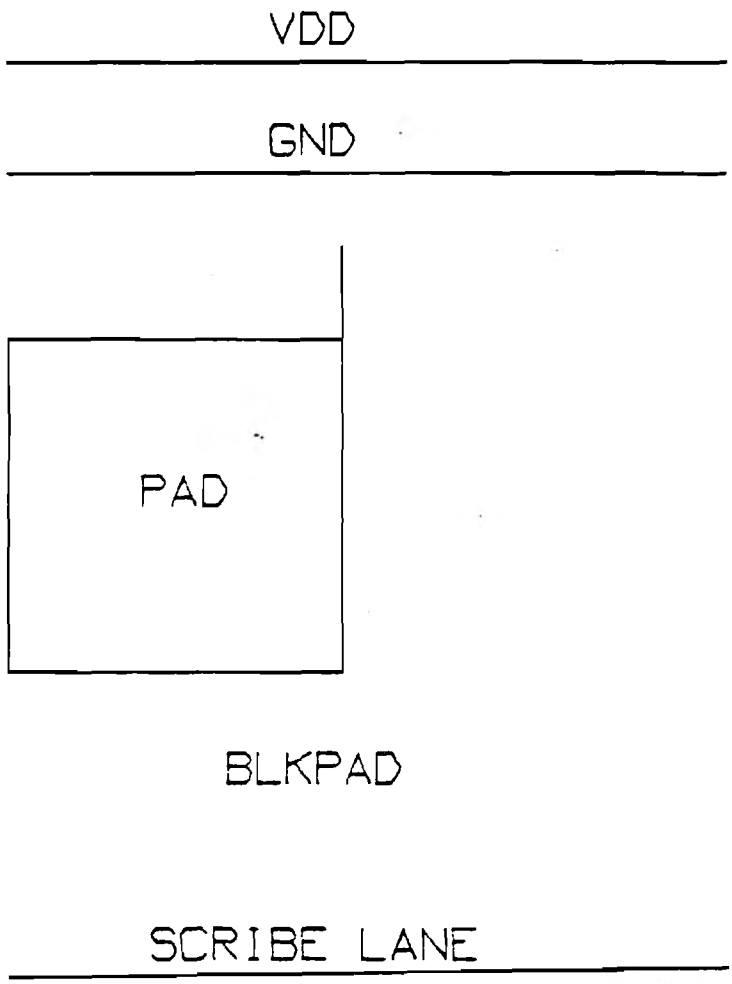


Figure 8-2: BLKPAD CELL SCHEMATIC

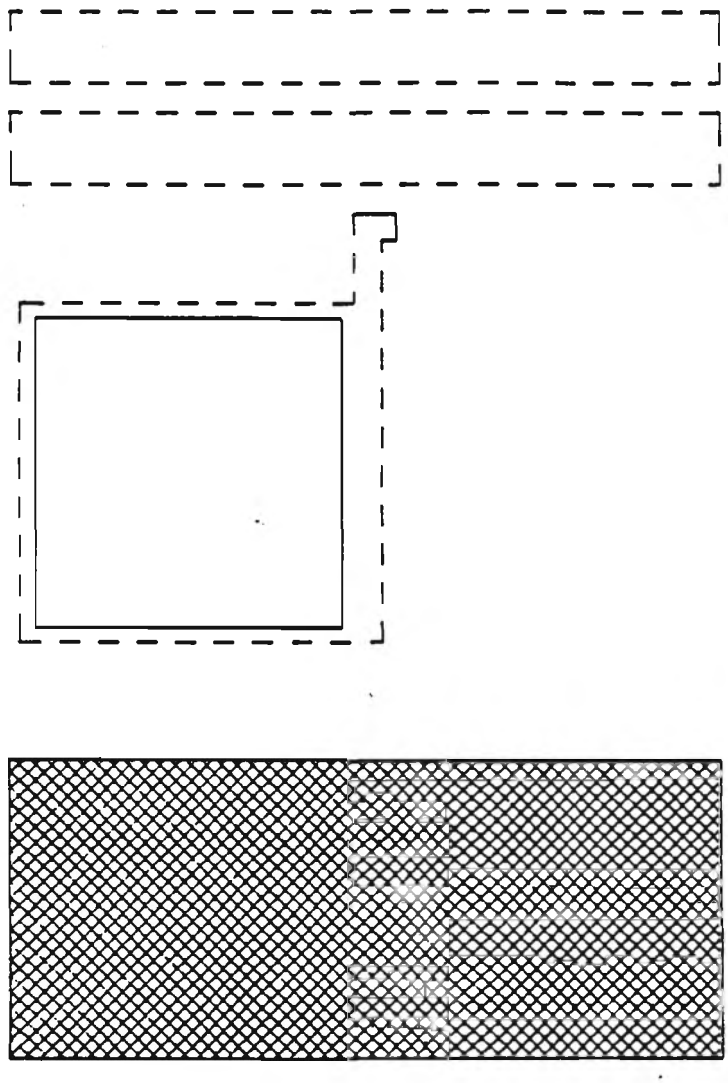


Figure 8-3: BLKPAD CELL COMPOSITE

PAD CELLS

Cell Name - IPROPAD

Function - This cell consists of a pad with an input protection device.

Width - 12 mils

Placement Restrictions - Edge

CIF Number -

Transistor size - 5 X .5 mill. or 120.5 X 6 micron

Graphics - Figure 8-4 on page 97

Schematic - Figure 8-5 on page 98

Composite - Figure 8-6 on page 99

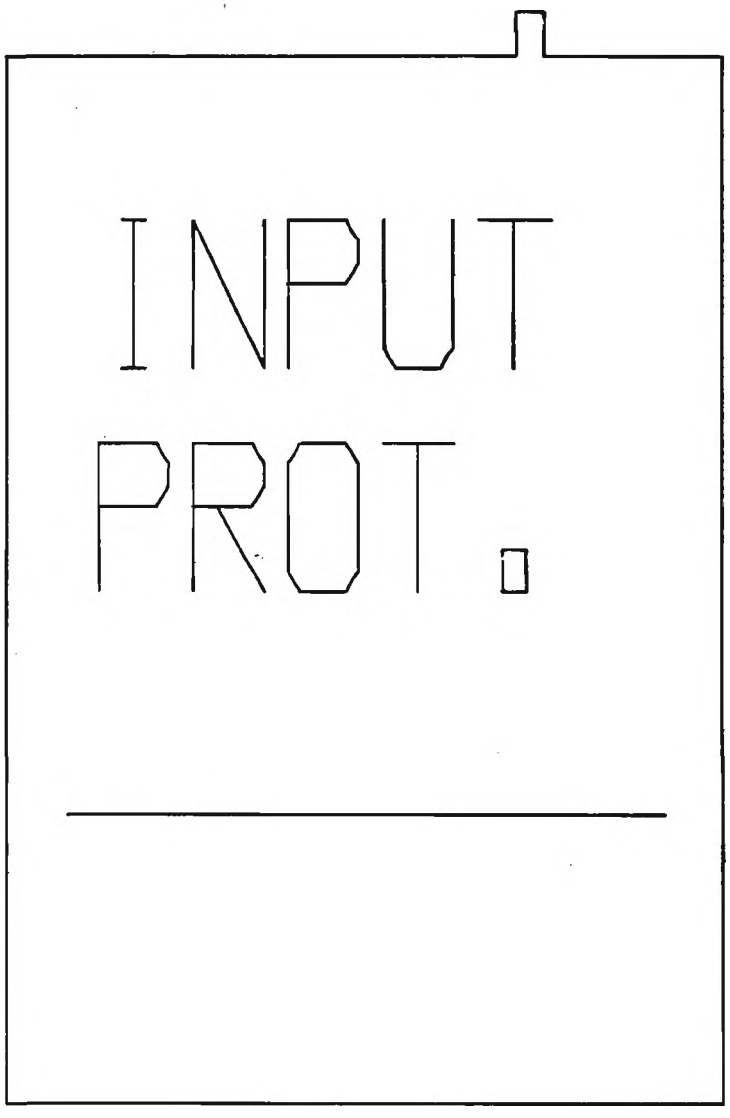


Figure 8-4: IPROPAD CELL GRAPHICS

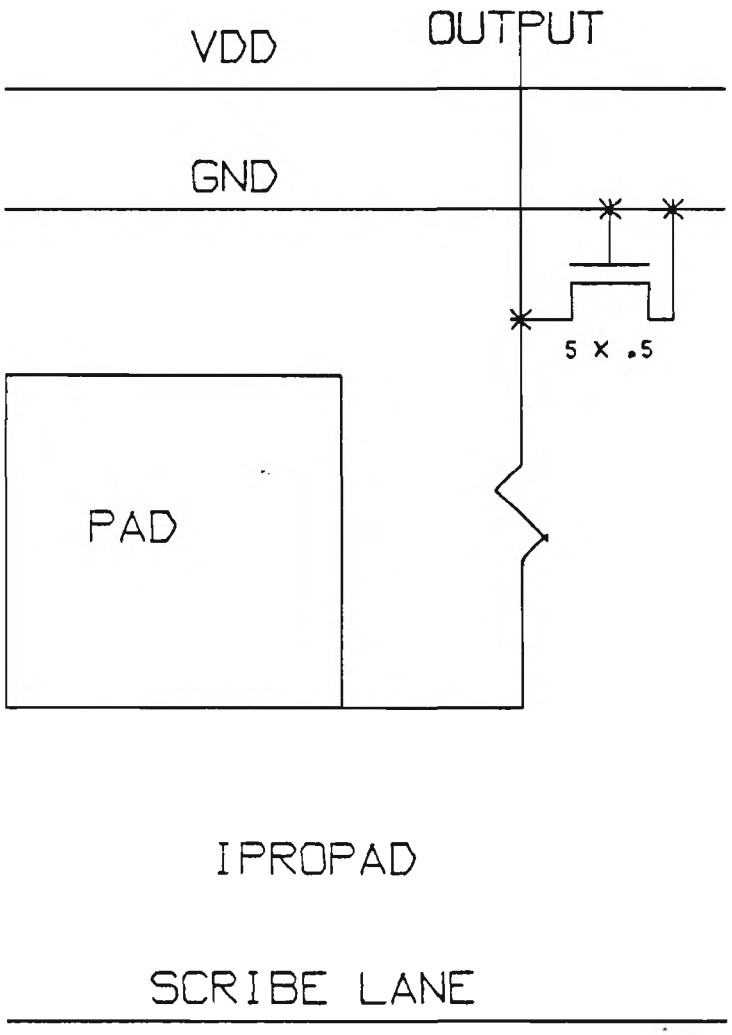


Figure 8-5: IPROPAD CELL SCHEMATIC

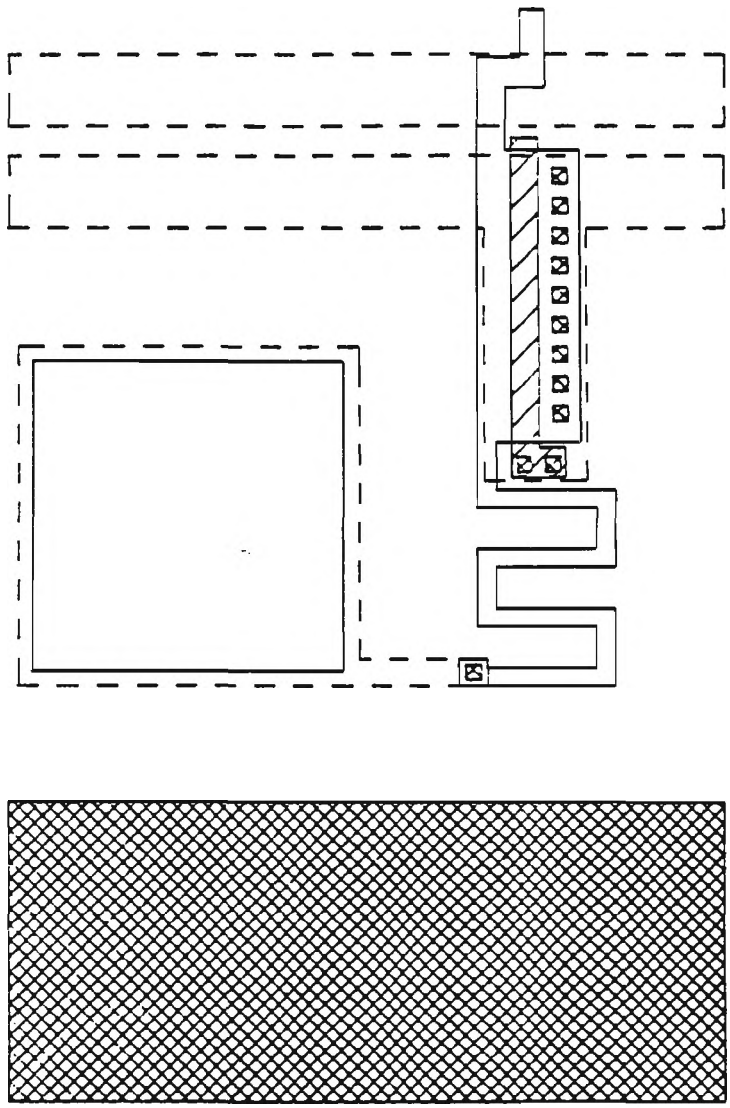


Figure 8-6: IPROPAD CELL COMPOSITE

PAD CELLS

Cell Name - IBUFPAD

Function - This cell consists of pad with input protection and an inverting input buffer.

Width - 12 mils

Placement Restrictions - Edge

CIF Number -

Transistor sizes - Q1=.25 X .25 mill. or 6 X 6 micron
Q2=2 X .25 mill. or 48 X 6 micron
Q3=5 X .5 mill. or 120.5 X 6 micron

Graphics - Figure 8-7 on page 101

Schematic - Figure 8-8 on page 102

Composite - Figure 8-9 on page 103

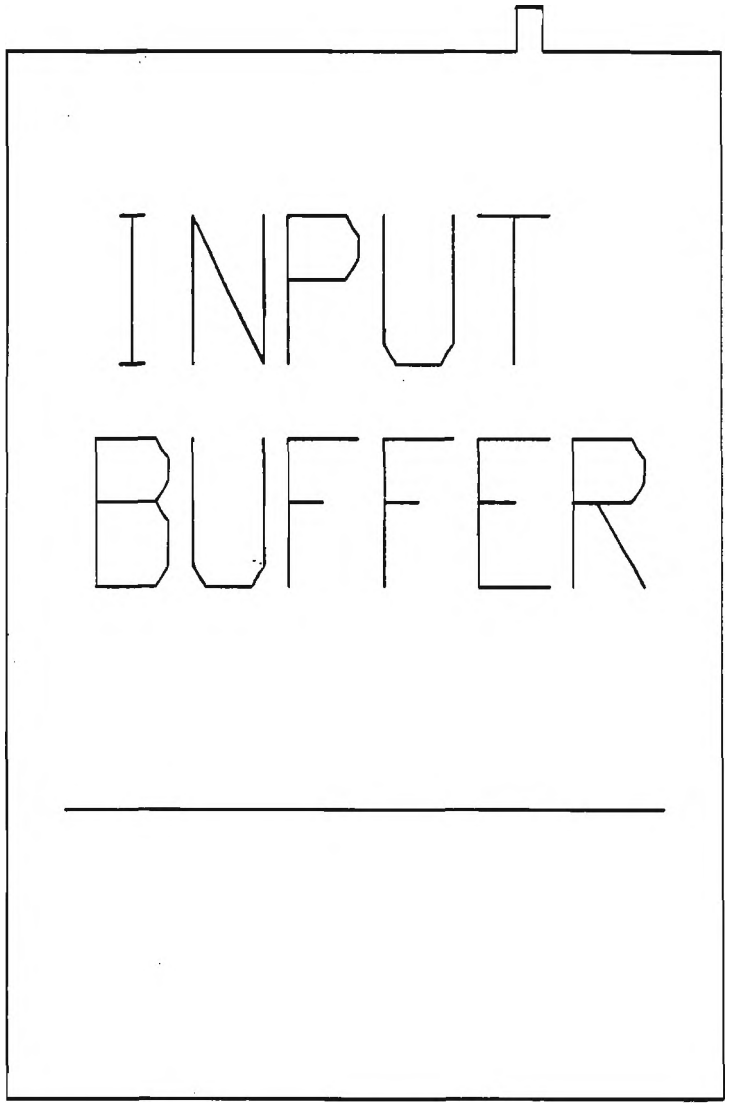


Figure 8-7: IBUFPAD CELL GRAPHICS

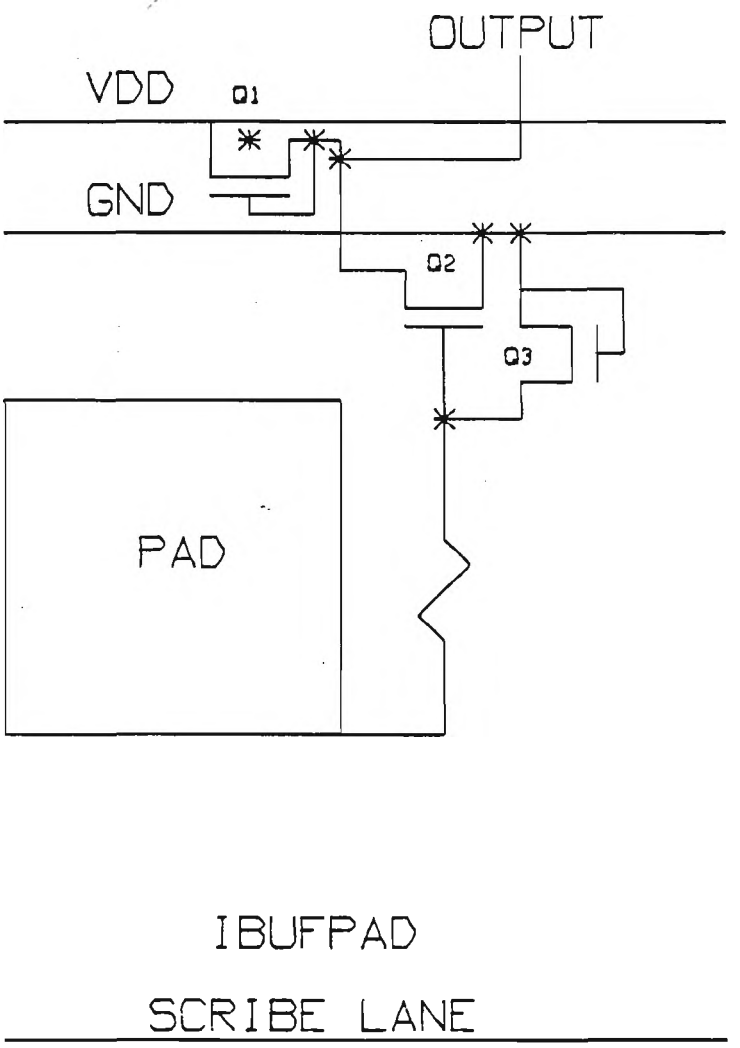


Figure 8-8: IBUFPAD CELL SCHEMATIC

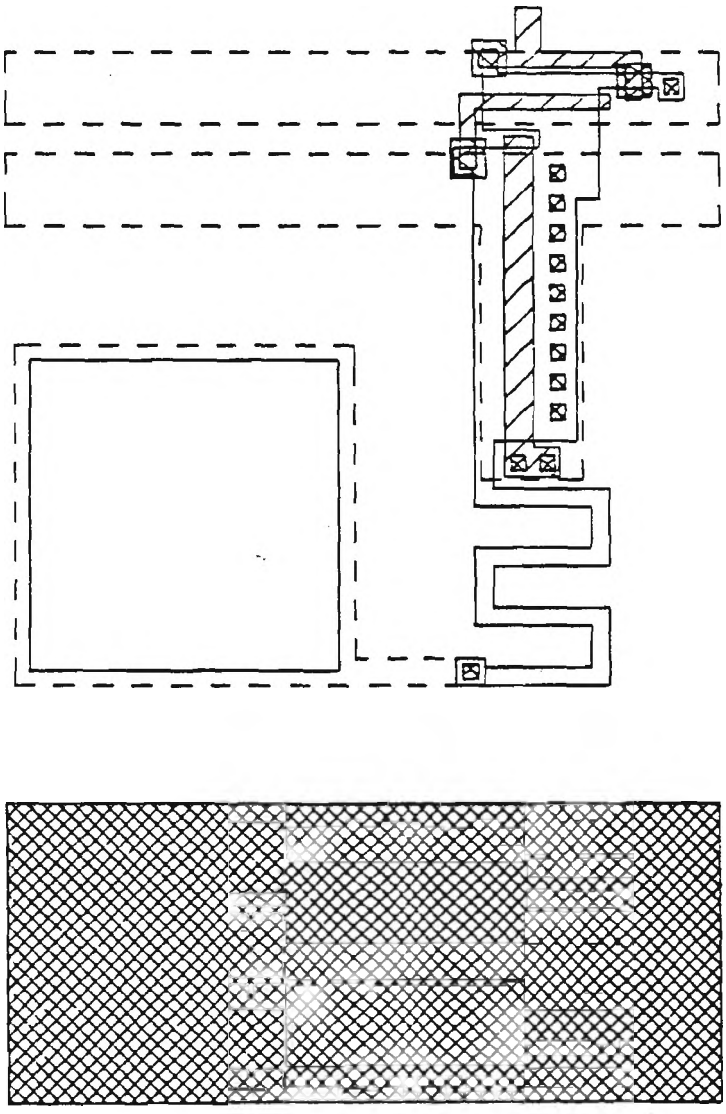


Figure 8-9: IBUFPAD CELL COMPOSITE

PAD CELLS

Cell Name - CIBUFPAD

Function - Identical to the IBUFPAD cell except for corner placement.

Width - 17 or 18 mils

Placement Restrictions - Corner

CIF Number -

Transistor sizes - Q1=.25 X .25 mill. or 6 X 6 micron
Q2=2 X .25 mill. or 48 X 6 micron
Q3=5 X .5 mill. or 120.5 X 6 micron

Graphics - Figure 8-10 on page 105

Schematic - Figure 8-11 on page 106

Composite - Figure 8-12 on page 107

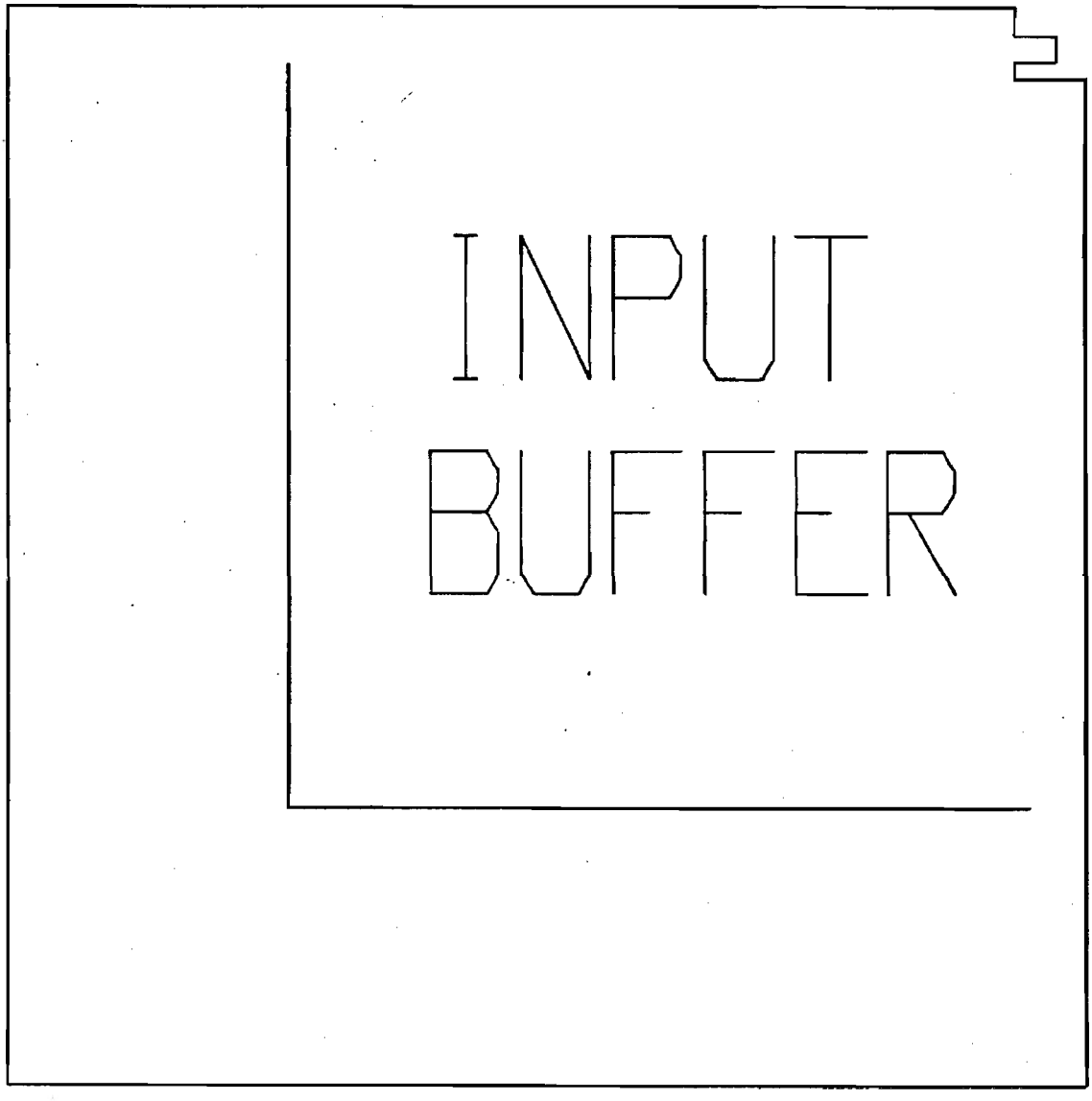


Figure 8-10: CIBUFPAD CELL GRAPHICS

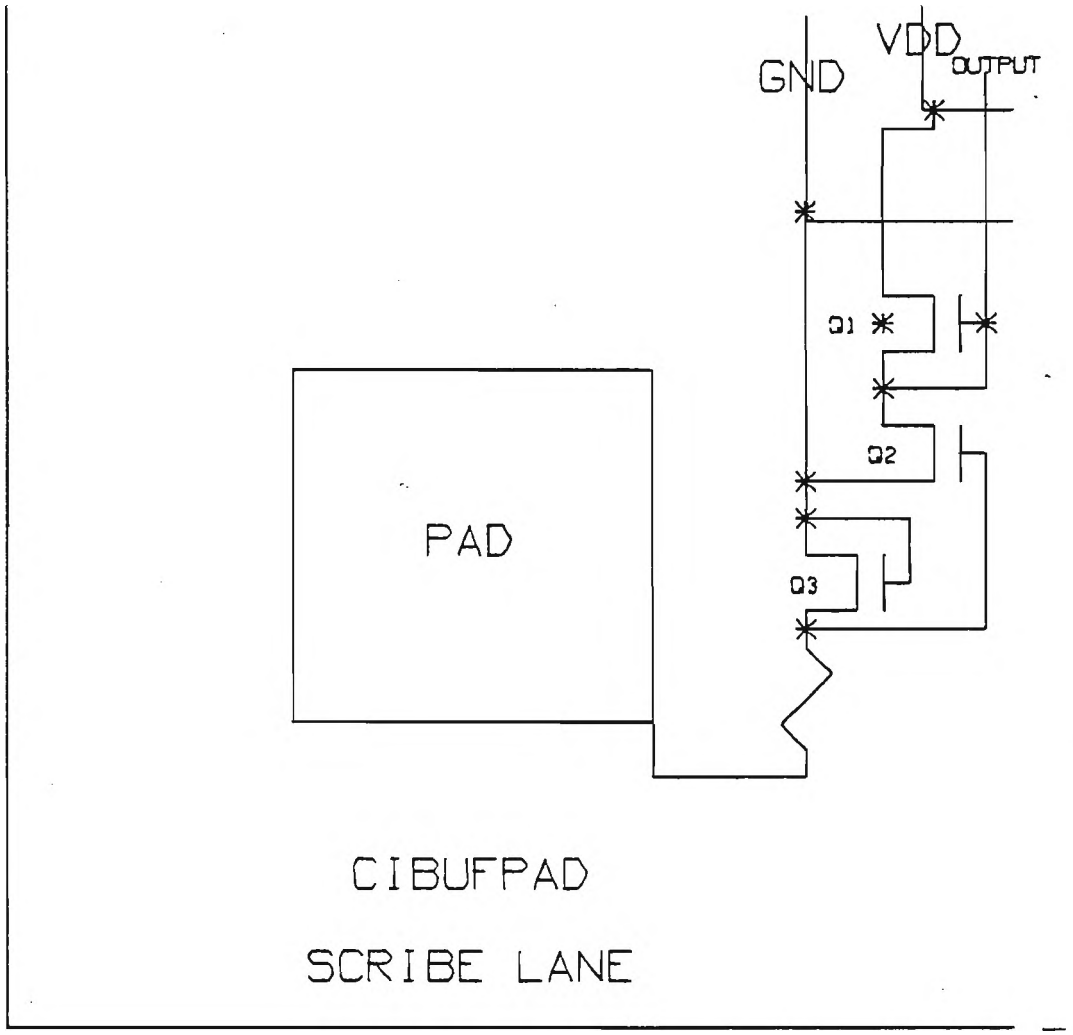


Figure 8-11: CIBUFPAD CELL SCHEMATIC

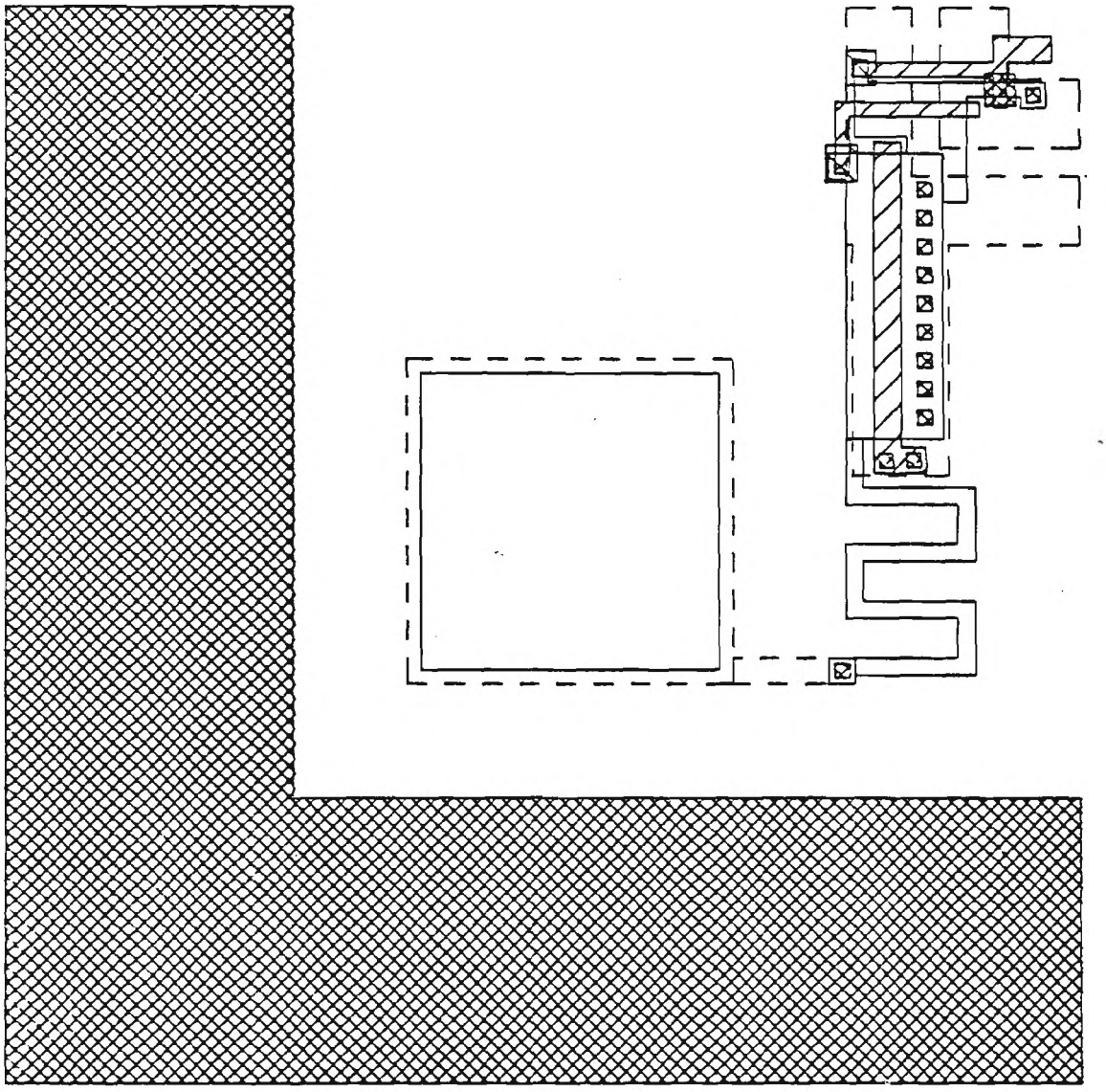


Figure 8-12: CIBUFPAD CELL COMPOSITE

PAD CELLS

Cell Name - OBUFPAD

Function - This cell consists of a pad driven by an inverting output superbuffer. The output is TTL compatable and is capable of driving one standard load.

Width - 18 mils

Placement Restrictions - Edge

CIF Number -

Transistor sizes - Q1=.25 X .25 mill. or 6 X 6 micron
Q2=.25 X .25 mill. or 6 X 6 micron
Q3=13.7 X .25 mill. or 258 X 6 micron
Q4=1 X .25 mill. or 24 X 6 micron
Q5=1 X .25 mill. or 24 X 6 micron
Q6=11.15 X .25 mill. or 199.5 X 6 micron

Graphics - Figure 8-13 on page 109

Schematic - Figure 8-14 on page 110

Composite - Figure 8-15 on page 111

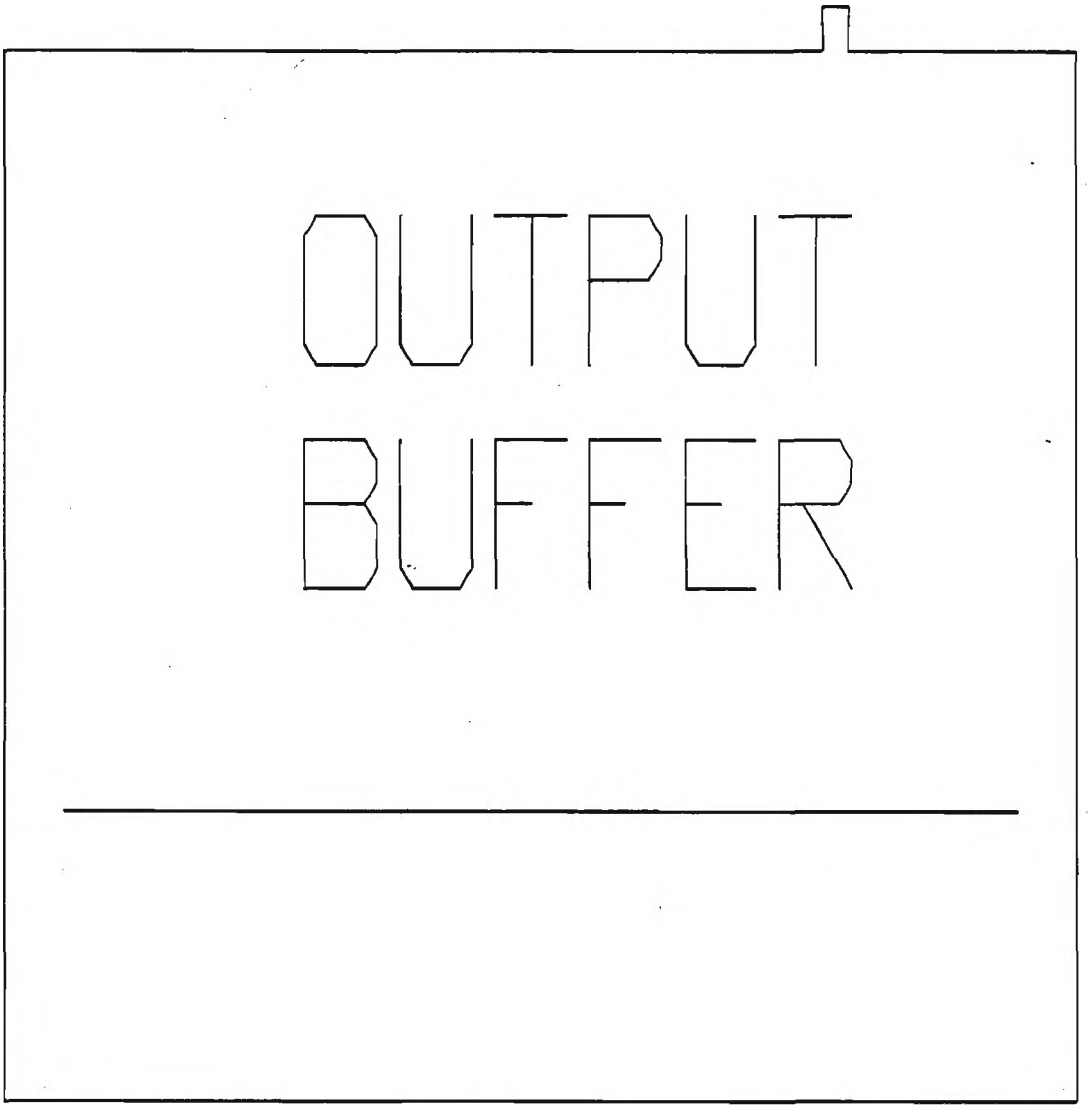


Figure 8-13: OBUFPAD CELL GRAPHICS

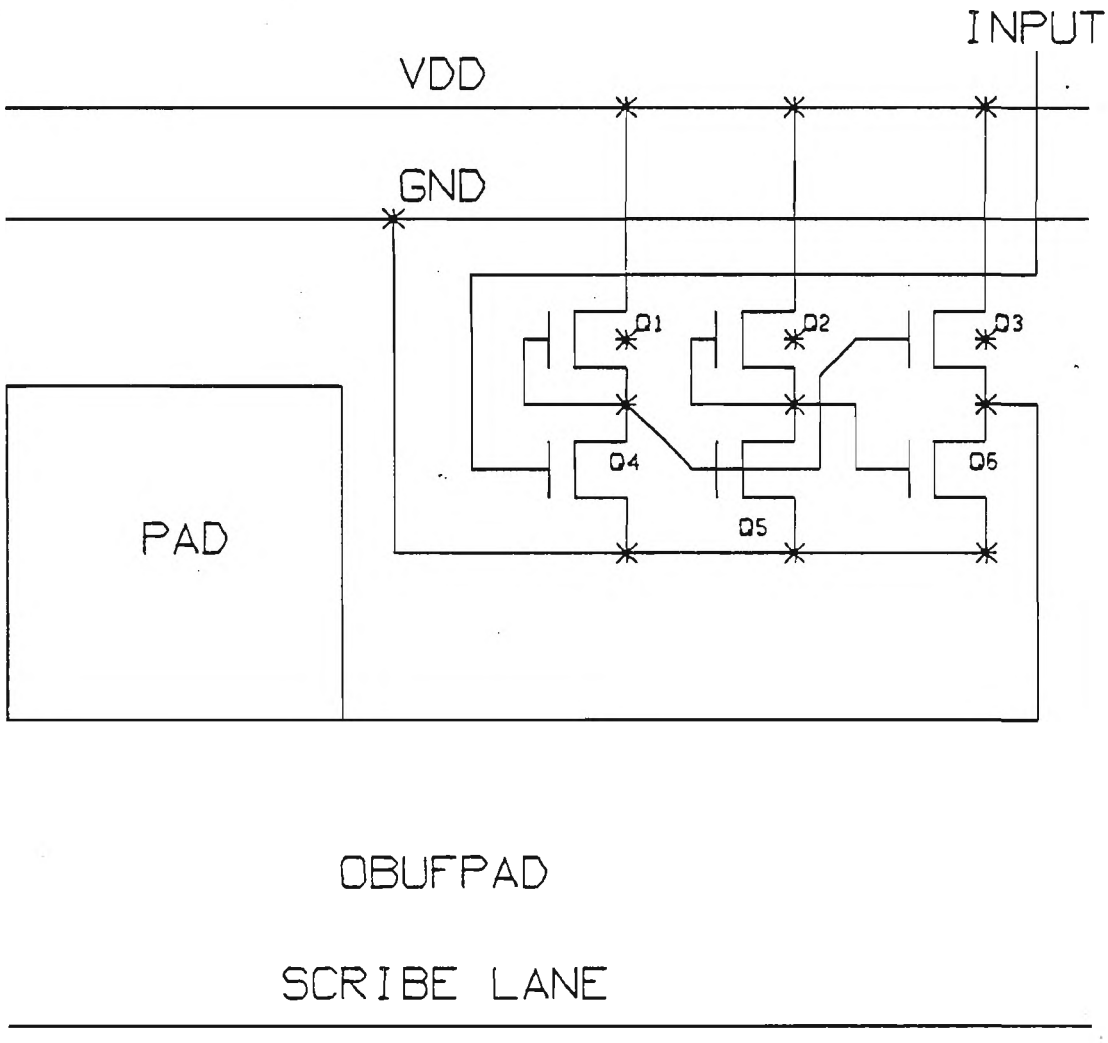


Figure 8-14: OBUFPAD CELL SCHEMATIC

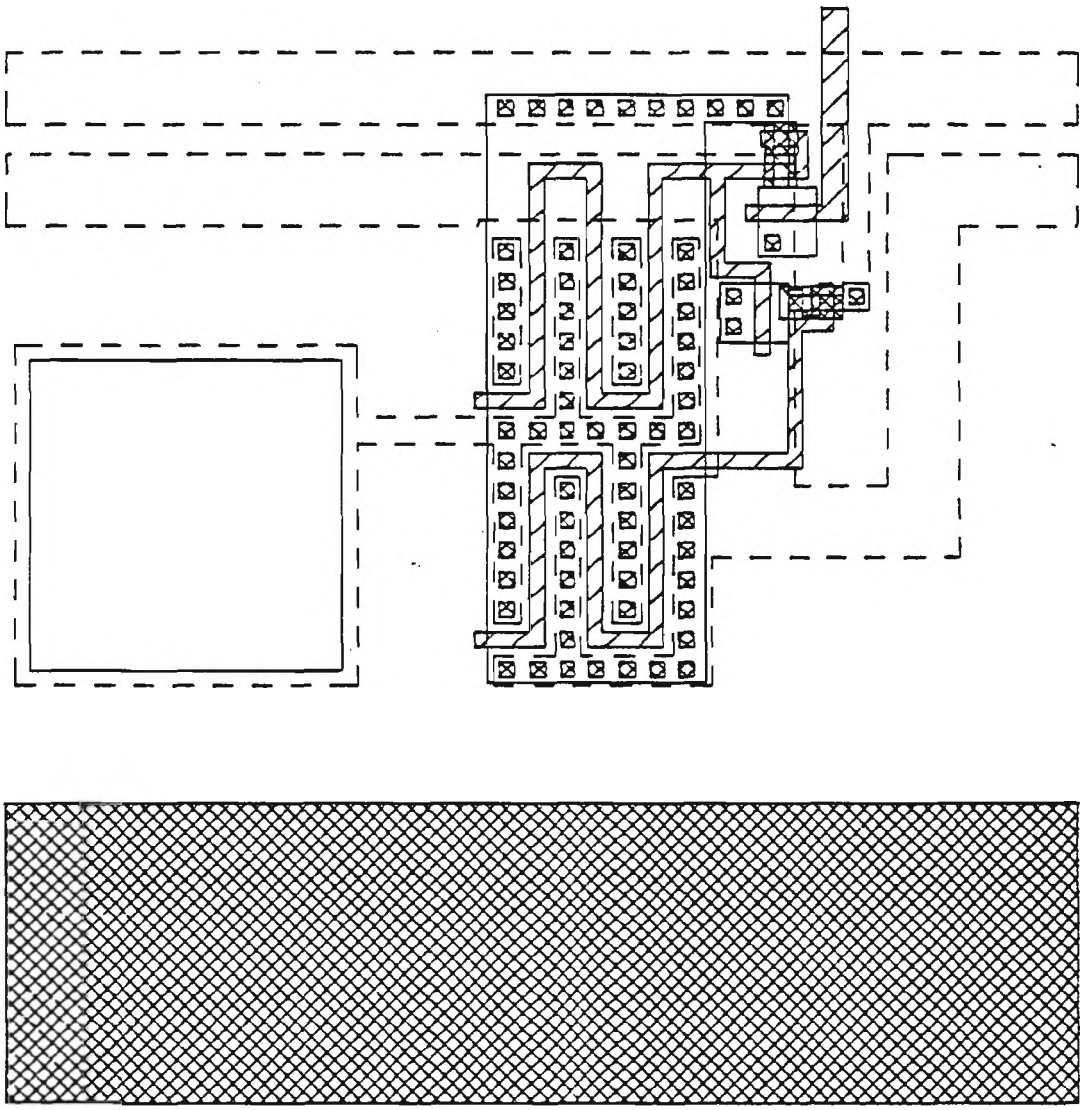


Figure 8-15: OBUFPAD CELL COMPOSITE

PAD CELLS

Cell Name - COBUFPAD

Function - Identical to OBUFPAD except for corner placemant.

Width - 23 or 24 mils

Placement Restrictions - Corner

CIF Number -

Transistor sizes - Q1=.25 X .25 mill. or 6 X 6 micron
Q2=.25 X .25 mill. or 6 X 6 micron
Q3=13.7 X .25 mill. or 258 X 6 micron
Q4=1 X .25 mill. or 24 X 6 micron
Q5=1 X .25 mill. or 24 X 6 micron
Q6=11.15 X .25 mill. or 199.5 X 6 micron

Graphics - Figure 8-16 on page 113

Schematic - Figure 8-17 on page 114

Composite - Figure 8-18 on page 115

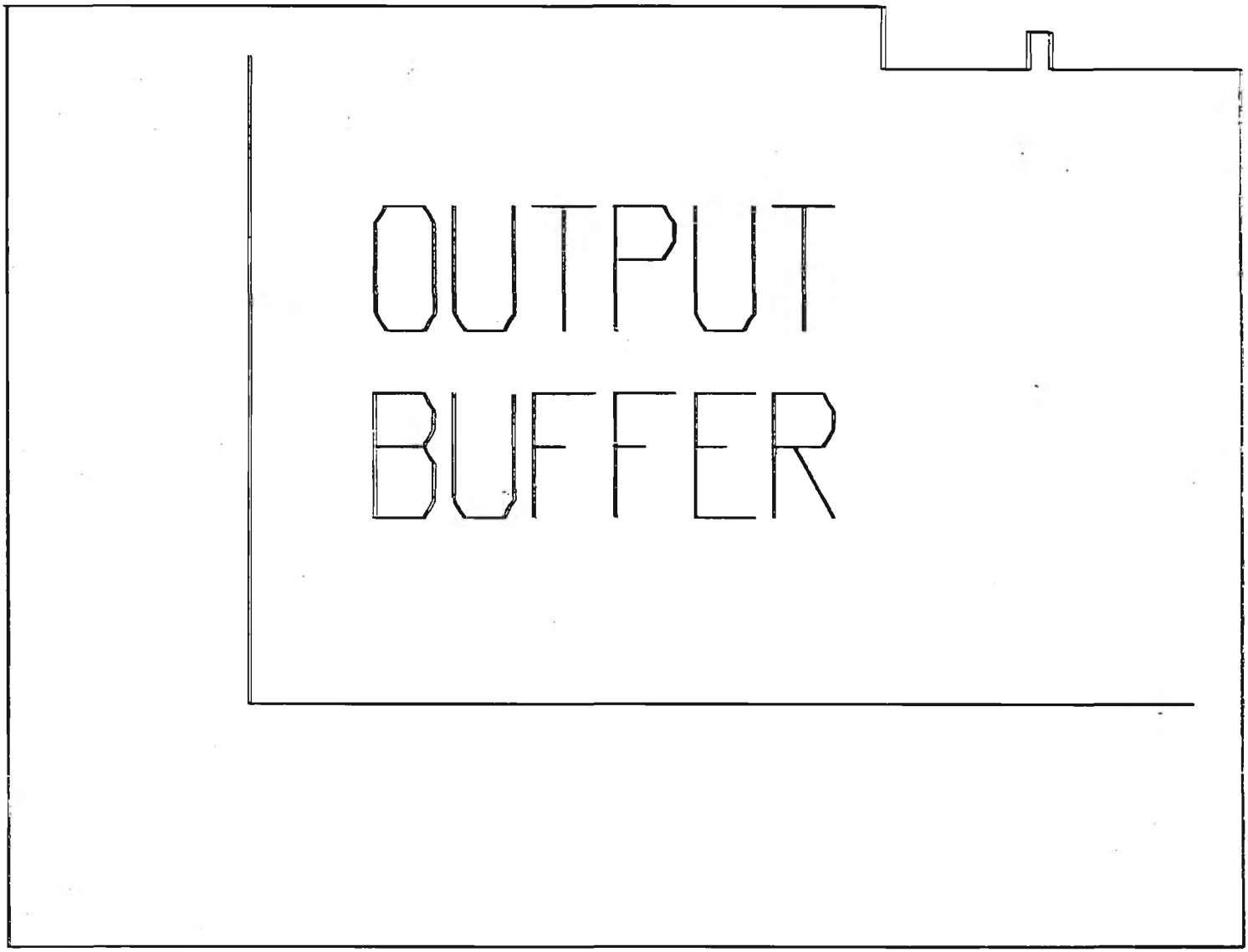


Figure 8-16: COBUFPAD CELL GRAPHICS

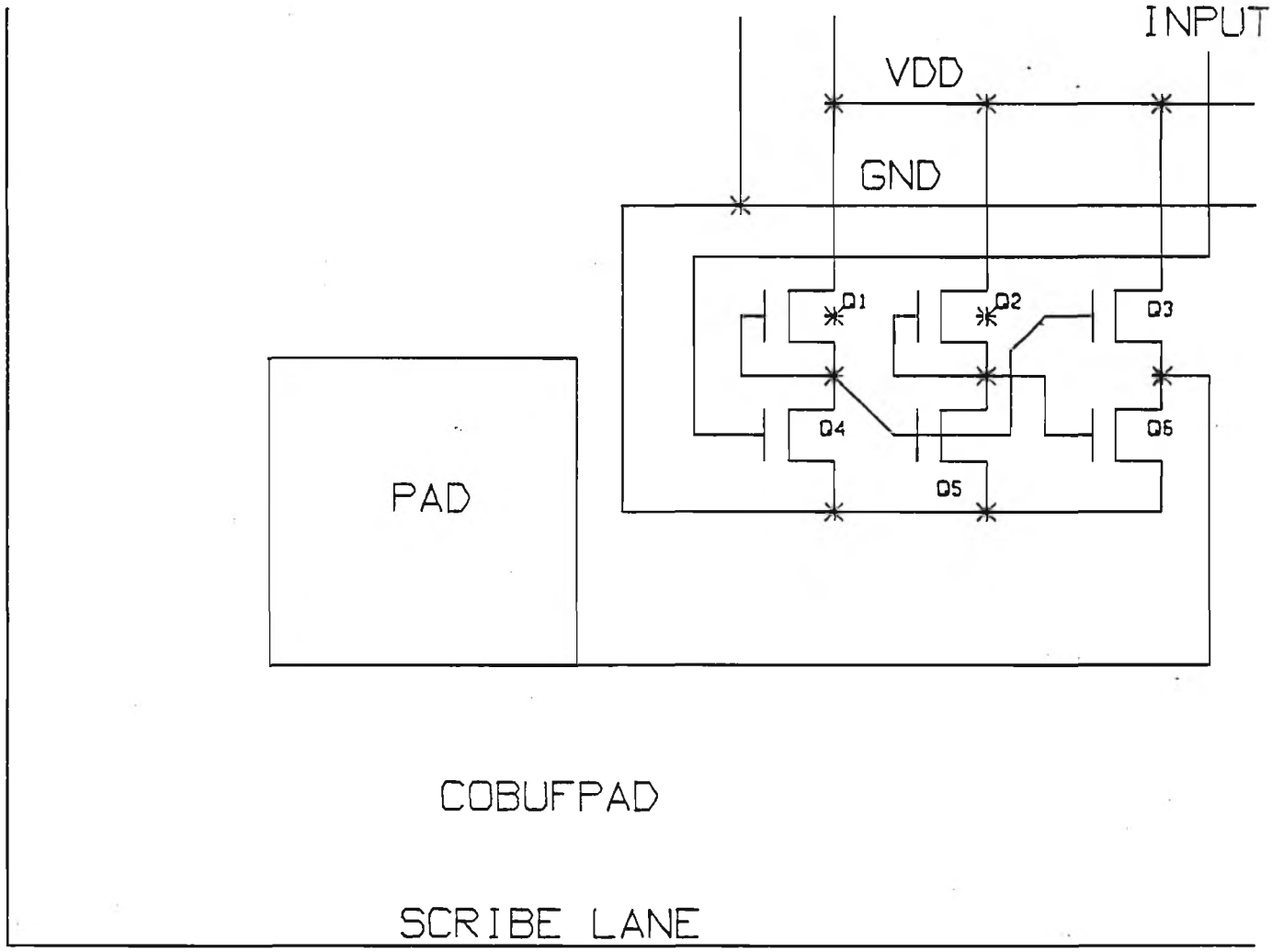


Figure 8-17: COBUFPAD CELL SCHEMATIC

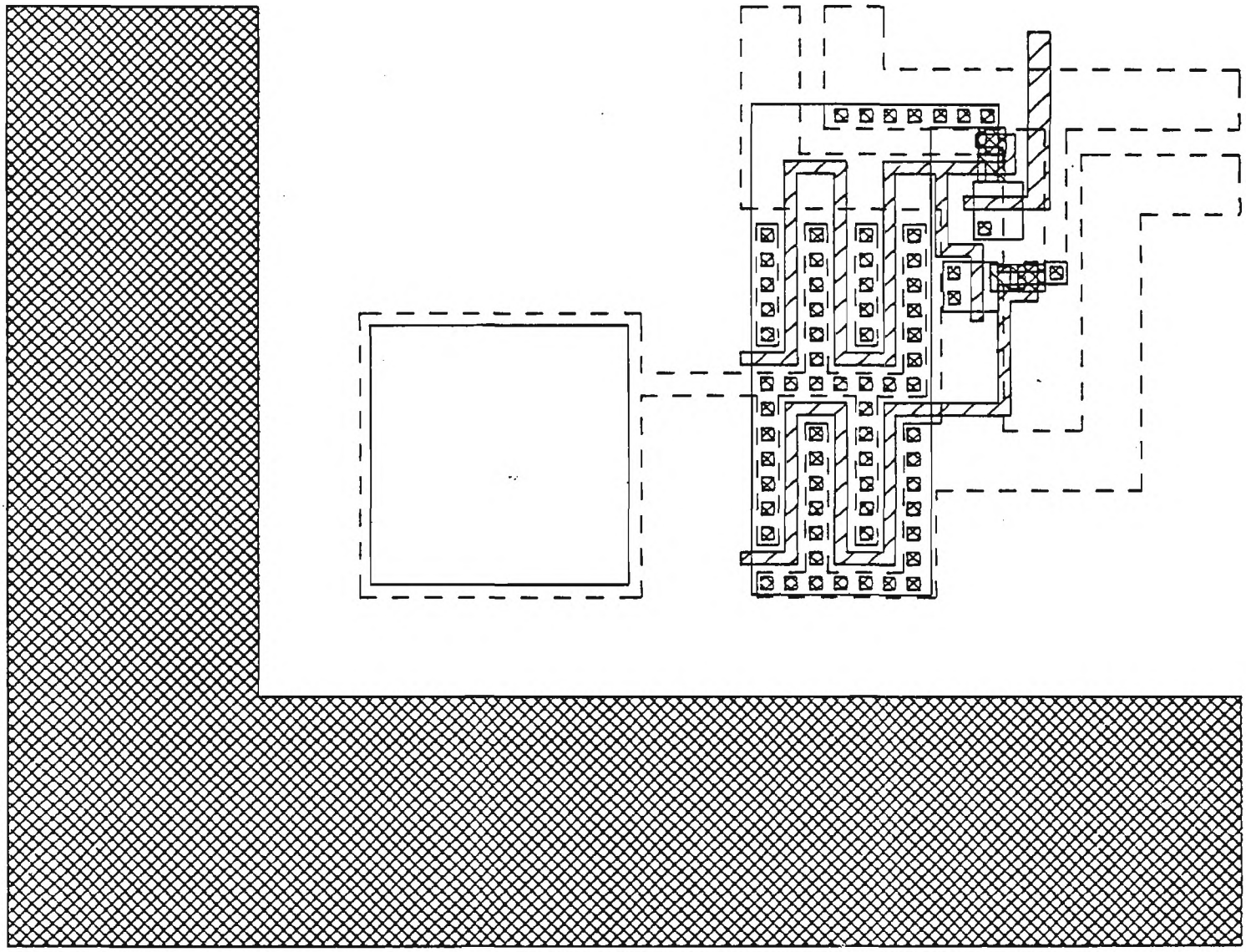


Figure 8-18: COBUFPAD CELL COMPOSITE

PAD CELLS

Cell Name - OCBUFPAD

Function - This pad is an open drain input-output pad with selectable pullup. The pad is driven by an inverting, open drain buffer. A selectable pullup is provided by a depletion load connected to the enhancement driver through a pass transistor. The gate of the pass transisitor should be tied high to enable the pullup and tied low to disable it. With the pullup enabled, the driver is TTL compatable and will drive 1 standard load. Input from the pad is through the standard inverting input driver. There is no input protection.

Width - 18 Mills.

Placement Restrictions - Edge.

CIF Number -

Transistor sizes - Q1=.25 X .5 mill.
Q2=1 X .25 mill.
Q3=.25 X .25 mill.
Q4=.5 X .25 mill.
Q5=.25 X .25 mill.
Q6=1 X .25 mill.
Q7=3 X .25 mill.
Q8=3.65 X .25 mill.
Q9=15.8 X .25 mill.

Graphics - Figure 8-19 on page 117

Schematic - Figure 8-20 on page 118

Composite - Figure 8-21 on page 119

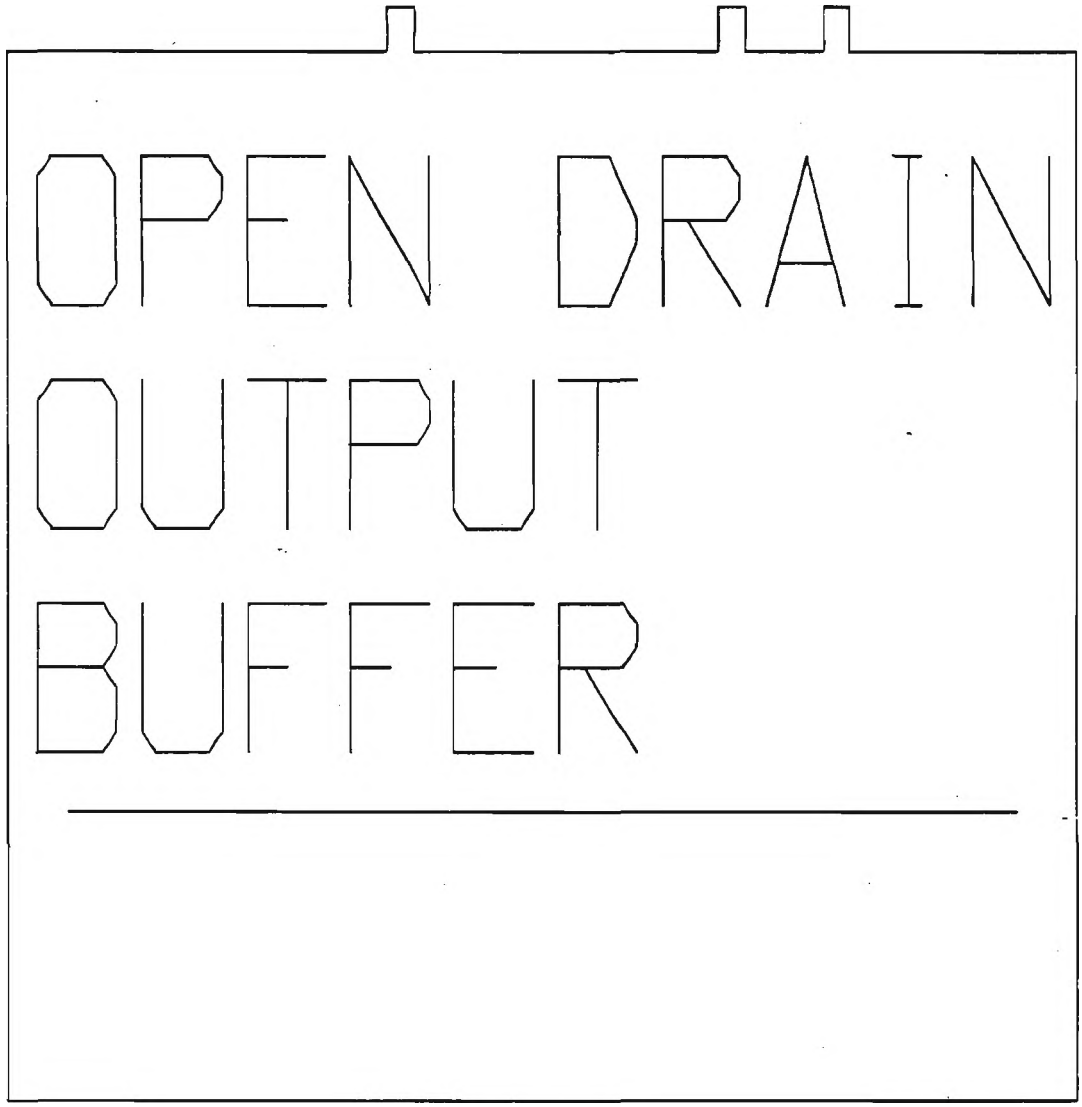


Figure 8-19: OCBUFPAD CELL GRAPHICS

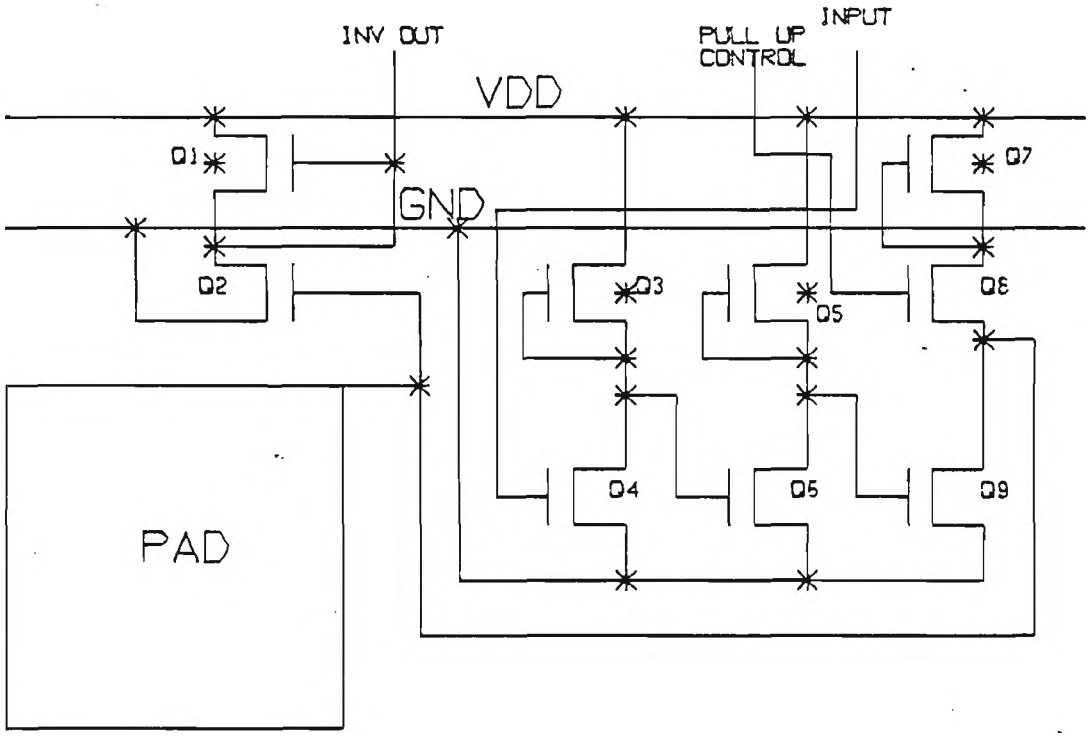


Figure 8-20: OCBUFPAD CELL SCHEMATIC

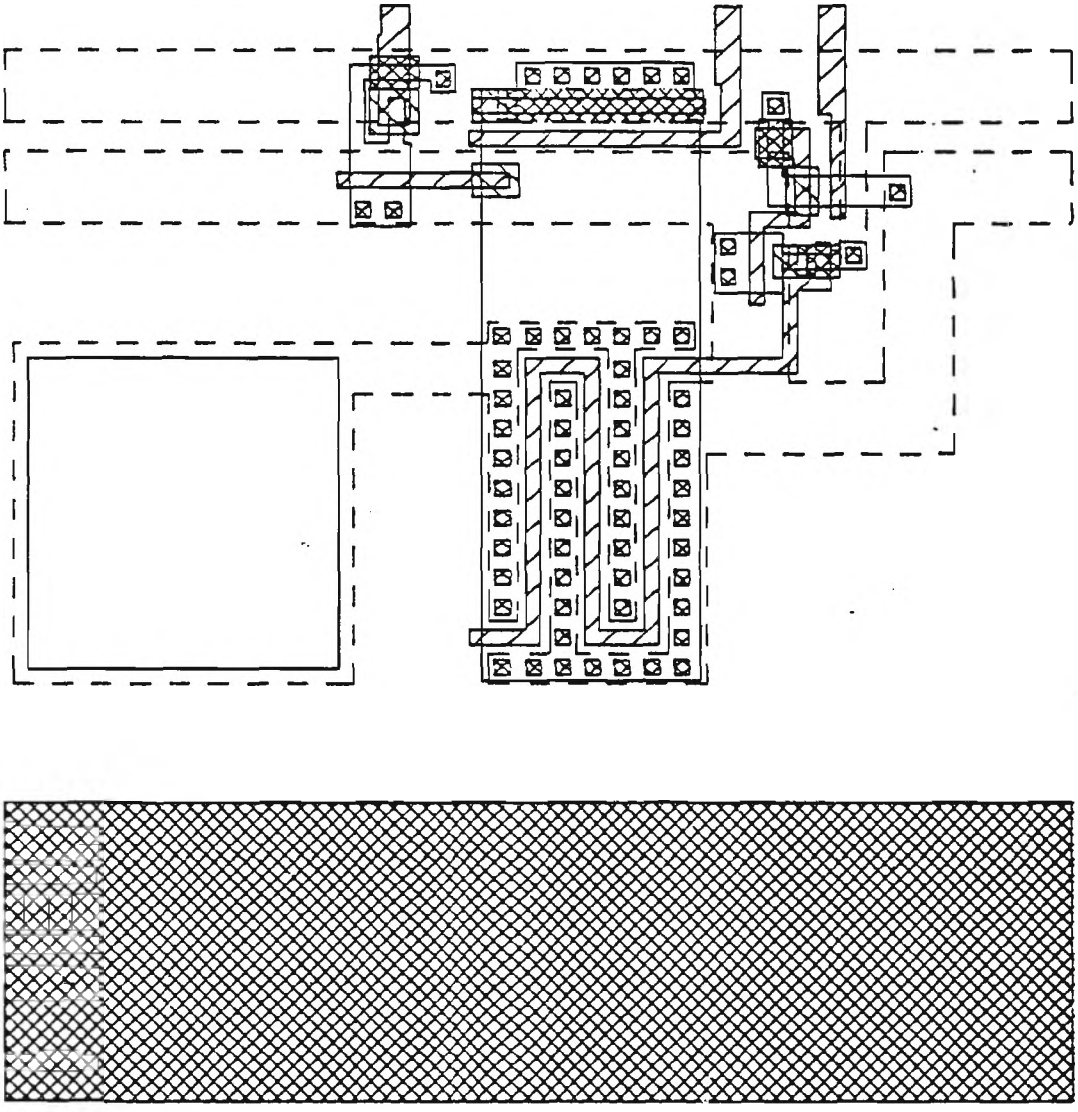


Figure 8-21: OCBUFPAD CELL COMPOSITE

PAD CELLS

Cell Name - VDDPAD

Function - This cell consists of a pad connected to the Vdd (inner) buss. The Ground buss is interupted by this cell.

Width - 17 or 18 mils

Placement Restrictions - Corner

CIF Number -

Graphics - Figure 8-22 on page 121

Schematic - Figure 8-23 on page 122

Composite - Figure 8-24 on page 123

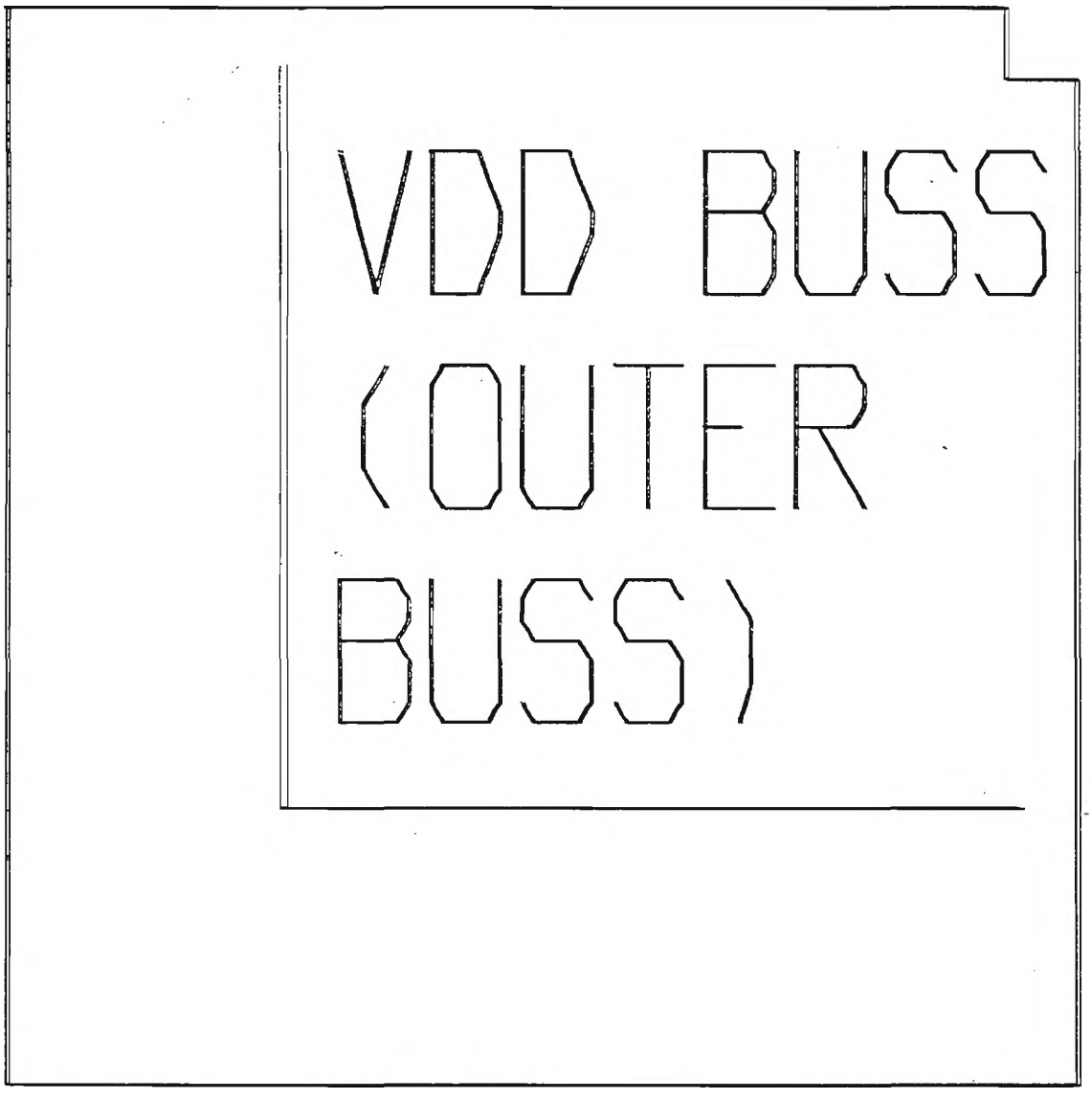


Figure 8-22: VDDPAD CELL GRAPHICS

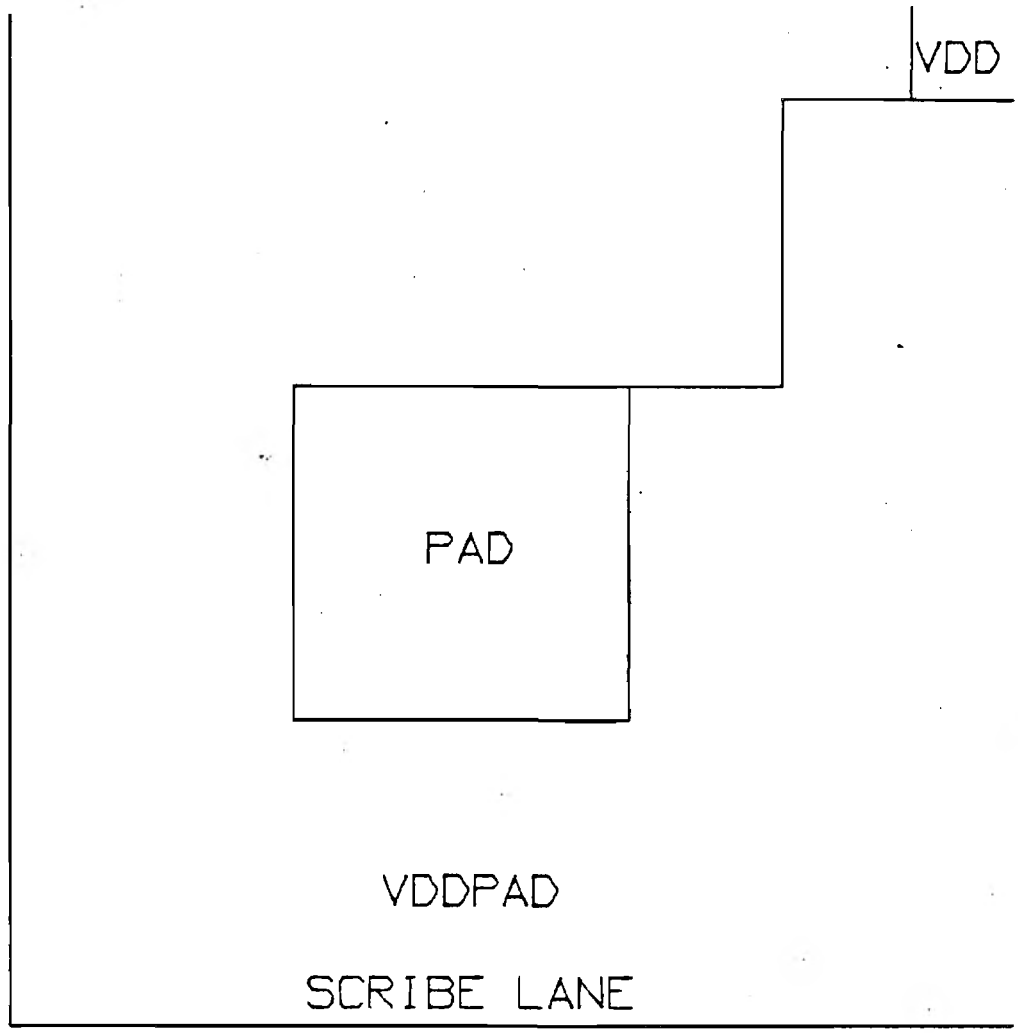


Figure 8-23: VDDPAD CELL SCHEMATIC

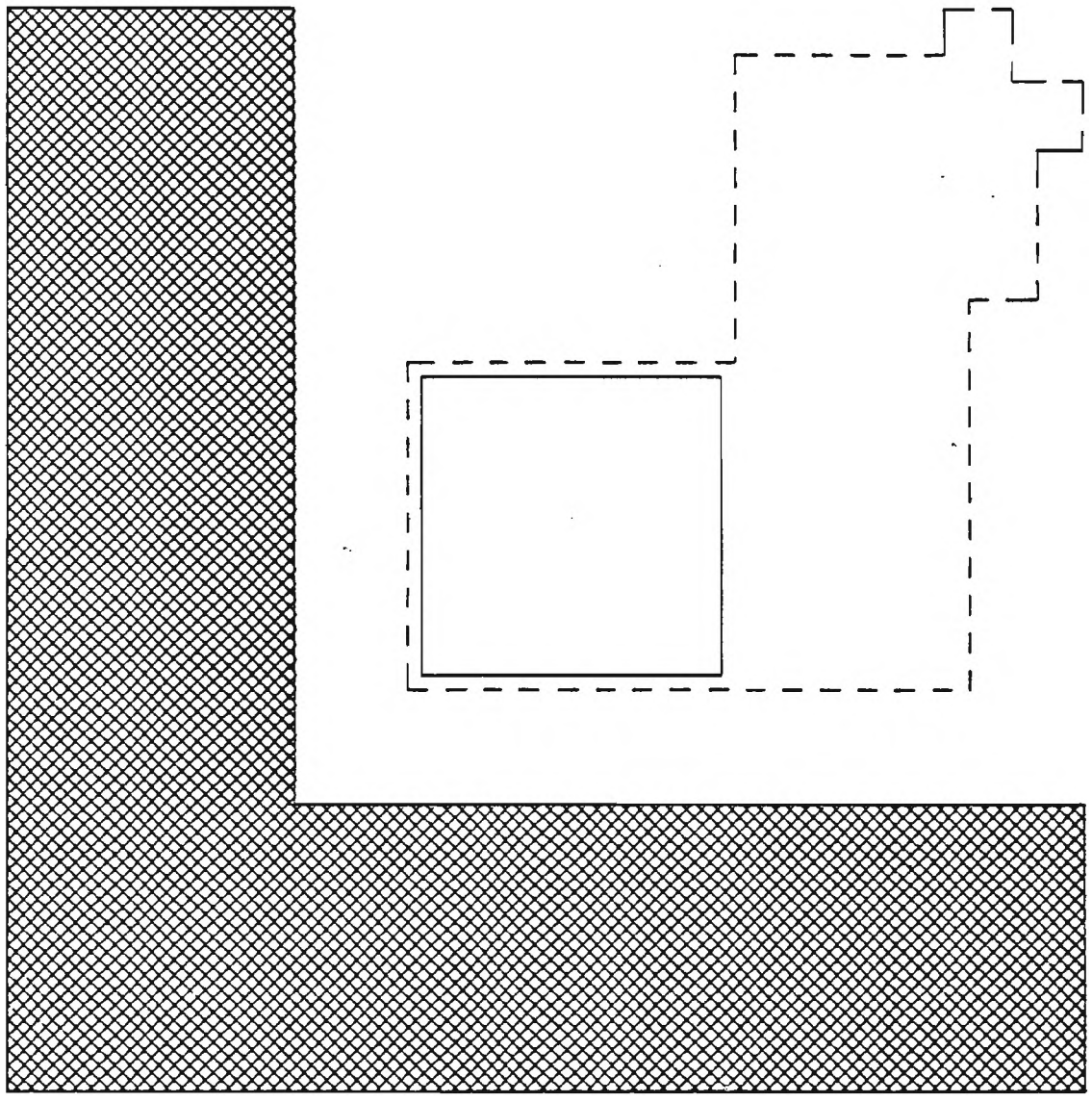


Figure 8-24: VDDPAD CELL COMPOSITE

PAD CELLS

Cell Name - GNDPAD

Function - This cell consists of a pad connected to the Ground (inner) buss. The Vdd buss is interupted by this cell

Width - 23 or 24 mils

Placement Restrictions - Corner

CIF Number -

Graphics - Figure 8-25 on page 125

Schematic - Figure 8-26 on page 126

Composite - Figure 8-27 on page 127

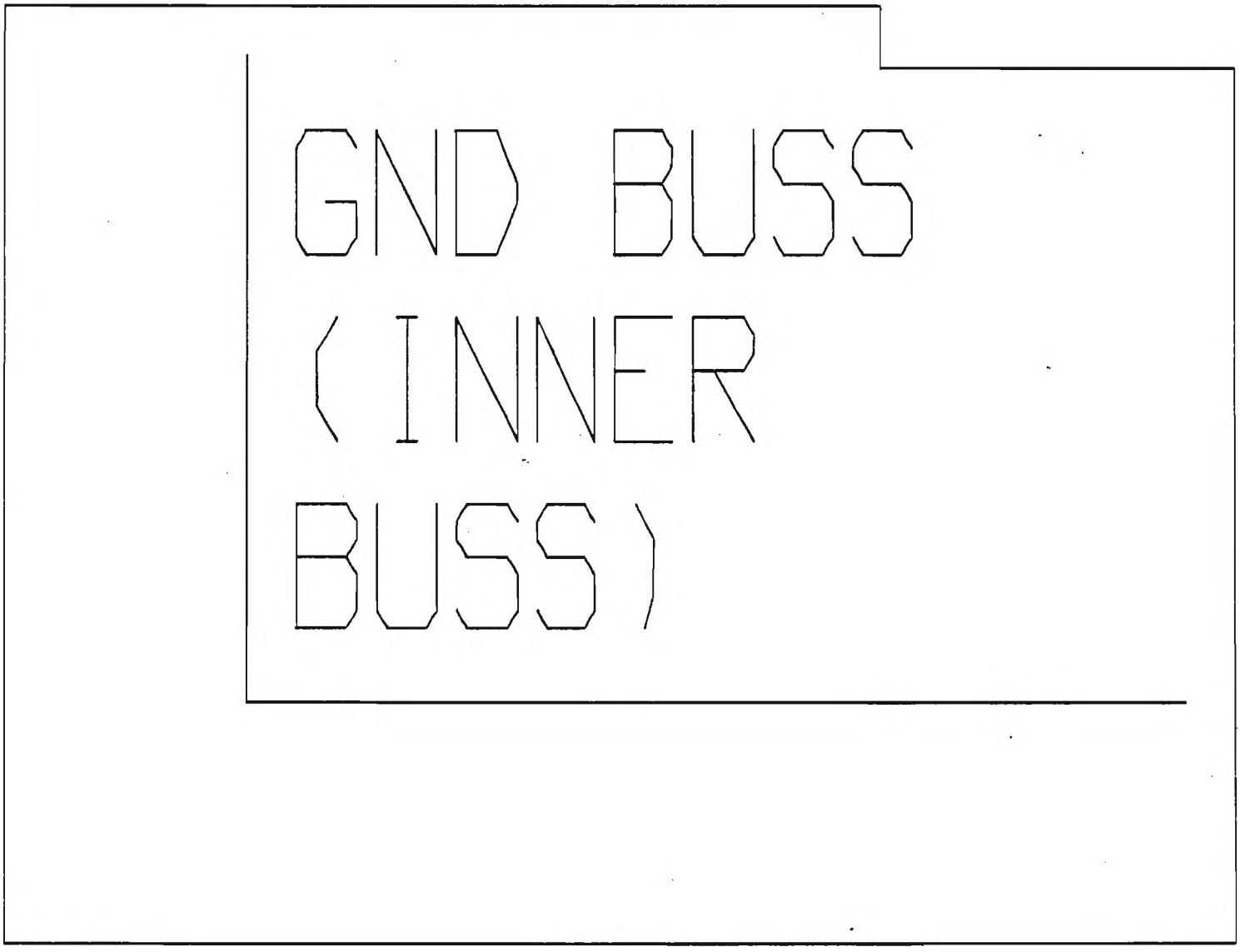


Figure 8-25: GNDPAD CELL GRAPHICS

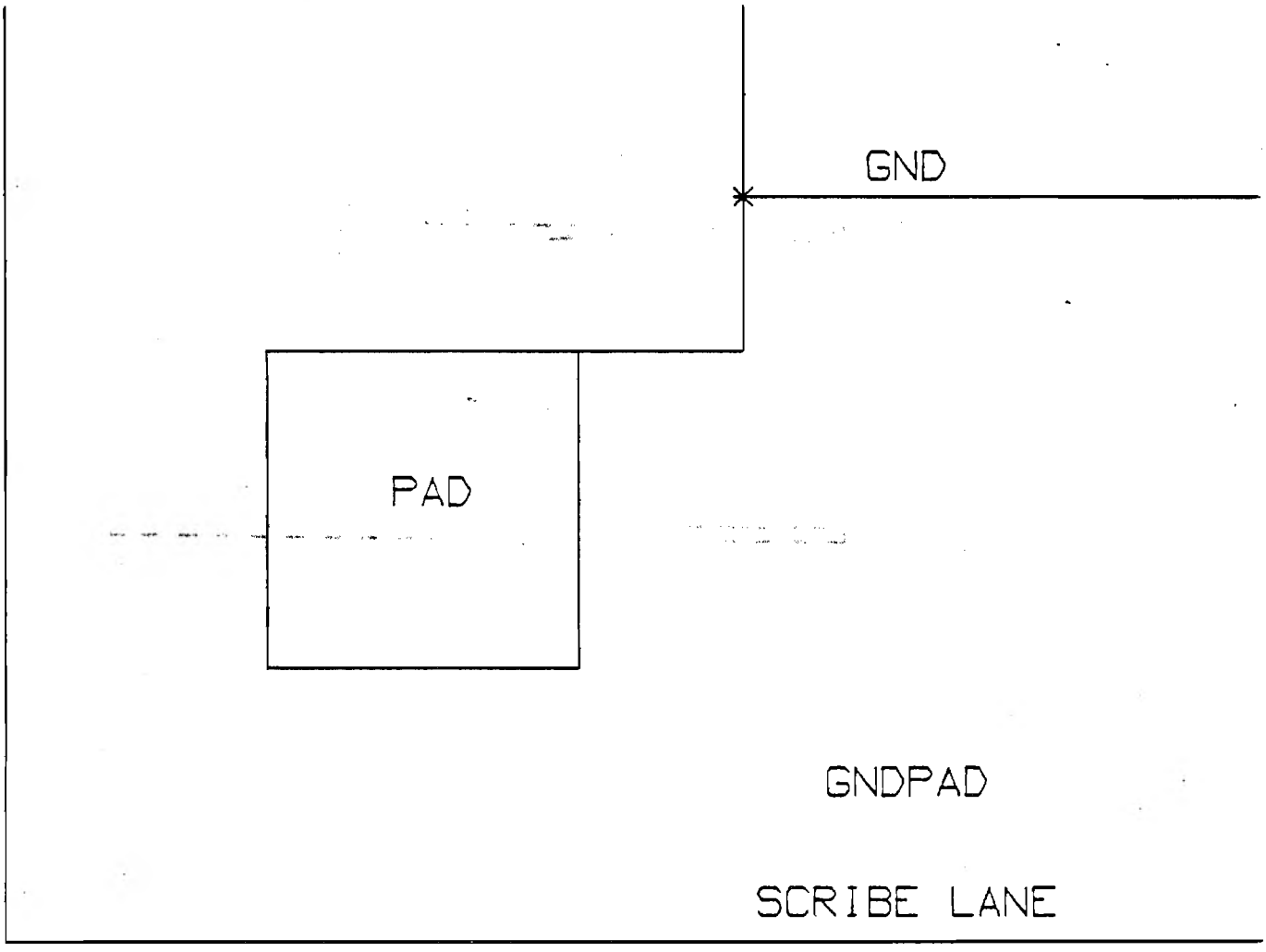


Figure 8-26: GNDPAD CELL SCHEMATIC

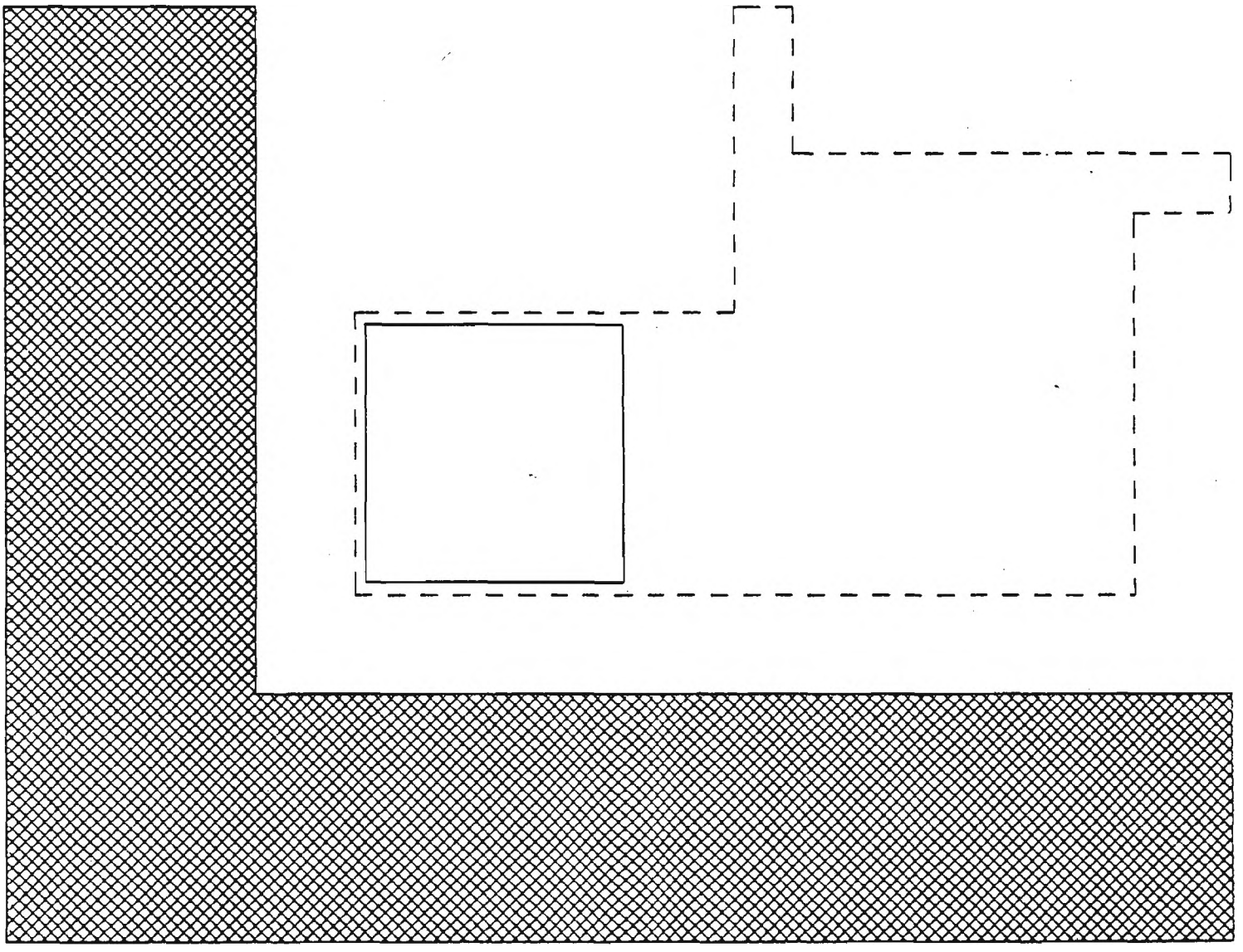


Figure 8-27: GNDPAD CELL COMPOSITE

PAD CELLS

Cell Name - FILLPAD

Function - This cell consists of a 6 mil wide section of scribe line and Power and Ground buss. It is used to fill in the edge of a die where pads are not desired.

Width - 6 mils

Placement Restrictions - Edge

CIF Number -

Graphics - Figure 8-28 on page 129

Schematic - Figure 8-29 on page 130

Composite - Figure 8-30 on page 131

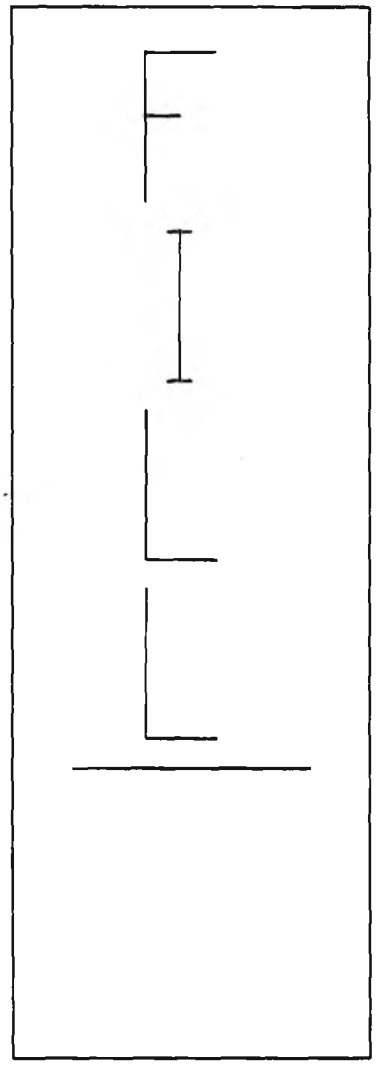


Figure 8-28: FILLPAD CELL GRAPHICS

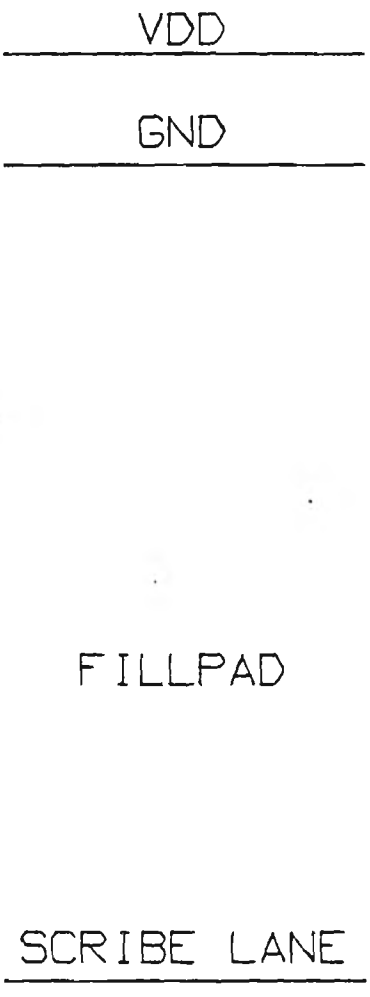
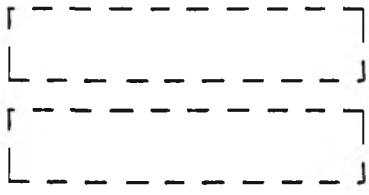


Figure 8-29: FILLPAD CELL SCHEMATIC



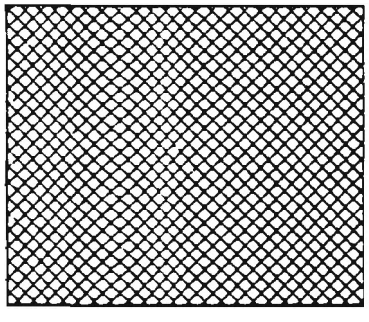


Figure 8-30: FILLPAD CELL COMPOSITE

PAD CELLS

Cell Name - CORNERPAD

Function - Like the Fillpad except for corners.

Width - 17 or 18 mils

Placement Restrictions - Corner

CIF Number -

Graphics - Figure 8-31 on page 133

Schematic - Figure 8-32 on page 134

Composite - Figure 8-33 on page 135

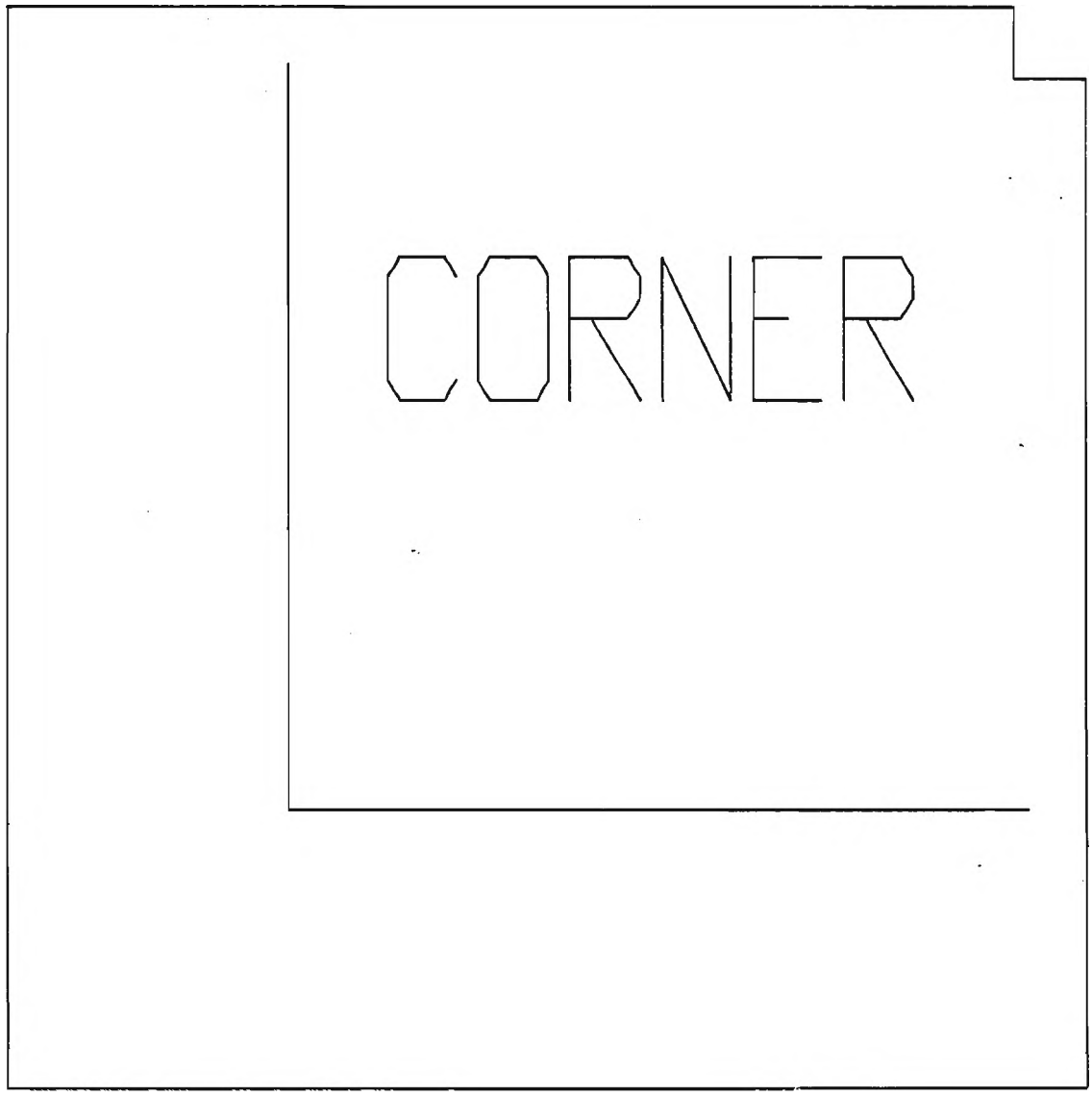


Figure 8-31: CORNERPAD CELL GRAPHICS

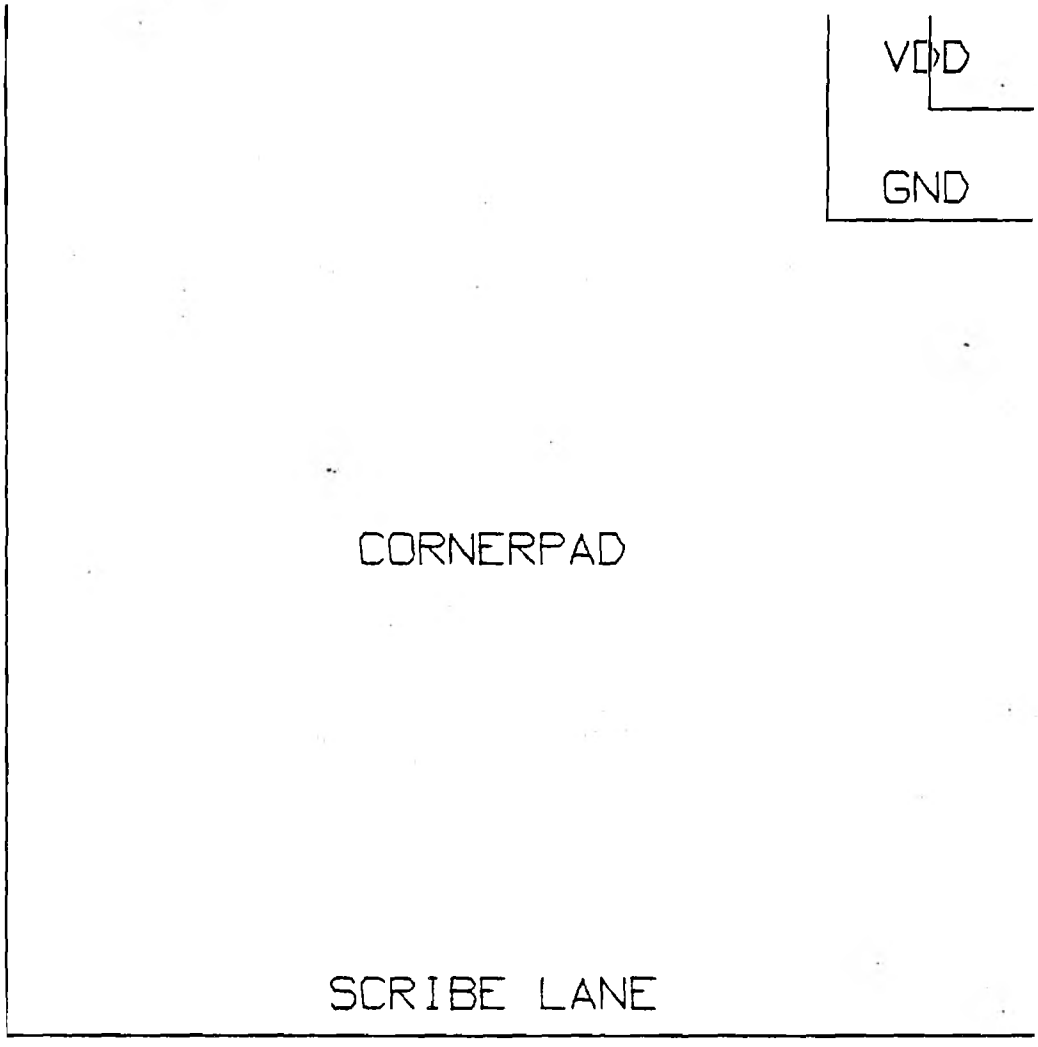


Figure 8-32: CORNERPAD CELL SCHEMATIC

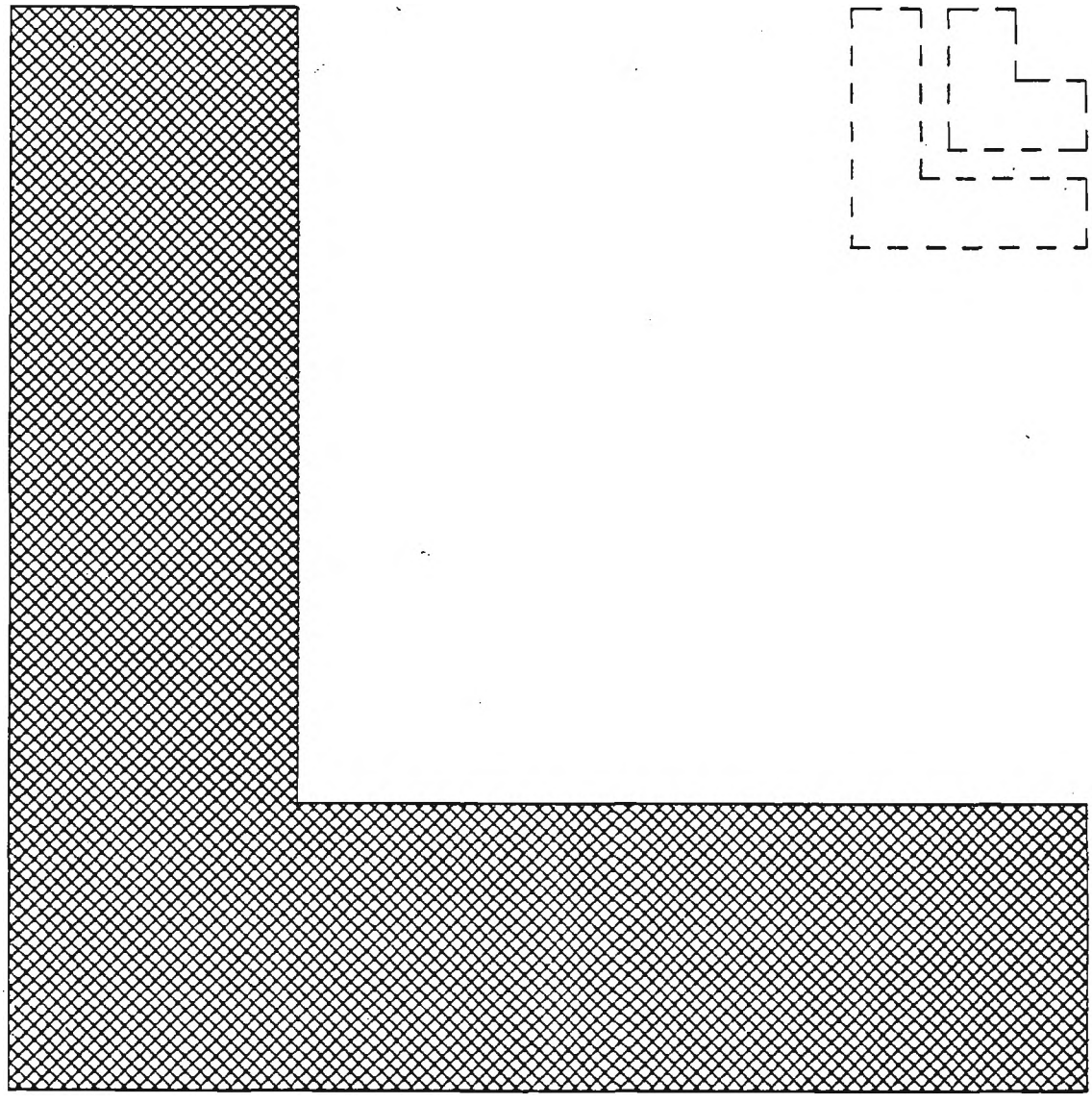


Figure 8-33: CORNERPAD CELL COMPOSITE

9. CONCLUSIONS

When using the CV system to build circuits with the PPL cell set the following procedure should be followed.

1. SELECT DIRECTORY yourdirectory

2. For english circuits:

```
DEL FIL CDEF**.US
COPY FIL
FROM: EPPL.DOC>CDEF.ECEL
TO: CDEF**.US
(This will copy the correct menu file to the station you are
working on.)
```

   a. SETUP (this command is on the digitizer pad of the CV and will set up the parameters correctly for that station.) The MRU will be M=1E-5,S=E,U=100. And the grid will be X=2.15,Y=1.55,D=1.

   b. SELECT PRED dirname>EPPL.x (WHERE x is GRP,CKT, or SCHEM)

For metric circuits:

```
DEL FIL CDEF**.US
COPY FIL
FROM: NMOS6.DOC>CDEF.MCEL
TO: CDEF**.US
(this will copy the correct menu file to the station you are
working on.)
```

   a. SETUP (from digitizer pad.) The MRU for the metric version is M=25E-6,S=M,U=4. And the grid is X=52,Y=35.

   b. SELECT PRED dirname>NMOS6.* (WHERE * is GRP,CKT or SCHEM)

When referring to either version of the cell set the directory extension GRP refers to the graphics directory, CKT refers to the composite directory, and SCHEM refers to the schematic directory.

When inserting the cells into your circuit you MUST use the menu pad in order for the cells to be inserted in the correct locations and with the proper tags. These tags are used by the program which flips the cells after the circuit has been completed and before the pads have been inserted.

After inserting all of the logical cells it is then necessary to insert row and column pull-up cells on all rows and columns which do not have cells with built in pull-ups. The remainder of the area must be filled with blank (BLK) cells to complete the rectangular area bounded by the outer cells. VBUS,GBUS,RCAP, LCAP, and CKCN cells must then be inserted around the border

of the circuit (see the individual documentation for these cells).

The final processing step on the active PPL area is to flip the cells. This is done because the cells share power and ground and contacts to conserve space. These programs need to be run from the menu. They are called 'Flip even rows' and 'Flip even columns'. They prompt the user to digitize the beginning location and then flip every other row or column location in the circuit.

To flip the rows, digitize to the left of the lower left corner of the LCAP in the lower left corner of the circuit. To flip the columns, digitize one row below the previous digitize. To determine that this was done correctly, you should make sure that the LCAP cells and the VBUSS cells get mirrored.

After running both programs do 'SEL PRED directory>x.y' (where x is EPPL or NMOS6 and y is CKT or SCHEM.) This will reset any changes made to the predecessor structure by the mirroring programs.

When the cells have been properly flipped, the pads may be inserted by selecting the pad grid and inserting the pads from the menu. Wires should be run from the pads to the circuit by selecting the wire grid and inserting metal wires of width W=.3 mill or 7 microns.

Figure 9-1 shows a complete PPL design of a simple counter. Notice the placement of the bussing cells used to complete the structure.