Advances in experimental technique for quantitative two-dimensional dopant profiling by scanning capacitance microscopy

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Several advances have been made toward the achievement of quantitative two-dimensional dopant and carrier profiling. To improve the dielectric and charge properties of the oxide–silicon interface, a method of low temperature heat treatment has been developed which produces an insulating layer with consistent quality and reproducibility. After a standard polishing procedure is applied to cross-sectional samples, the samples are heated to 300 °C for 30 min under ultraviolet illumination. This additional surface treatment dramatically improves dielectric layer uniformity, scanning capacitance microscopy (SCM) signal to noise ratio, and $C-V$ curve flat band offset. Examples of the improvement in the surface quality and comparisons of converted SCM data with secondary ion mass spectrometry (SIMS) data are shown. A SCM tip study has also been performed that indicates significant tip depletion problems can occur. It is shown that doped silicon tips are often depleted by the applied SCM bias voltage causing errors in the SCM measured profile. Worn metal coated and silicided silicon tips also can cause similar problems. When these effects are tested for and eliminated, excellent agreement can be achieved between quantitative SCM profiles and SIMS data over a five-decade range of dopant density using a proper physical model. The impact of the tip size and shape on SCM spatial accuracy is simulated. A flat tip model gives a good agreement with experimental data. It is found that the dc offset used to compensate the $C-V$ curve flat band shift has a consistently opposite sign on p- and n-type substrates. This corresponds to a positive surface on p-type silicon and to a negative surface on n-type silicon. Rectification of the large capacitance probing voltage is considered as a mechanism responsible for the apparent flat band shift of (0.4–1) V measured on the samples after heating under UV irradiation. To explain the larger flat band shift of (1–5) V, tip induced charging of water-related traps is proposed and discussed. © *1999 American Institute of Physics.* [S0034-6748(99)03001-4]

I. INTRODUCTION

Over the past few years, the use of the scanning capacitance microscope (SCM) for the quantitative measurement of two-dimensional (2D) dopant profile of submicron devices has been increasing.[1–7] The requirements for the 2D mapping of new-device-generations include a spatial accuracy below 5 nm and sensitivity to the doping concentration from 10^{16} to 10^{20} cm^{-3} as well as reproducibility of the result.[8] The possibility to fulfill these requirements strongly depends on the experimental ability to control and maintain the state of the probe–sample interface in conjunction with the conversion algorithm based on a realistic physical model. As in the case of a 1D parallel plate metal–oxide–semiconductor (MOS) capacitor, the SCM is sensitive to the variations in dopant density and surface charge properties of the insulator–semiconductor system. Due to the small size and nonplanar shape of the probe tip, the situation for SCM dopant profiling is more complex in both theoretical and experimental aspects than the 1D MOS capacitance. Theoretically, a quasi-2D model of a hemispherical tip brought to the planar insulator–semiconductor surface has been developed and has been proven to be a quick and convenient way to convert experimental SCM data.[2–4] The experimental situation in SCM imaging remains not so clear because of the complexity of the 3D tip–air–insulator–semiconductor surface interaction. Two major challenges for SCM measurements include the quality of the insulating layer between the tip and semiconductor and the tip quality itself. In the present work, recent improvements in sample preparation and tip quality evaluation are reported.

II. SURFACE QUALITY

Several methods have been used to produce an insulating layer on the silicon surface for SCM imaging.[9] It was found that most of the traditionally used dielectric layers (native oxide, thermally induced oxide, sputtered silicon dioxide, etc.) for different reasons could not fulfill the requirements for quantitative SCM dopant profiling. The insulating layer produced by the final step of standard polishing technique has been found to be of sufficient quality for SCM imaging.[2,10] Samples prepared in this way require no additional oxide deposition on the semiconductor surface for insulation. However, other qualities of this insulating layer cannot be controlled during sample preparation and reproducibility of SCM results is often not adequate for quantitative analysis.

The main disadvantages of this surface preparation method include low signal–noise ratio, nonuniform dielectric and charge properties along the polished surface, and large dc flat-band offset of $C-V$ curves. For a conventional 1D

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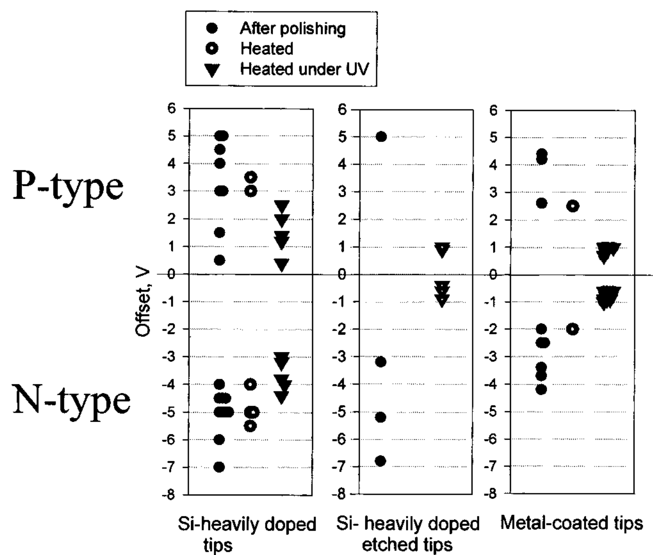

FIG. 1. dc offset of the maximum ΔC signal measured on the silicon substrate with doping concentration of $\sim 10^{15}$ cm^{-3} ($C-V$ curve flat-band shift). The voltage is applied to the sample and tip is grounded.

MOS capacitor, oxide charge (fixed or trapped) causes the flat band of $C-V$ curve to be shifted along the voltage axis, while interface traps (surface states) affect the $C-V$ curve by stretching out the transition region between accumulation and inversion.[11] The density of the oxide charge and surface traps can be calculated by comparison of measured and theoretical $C-V$ curves. In the SCM case, the $C-V$ curve is additionally stretched out by the 3D character of the potential distribution between the probing tip and oxide–semiconductor interface, as well as by the large capacitance sensor probing voltage. Moreover, the basic modeling parameters (dielectric constant, oxide thickness, tip size, and capacitor probing voltage) are not exactly known to provide a quantitative $C-V$ curve comparison. Nevertheless, the flat-band position measurement in the SCM case may be at least qualitatively used to evaluate the oxide charge property and its change under different surface treatments. In Fig. 1 the dc offsets measured by SCM on p- and n-type silicon substrates with doping concentration of $\sim 10^{15}$ cm^{-3} are shown. The offset value is the measured dc bias corresponding to the maximum change in capacitance with an ac depletion bias of 1 V amplitude applied to the sample (tip is grounded). This dc offset corresponds to the maximum slope of the $C-V$ curve ($dC/V=\max$) and may be used to approximately evaluate the flat-band shift.[12]

As one can see in Fig. 1, the dc offset (flat-band position) for the as-polished surface varies from sample to sample in a very wide range from +0.4 to +5 V for p-type and from -2 to -7 V for n type of silicon substrate. The large value as well as the large differences in flat-band offset for p- and n-type substrates cause some problems for SCM imaging. In the case of samples without junction, adjusting the dc offset voltage applied to the sample can compensate the flat-band shift caused by charge.[2,9] This adjustment is performed on the most lightly doped region of the sample and as a rule, remains adequate (maximum change in capacitance) for heavily doped regions as well. Another situation is seen in p-n junction imaging. As in a case of the 1D MOS capacitor, the charge trapped at the oxide–semiconductor interface causes a $C-V$ curve flat-band shift. The apparent position of p-n junction is very sensitive to the oxide charge due to the 3D interaction of the built-in p-n depletion and charge-induced surface depletion.[5,7] When an oxide charge is uniformly distributed along the surface, the charge-induced depletion can be somewhat compensated by dc voltage applied to the sample, in a manner similar to the nonjunction case. A nonuniform charge distribution causes variations in the charge-induced depletion, which cannot be compensated by the dc offset voltage over the whole surface. As a result, the measured position of p-n junction is shifted, causing errors in the spatial p-n junction delineation.

In Fig. 2, cross-sectional SCM 2D images are shown of a gate-like structure taken in ΔC mode (constant ac depletion bias is applied to the sample and the change in capacitance is recorded). The sample was prepared by implanting

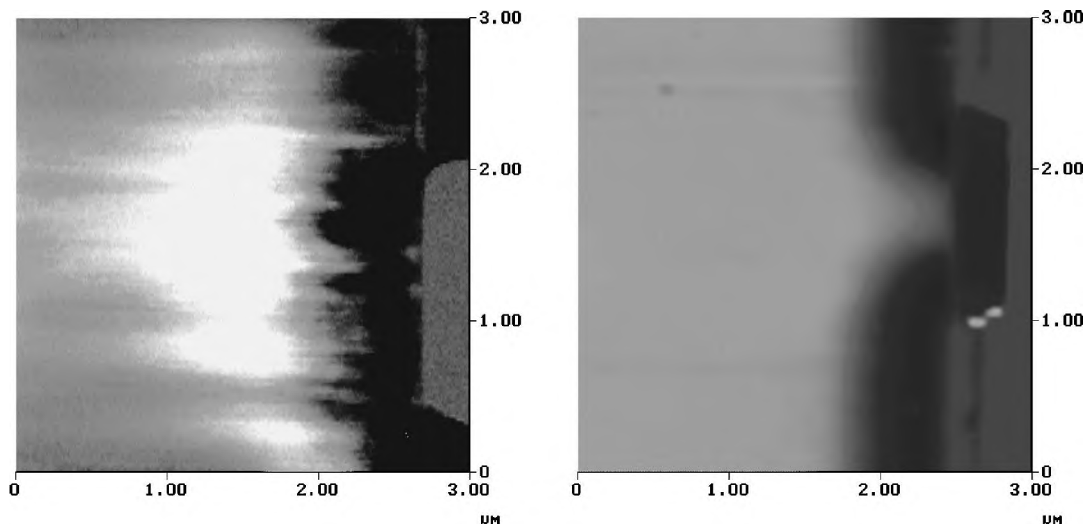

FIG. 2. Cross-sectional SCM images in the vicinity of a p-n junction, left-hand side after polishing with colloidal silica suspension, and right-hand side after low temperature heating under UV exposure.

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with 35 keV As ions at a dose of 10^{15} cm^{-2} into a *p*-type substrate with a B-doping concentration of 10^{15} cm^{-3} and annealed at 950 °C for 80 min. *p*-*n* junctions are formed between 1.5 μm gates with 1.5 μm spacing. The left-hand side image is centered between two gates while a single gate is shown in the right-hand side image in Fig. 2. The left-hand side image was taken on an untreated surface formed after polishing with a colloidal silica suspension. This image is a good illustration of a SCM image taken on a surface with a difference in flat-band position for *p*- and *n*-type sides of the junction. The dc offset voltage is chosen to compensate for the flat-band shift at the *n*-type region of the sample (dark region on the image). This dc bias pushes the *p*-type response (light region) far from the gate edge, so that there is no *p*-*n* junction contrast in the vicinity of the gate.

Another disadvantage of the large dc offset is the possibility that field-induced oxidation (FIO) will occur during SCM imaging. It has been observed that during atomic force microscopy (AFM) scanning along the silicon surface with a positive bias on the sample, additional oxide growth is induced by the tip–sample field.[13] The rate of FIO depends on the doping concentration, scanning rate, and on the difference in the applied dc voltage and the FIO threshold voltage found to be +(3–5) V. The same effect is observed in our experiments. FIO leads to a decrease in SCM sensitivity and when FIO occurs on consecutive scans, little useful information can be taken from this surface area. Even when SCM imaging is performed with positive offset voltage, but less than the FIO threshold voltage, the surface is often charged causing a significant decrease in SCM sensitivity.

Several attempts have been made to improve the dielectric and charge properties of the insulating layer. A good result has been achieved by sample heating at 300 °C for 30–40 min in an air environment. After heat treatment, the signal/noise ratio increases several times and the ΔC signal distribution becomes more uniform along the polished surface. Nevertheless, a dc offset shift remains very high even after heating and still differs substantially for *p*- and *n*-type semiconductor (see Fig. 1). The best result has been achieved using ultraviolet (UV) irradiation of the polished surface during the heat treatment (the preliminary results were reported earlier[14]). The UV exposure is performed using a ''Mineral-light'' S89 standard UV lamp (from Ultra Violet Products, Inc.) at a distance of 3–5 in. The combination of UV exposure with heat treatment leads to a further increase in the signal/noise ratio so that the measured SCM dynamic range (ratio of the signal for lightly and heavily doped regions of the sample) is in good agreement with theoretical predictions.

The most significant change is found in the charging properties of the dielectric–semiconductor interface. First, the measured dc offset moves toward 0 V for all tips used (see Fig. 1). It is found that for tips which can be treated as quasimetallic, the dc flat-band offset slightly changes from sample to sample in a range from +0.6 to +1.0 V for *p* type and from −0.4 to −1.0 V for the *n* type of substrate. Practically, this means that there is very little charge trapped in the oxide and the quality of this system is close to the ideal one for SCM imaging. The right-hand side image in Fig. 2 shows a SCM image taken with 0 V dc offset after heating with UV exposure of the polished surface. Due to the relatively small dc flat-band offset difference between *n*- and *p*-type regions (<1 V), the contrast between the *p* and *n* side of the junction is clearly seen in the vicinity of the gate. The 2D position of the electrical junction can be easily found as the transition line between the *p*- and *n*-type regions. The combination of the heat treatment and UV irradiation leads to the additional passivation and charge redistribution along the polished surface. We believe that the streaky lines on the left-hand side image in Fig. 2 are due to the nonuniform charge distribution left after polishing (the direction of polishing is perpendicular to the sample edge). Note, that the topographic image was taken simultaneously, and is very uniform and does not reveal any scan errors. As can be seen in the right-hand side image, there are no such features after heating with UV irradiation.

III. TIP QUALITY EVALUATION

In this work, three types of probing tips (provide by Digital Instruments, Inc.) are investigated for dopant profiling in the doping range of 10^{15}–10^{20} cm^{-3}. The heavily doped silicon tips have been ion implanted and RTA annealed. The metal-coated tips are commercially available Co/Cr-coated silicon tips, such as those used for magnetic force microscopy. Silicided silicon tips are the third types characterized. Basically, the metal coated and silicided tips provide a good metal-like behavior over the dopant range investigated.

Two major problems of heavily doped silicon tips are found. First, a native oxide on the tip apex exists and its quality varies from tip to tip causing a variation in the measured dc offset. Due to charge in this oxide, the dc offset measured with these tips is higher than those measured with metal-coated tips, even for samples heated with UV exposure (see Fig. 1). Field induced oxidation of the heavily doped silicon tips is also observed during SCM imaging with either a dc or ac bias voltage larger than the threshold FIO voltage. The additional oxidation of the tip apex significantly decreases the SCM sensitivity and reduces the experimental dynamic range. To remove the oxide, the doped silicon tips were etched in 5% HF solution for 15–30 s. After the oxide etch, the dc offset is practically the same as those measured by the metal-coated tips (Fig. 1).

The second problem with the heavily doped silicon tips is that tip depletion is observed, which is comparable to the sample depletion in a heavily doped region. To measure this tip depletion effect, the tip is brought to a metal surface and a ΔC signal is measured as a function of the ac bias voltage applied. For this experiment, a Ni thin film with native oxide grown during storage in air (several months) is used. As measured, the direct current between tip and metal film is less than 10^{-12} A even for large voltage of 10 V. In Fig. 3 the depletion effect measured for a heavily doped silicon tip is compared with those for a metal-coated tip. The ΔC signal dependence on the ac voltage measured with the metal-coated tip is due to instrumentation coupling (presumably through a ground loop existing between the sensor system

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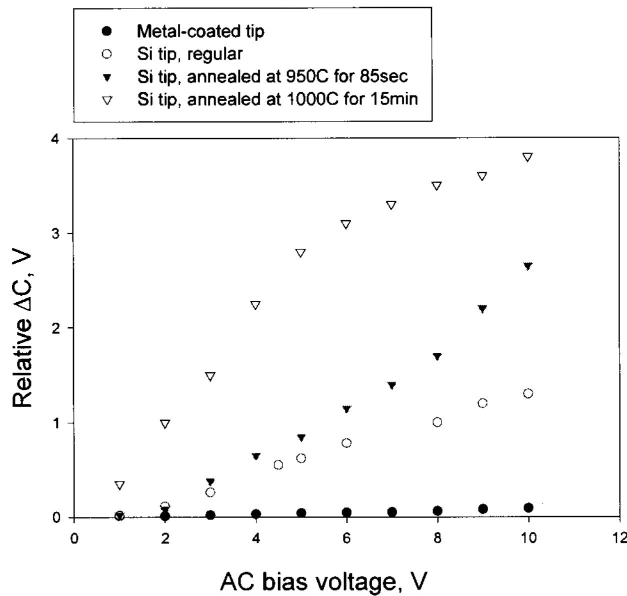

FIG. 3. Tip depletion effect measured on a metal surface.

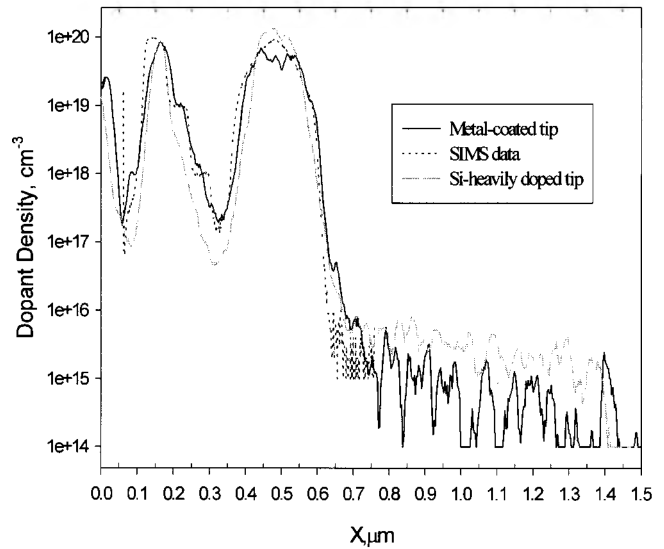

FIG. 4. Comparison of converted SCM data with the vertical SIMS dopant profile.

and the AC generator). This coupling effect is small compared to the ΔC signal which comes from both lightly and heavily doped regions of the sample (by a factor of $\sim$100 for lightly and 2–3 for heavily doped regions). The coupling and tip depletion effects measured with the heavily doped silicon tips on a metal surface are at least ten times greater than those measured with metal-coated tips. The heavily doped silicon tips were annealed to change the surface doping concentration at the tip apex. As can be seen in Fig. 3, the ΔC signal measured with annealed tips significantly increases compared with nonannealed tips. The increase depends on the annealing parameters. It is found that the depletion effect varies from tip to tip.

The impact of tip depletion on quantitative SCM dopant profiling is shown in Fig. 4. The SEMATECH No. 1 sample with two peaks in the dopant profile and two steps (50 nm width) on the trailing edge of the first peak is used. An abrupt vertical dopant profile was grown by a custom Si–Ge chemical vapor deposition system. In Fig. 4 the vertical dopant profile measured by secondary ion mass spectrometry (SIMS) is compared with SCM results. The SCM data are measured in ΔV mode[2,9] and converted to a dopant profile using the quantitative SCM conversion algorithm described elsewhere.[2,3] The SCM profile is pinned at one point in the dopant profile (10^{20} cm^{-3}). Using a single free parameter, the SCM data are converted to dopant concentration to fit the substrate doping level at 10^{15} cm^{-3}. With this approach, a good fit of the SIMS vertical dopant profile and the SCM data taken with the metal-coated tip is observed. However, the results are different for data taken with a regular heavily doped silicon tip. As shown in Fig. 4, heavily doped silicon tip data could not fit the dopant profile for three basic doping concentrations at 10^{20}, 10^{17}, and 10^{15} cm^{-3} using the same approach as for the metal-coated tip. The explanation for this result is that in the ΔV mode the magnitude of ac bias is automatically changed to maintain the ΔC signal constant. This leads to a large ac voltage in heavily doped regions and a small ac voltage in lightly doped regions of the sample. Since the tip depletion effect depends on the ac bias voltage (see Fig. 3) the contribution of the tip depletion to the total SCM signal changes with the doping concentration and therefore distorts the SCM data.

IV. SCM SPATIAL RESOLUTION

The dopant profile of the SEMATECH No. 1 sample has two dopant steps at 10^{19} and 10^{18} cm^{-3} with spatial width of 50 nm (Fig. 4). The SCM measurements give the right position of these steps, but with a width that is smaller than the actual width. To investigate the SCM spatial resolution dependence on the tip size, metal-like tips with hemispherical radii of 15, 25, and 35 nm have been used. We have found almost no correlation between the tip size and spatial resolution. To understand such a strange result, the shape of the tip apex was examined by scanning electron microscopy before and after SCM imaging. It is found that even after a short time of SCM scanning, the very apex of the tip is worn (sometimes as short as several line scans). The worn tip is found to be no longer hemispherical, but rather flat. In some cases, tip depletion of a worn metal-coated tip is observed and the impact of the tip depletion on the quantitative SCM dopant profile is basically the same as that shown for a heavily doped silicon tip. These problems are common for all probes, which are based upon crystalline silicon tips.

The impact of the tip model on the spatial resolution was numerically simulated and the results are compared with experimental data in Fig. 5. As an input to the SCM simulator, the vertical dopant profile measured by SIMS is used and the SCM signal in the ΔV mode is calculated taking into account the gradient of the doping concentration underneath the tip.[15] The impact of the tip apex shape on the SCM spatial resolution is clearly seen in Fig. 5. The resolution of 50 nm steps dramatically decreases with increase in the flat tip radius from 15 to 35 nm while the hemispherical tip model gives almost the same resolution for both tip sizes. It is seen that the spatial resolution, general shape, and dynamic range of

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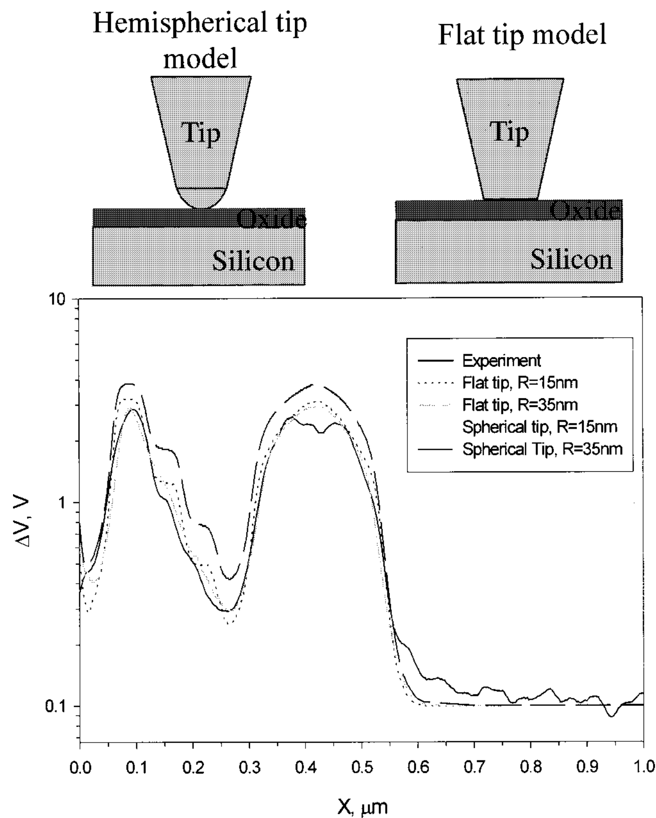

FIG. 5. Impact of the tip model on the spatial resolution simulated for SEMATEC No. 1 sample in ΔV mode.

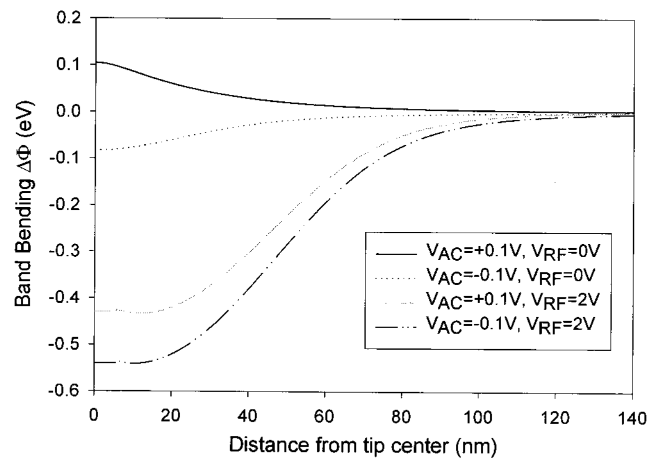

FIG. 6. Time average band bending underneath the hemispherical tip with radius $R_t = 35$ nm calculated in small signal approximation $V_{rf}=0$ V and for amplitude of probing signal $V_{rf}=2$ V. The oxide thickness is $t_{ox}=20$ Å and silicon doping concentration is $N_D = 10^{15}$ cm^{-3}.

the ΔV signal calculated for the flat tip model agree well with experimental data. Based on this comparison, the effective radius of a worn tip can be evaluated as $R_t > 30$ nm (note, that in many cases the experimental spatial resolution is even worse than is shown in Fig. 5). In the simulation algorithm for both tip types, the model of a tip surrounded with air, resting on a thin oxide which covered the silicon was used. As an alternative mechanism of degradation in spatial resolution, a tip surrounded with water has been evaluated. When the dielectric constant of air is replaced by the dielectric constant of water, a strong spatial degradation is observed in the simulation. However, the general shape and significant decrease in the dynamic range calculated with the tip surrounded with water are not consistent with experimental data. Further studies in this area are required.

V. DISCUSSION

Figure 1 summarizes the set of SCM flat-band shift measurements performed on lightly doped n- and p-type silicon for as-polished, heated (in an air environment), and heated with UV exposure. After all surface treatments, the dc offset used to compensate flat-band shift is consistently positive on p type and negative on n type of the silicon substrate (remember that the dc offset is applied to the substrate). This result is unusual for the conventional 1D MOS capacitance measurements. To understand it, two major factors that are different in the SCM experiment should be considered. First, in SCM measurements the small signal approximation is violated because a large capacitance sensor probing voltage is applied. Second, an ultrathin oxide with thickness of (10–30) Å is required for SCM data acquisition to achieve high spatial resolution in a wide range of doping concentrations. To avoid dopant ion redistribution by high temperatures needed for thermal oxide growth, low temperature oxidation processes are commonly used for the SCM cross sectional dopant profiling. The structural, dielectric, and charging properties of low temperature oxides are not well investigated and in some cases can be understood only by an analogy with the thermal oxide widely described in the literature.

The amplitude of capacitance probing voltage depends on many factors including geometry of the experiment, stray capacitance, and set point on the sensor resonance. For the real experimental condition the value V_{rf} (rf probing signal) can vary from one to many volts.[2,3] During the negative and positive cycle, the rf signal drives the silicon under the tip into both deep depletion and accumulation. In Fig. 6 the time average band bending underneath the tip is calculated in the small signal approximation ($V_{rf}=0$) and for a typical value of the probing voltage ($V_{rf}=2$ V). An ac bias voltage amplitude of $V_{ac}=0.1$ V is chosen as it is in a real ΔV SCM mode on a lightly doped silicon. As can be seen, the large rf probing voltage produces an average depletion. This rectification effect is due to the difference in band bending in accumulation (small) and depletion (large), so that on average, the silicon under the tip is depleted with $\Delta\Phi \sim 0.5$ eV. Hence the rectification of a large probing voltage drives both p- and n-type silicon into depletion, the measured flat-band position of the $C-V$ curves is shifted in opposite directions for p and n type of silicon. The apparent flat-band shift should be experimentally compensated by dc voltage of $V_{off} \sim +0.5$ V for the p type and $V_{off} \sim -0.5$ V for n type of substrate. This simulated result is in good agreement with the flat-band shift of (0.4–1) V measured on the samples heated with UV exposure (see Fig. 1). However, the larger shift of (1–5) V measured on as-polished and heated (in air) surfaces could not be explain by this effect and other mechanisms should be considered.

Recently, an x-ray photoelectron spectroscopy study of

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surface preparation techniques commonly used for SCM measurements was reported.[16] According to this study, silicon surfaces after polishing by a colloidal silica suspension have about one monolayer or even less of silicon bonded to oxygen atoms and after heating at 200 °C in air the ''effective thickness'' of the oxidized layer was evaluated as (4–6)Å. As has been shown previously,[17] in MOS structures with ultrathin oxide (less than 10 Å) the Si–SiO_2 interface is in equilibrium with the metal because of tunneling transparency of this oxide layer and the semiconductor surface is pinned to the Fermi level of the metal. In this case Schottky barrier characteristics are observed. For MOS Schottky emission structures, a strong current is expected for forward biases (minus for n type and plus for p-type substrate, in our case). At reverse bias, the $C-(V)^{-1/2}$ capacitance–voltage characteristics with a maximum slope near 0 V are expected. In our experiments such behaviors have not been observed. For quantitative SCM dopant profiling the flat-band shift is compensated by adjusting the dc voltage to produce the maximum SCM signal on the most lightly doped region of the sample (see Fig. 1). In the case of a Schottky emission structure, the sign of the measured dc offset means a strong forward biasing for both n- and p-type substrates, so that distortion of SCM data should be expected. However, on the nonjunction samples heated in the air at 250–300 °C the SCM data have been taken routinely with dc offset in a range of (1–5) V and a good fit between SCM and SIMS dopant profile data have been observed in a wide dopant range of $10^{15}-10^{20}$ cm^{-3}.[2,3] In many cases, quantitative data with a large dc offset voltage were measured on as-polished surfaces and no leakage current was detected.

A systematic study of chemomechanical polishing of silicon with a colloidal silica suspension (slurry) has shown that the removal rate as well as the oxidizing effect strongly depends upon the slurry pH.[18] The highest removal rate and close to the ideal hydrogen termination of silicon surfaces are achieved at pH=11.5. At lower pH, a drop in the removal rate has been observed together with an increase in oxidation rate. In our experiments we are using the colloidal silica with pH$\sim$7. According to the authors of Ref. 18, this slurry solution provides a minimal removal rate and a maximum oxidizing effect. The typical oxide thickness used to convert SCM data to the doping concentration is (15–30) Å. We believe that these values correspond to the typical oxide thickness seen in our SCM measurements. The discrepancies in oxide thickness evaluated by the authors in Ref. 16 and our results may be caused by the difference in slurry pH used during a final step of sample polishing.

In MOS structures with oxide thickness in the range of 20–50 Å the Si–SiO_2 interface is in equilibrium with the semiconductor and typical MOS capacitor behavior is observed.[17] However, the probability of a direct quantum mechanical tunneling across the SiO_2 barrier in accumulation is still high enough to modify MOS capacitance measurements. Brar, Wilk, and Seabaugh[19] have measured the direct tunneling current in 1D MOS structures with oxide thickness in a range of t_{ox}=(16–35) Å. In the accumulation (V=2 V) the tunneling current density decreases with increase in oxide thickness over seven orders of magnitude from $\sim 0.5\times10^2$ A cm^{-2} (t_{ox}=16.5 Å to $\sim 1\times10^{-6}$ A cm^{-2} (t_{ox}=35 Å). These data can be used to evaluate the equivalent tunneling conductance parallel to the oxide–semiconductor capacitance in the SCM case. For typical tip radius R_t=350 Å (flat tip is considered) the tunneling conductance is evaluated as $G_{ts}^{-1}\sim 0.5\times10^{10}\ \Omega$ (t_{ox}=16.5 Å) while the capacitance impedance at the measurement frequency of 915 MHz is only $Z_{ox}\sim(10^7-10^8)\Omega$. Even in the worst case of a thin oxide $t_{ox}\sim$15 Å and flat tip model, the maximum value of the tunneling conductance is negligibly small and may be neglected in SCM measurements.

From another point of view, the carriers tunneling through the oxide in accumulation can be captured on the oxide traps and cause the $C-V$ curve flat-band shift. It is well known that all thermally grown SiO_2 films, which have been exposed to water, contain oxide traps related to the presence of water.[11,20,21] These water-related electrically neutral traps could be charged not only by avalanche electron ejection[20,21] but also by any charge flowing through the oxide.[21] Both negative[20,21] and positive[21] charging effects have been observed generated by injected current. The final step of chemomechanical polishing with silica suspension at pH$\sim$7 is a purely ''wet'' oxidation process in which oxide growth is due to slow oxidation in the presence of oxygen-containing water.[18,22] Because of this wet oxidation, the density of water-related traps in as-polished surfaces is expected to be higher than in ''dry'' thermally grown oxide films. In our opinion, the water-related traps may be responsible for the flat-band shifts that have been observed in our experiments. A high density of total charge on the order of 10^{13} cm^{-2} is expected to explain the flat-band shift of a few volts. This value seems to be reasonable for the wet oxidizing technology.

The sign of the dc offset voltage measured by SCM (see Fig. 1) indicates that the surface of n-type silicon is negatively charged, while the surface of the p-type silicon is positively charged. The sign of the trapped charge thus corresponds to the sign of the majority carriers in the silicon. This is a surprising result. We believe that this substrate dependent charging may be caused by the measurement process itself as described below. Since a large rf capacitance sensor probing voltage is often used (2 V peak), significant band bending at the silicon surface is continuously occurring. During the accumulation part of the rf cycle, the silicon conduction band (for the n-type substrate) is bent down. Majority carriers in the conduction band may tunnel to electrically neutral traps near the conduction band edge and be captured. This trapped charge shifts the flat-band potential of the surface toward depletion. During the depletion part of the rf cycle (for n-type material), the silicon conduction band is bent up. The recently filled traps are less likely to empty into the silicon because there are no states in the band gap. Therefore, on average, the oxide traps become negatively charged for n-type substrates. The same is true for p-type material, but the sign of the net-trapped charge is positive. This model also explains some of our experimental $C-V$ curve observations. It has been observed that strong accumulation in $C-V$ measurements is hard to reach on very thin oxides. It appears that the flat-band continuously shifts toward depletion during

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measurement and accumulation cannot be reached. This model is consistent with these observations. A detailed study of these phenomena is currently underway.

As shown in Fig. 1, after heating in air the flat-band shift is still large, manifesting that the density of oxide traps is still high and is not significantly changed in comparison with as-polished samples. This result agrees well with annealing experiments on 1D MOS structures.[11,20] It has been shown that low temperature heating at 200 °C does not change the chemical origin and density of water-related traps and can only discharge the preliminary charged trapping centers. The processes of charging by avalanche electron injection and discharging by low temperature heat treatment has been found to be reversible.[11] Another situation is seen in our experiments after heating with UV irradiation. The small dc offset shift after this treatment manifests that the density of trapping centers drops down at least an order of magnitude (to the level less than 10^{12} cm^{-2}) causing the additional flat-band shift of only an order of ~0.1 eV. At the present time the chemical origin as well as mechanism of the annealing of water-related traps is not well understood.[11] We believe that UV irradiation advances further oxidation and annealing of water-related traps, lowering their density to a small level for SCM measurements. The passivation of the SiO_2–Si interface by hydrogen and removing the contamination from the top of the oxide layer, as well, seem to be essential parts of this surface treatment as observed in UV cleaning experiments.[23]

An additional observation has been made during these experiments. The dc offset data shown in Fig. 1 have been measured after heating under a room ambient with relative humidity RH>40% and temperature of 22 °C. At a low humidity RH<20% the flat-band shift after heating with UV irradiation remains almost the same as after heating without UV exposure. At intermediate humidity 20%<RH<40%, an asymmetry in the flat-band shift for *n*- and *p*-type silicon has been observed. While in *p*-type silicon the dc offset decreases to (0.4–1) V as it was for RH>40%, the dc offset measured on the *n*-type substrate does not decrease significantly and remains large in the range of −(1–2) V even after heating under UV irradiation. This result correlates with observations that the complete discharge of negatively charged water-related centers by low temperature heating can be achieved only in a wet ambient with relative humidity of ~50%.[11,20] Experiments to date do not permit any firm conclusions about the origin of negatively and positively charged oxide traps as well as the role of water in their annealing. Further experimentation, and especially modeling, is necessary to understand these phenomena.

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