A Wireless Integrated Circuit for 100-Channel Charge-Balanced Neural Stimulation

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***Abstract*—The authors present the design of an integrated circuit for wireless neural stimulation, along with benchtop and *in-vivo* experimental results. The chip has the ability to drive 100 individual stimulation electrodes with constant-current pulses of varying amplitude, duration, interphasic delay, and repetition rate. The stimulation is performed by using a biphasic (cathodic and anodic) current source, injecting and retracting charge from the nervous system. Wireless communication and power are delivered over a 2.765-MHz inductive link. Only three off-chip components are needed to operate the stimulator: a 10-nF capacitor to aid in power-supply regulation, a small capacitor (< 100 pF) for tuning the coil to resonance, and a coil for power and command reception. The chip was fabricated in a commercially available 0.6-μm 2P3M BiCMOS process. The chip was able to activate motor fibers to produce muscle twitches via a Utah Slanted Electrode Array implanted in cat sciatic nerve, and to activate sensory fibers to recruit evoked potentials in somatosensory cortex.**

***Index Terms*—Wirless integrated circuit.**

I. Introduction

THERE has recently been much success and research into applications for electrical neural stimulation, including deep brain stimulators, visual and auditory neural stimulators, and neuromuscular stimulators for the purpose of contracting paralyzed or otherwise disabled muscles [1]–[6]. Stimulation occurs when there is charge exchange over an electrode, creating an oxidation-reduction reaction at the electrode-tissue interface. In order to reduce electrode corrosion or cell death, no net charge should be transferred from the electrode into tissue. Two factors that are important to ensure charge balance are the type of stimulation used and a charge-balancing methodology.

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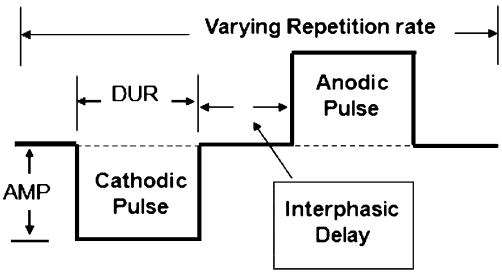


Fig. 1. Diagram of biphasic constant-current (CCS) pulse produced by the INIS chip.

Multiple stimulation techniques and waveforms have been used to produce the charge needed to recruit a motor response. A few of these stimulation techniques include voltage-controlled stimulation (VCS) [7]–[11], constant-charge or switched-capacitor stimulation (SCS) [12]–[14], and constant-current stimulation (CCS) [1]–[5], [15]–[20]. VCS is a highly efficient way to stimulate using a power-supply voltage, but it is difficult to control the amount of charge being injected and is highly dependent on the electrode tissue impedance. SCS is able to control the amount of charge injected in to the tissue by discharging a series of capacitors. However, capacitors are either very costly in terms of chip area or must be implemented off-chip. CCS is achieved by providing a constant current into an electrode. Since this technique allows for a high controllability of charge injection independent of electrode impedance, we use a biphasic (Fig. 1) CCS as our method of stimulation. Using a biphasic pulse, rather than a monophasic pulse, maintains charge balance. The charge delivered during the cathodic pulse is neutralized with the anodic pulse [16]. However, due mainly to second-order effects, a net charge can remain in the tissue. An important technique that has been implemented on many stimulators is a charge-balancing circuit to recover the charge.

Charge-balancing circuits bleed off or supply charge to maintain zero net charge over the complete stimulation cycle. A few charge-balancing circuits that have been implemented in previous works are blocking capacitors [12], electrode shorting or discharge resistors [21], an active charge-balancing technique described in [4], [17], [22], and an adaptive, passive discharge technique [23]. Blocking capacitors are generally too large to fit on an IC and must be implemented off-chip. Discharge resistors are large and can divert a substantial part of the stimulation current.

We have designed and implemented a low-power, implantable, 100-channel wireless neural stimulator using biphasic CCS, a novel active charge-recovery circuit, and local

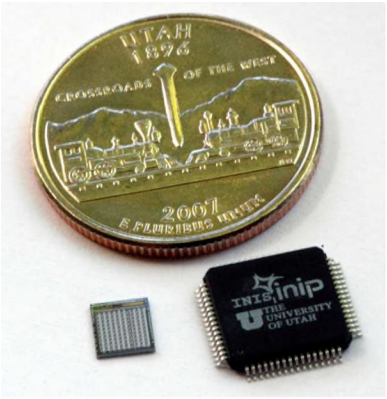


Fig. 2. INIS integrated circuit in bare die form and packaged in a plastic quad flatpack (QFP) package.

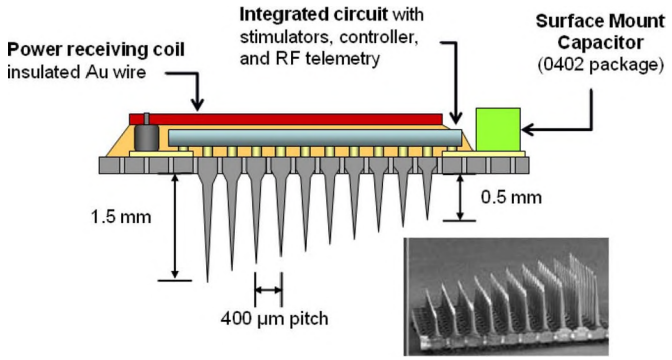


Fig. 3. Vision of a complete integrated neural interface (INI) assembly, with a USEA insert.

digital control for timing of individual electrodes. Recent advances in circuit integration have led to the ability to flip-chip bond microchips directly to the back of a 100-channel microelectromechanical-systems (MEMS) Utah slanted electrode array (USEA) or Utah (nonslanted) electrode array (UEA) (Figs. 2 and 3) [24]–[26]. The stimulator under development will take advantage of the selectivity inherent in the USEA or UEA, and could, for example, be used in next-generation prosthetic devices to provide tactile and proprioceptive sensation to people with amputations. Injecting and retracting charge from sensory nerves in the residual limb could create the internal feedback. The stimulator could also activate motor fibers in nerves to reanimate paralyzed muscles, or activate cortical neural tissue to restore lost sensory function. This integrated neural interface (INI) stimulator project is an extension of and a complementary design to an INI neural recording system also developed by our group [27].

In this paper, we present a fabricated and tested 100-channel wireless neural stimulator chip. The first integrated neural interface stimulator chip (INIS) uses a biphasic constant current source (Fig. 1) to provide neural stimulation. The rapid injection and retraction of charge indirectly changes the transmembrane potentials of nearby axons sufficiently to trigger action potentials. In order to deliver precise and reproducible control, the neural stimulator controls stimulation timing onboard after the desired values are programmed via wireless command transmission. Stimulation parameters may be reprogrammed at any

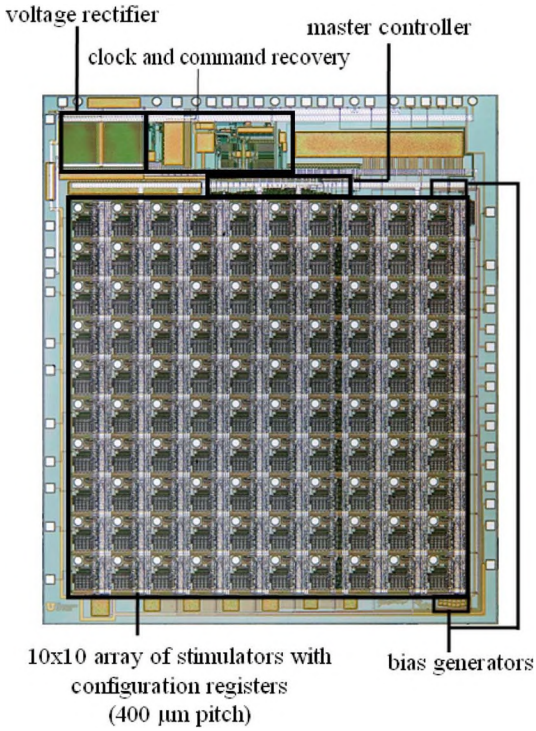


Fig. 4. Microphotograph of 4.6×5.4 mm^2 INIS wireless neural stimulation chip, fabricated in a commercial 0.6-μm 2P3M BiCMOS process.

time, and individual electrode sites may be activated or shut down at any time. Only three off-chip components are needed to operate the stimulator: a 10-nF capacitor to aid in power-supply regulation, a small capacitor ($<$100 pF) for tuning the coil to resonance, and a coil for power and command reception. Presented here are system-level chip designs and specifications that are well-suited for mating a chip to a 100-electrode UEA or USEA, plus experimental results from benchtop testing and *in-vivo* nerve stimulation sessions, that demonstrate the chip's successful operation.

II. INIS System Design

The 4.6×5.4 mm^2 INIS integrated circuit (IC) was fabricated in a commercially available 0.6-μm 2P3M BiCMOS process (Fig. 4). The majority of the layout area is occupied by a 10 $\times$ 10 array of stimulation cells with bond pads that match the 400-μm pitch of a USEA or UEA. Each of the 100 stimulation sites can be independently programmed and controlled. Power is supplied to the chip via a 2.765-MHz inductive link [28]. The voltage rectifier converts the ac coil voltage to an unregulated dc voltage; an on-chip series regulator using a bipolar output driver provides a nominal 5-V supply. The system clock is also obtained from the ac coil voltage; commands are sent at 20 kb/s to the chip via amplitude-shift keying (ASK) of the 2.765-MHz power signal [27]. The power-link frequency is divided by two to obtain the system clock frequency of 1.38 MHz.

The 10 $\times$ 10 array of stimulators is controlled by one global finite state machine (FSM). The global FSM interprets commands received from the amplitude-shift keying (ASK)-modulated power signal and communicates with the selected electrode site to program the current pulse amplitude, duration, in-

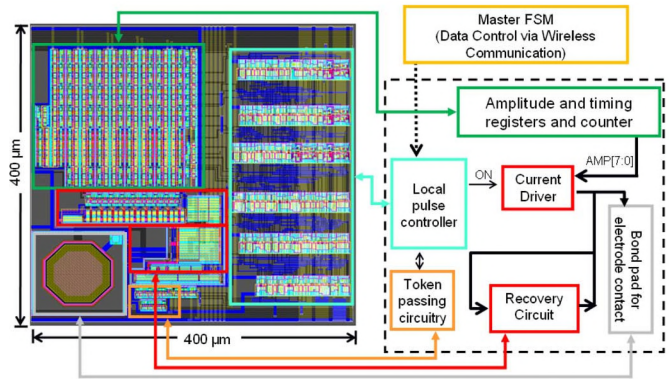


Fig. 5. Block diagram and layout of the global FSM, bias generator, power, clock, and command recovery, and electrode bond pad.

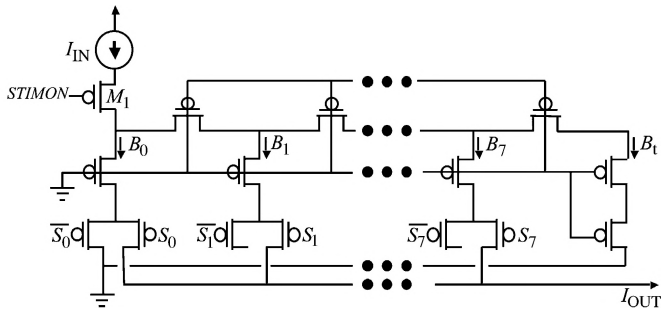


Fig. 6. $R-2R$ DAC MOSFET configuration.

terphasic delay, and repetition rate for that specific site. Each stimulator has independent values for each parameter that are stored in local registers. In order to produce the needed biphasic CCS pulse, each stimulator is made up of analog and digital components. Fig. 5 illustrates the system-level design as well as the components of a typical stimulator. Each site contains a digital-to-analog converter (DAC), output stage, active charge-recovery circuit, internal FSM, token cell, counter, and register bank.

The digital components for each stimulation site set the timing and control of the analog circuitry. The analog circuitry generates the current amplitude and direction for stimulation. Each stimulation cell consists of three analog subcircuits: an 8-b metal–oxide semiconductor field-effect transistor (MOSFET) $R-2R$ DAC [15] to provide a stimulation current, an output stage to amplify and control whether the current is sourcing or sinking from/to the electrode, and an active charge-recovery circuit to bleed off residual charge by supplying small amounts of current to the electrode to maintain charge balance. The entire chip contains one analog bias generator network to provide currents and cascode voltages used in the analog components of the individual stimulation cells.

The $R-2R$ DAC configuration used is shown in Fig. 6 [29]. All transistors had a width-to-length ratio of $4\ \mu\mathrm{m}/4\ \mu\mathrm{m}$ with the exception of transistor M_1, which had a width-to-length ratio of $24\ \mu\mathrm{m}/1.8\ \mu\mathrm{m}$. An $R-2R$ configuration was chosen over a typical binary weighted configuration to conserve power and size as it is repeated 100 times for each stimulation site. To conserve more power the DAC is turned off while not stimulating. As the number of bits increase, the $R-2R$ DAC becomes more advantageous since its size increases on the order of n, compared to 2^n for a binary weighted configuration. An $R-2R$ configuration has the disadvantage that much of the input current can be wasted. However, the total current supplied to the DAC from the global bias generator, labeled I_{in}, is one-tenth of the desired stimulation current, limiting the wasted current. The loads of the horizontal and vertical points of each branch $(B_0, B_1, \ldots B_7)$ are equal, thus splitting the current in half. Thus, the current through the branches is divided by powers of two as it moves from the first branch down to the nth branch. For the current to divide by powers of two through the network, the geometry and gate-to-body voltage need to be identical for all transistors. The circuit also needs to have a terminating branch I_t which acts as the load for the nth branch. The current in any particular branch is $\mathrm{I}_i = \mathrm{I}_{in}/2^i$, and the total output current is given by

$$I_{\mathrm{out}} = I_{\mathrm{in}} \sum_{i=1}^{n} \frac{s_i}{2^i} \tag{1}$$

where i represents each individual branch, n is the total number of branches, and S_i takes the value of one if connected to I_{out} and zero if connected to ground. The range of output current for the DAC is from 0.09–25 μA, with a step size of 90 nA. Device mismatch will lead to nonlinearity; the average normalized differential nonlinearity (DNL) was measured to be 0.21 and the average normalized integral nonlinearity (INL) was 0.98 (Fig. 7). The current produced by the DAC is fed to the output stage.

The output stage (Fig. 8) serves multiple purposes. First, to conserve power, the DAC was designed to produce a current of 0.1 to 25 μA, a tenth of the desired stimulation current of 1–250 μA. The output stage amplifies the current by a factor of ten. Second, the output stage provides the ability to source or sink current from/to the electrode, with the sourcing and sinking well matched in order to maintain a charge balance on the electrode. Third, the output voltage swings close to the power rails of $\pm$2.5 V to maximize the compliance voltage (Fig. 9).

The design of the output stage uses wide-swing cascode current mirrors to achieve a wide operating range. Transistors M3 and M4 are used to switch between sourcing or sinking current to the electrode. The gates of these two transistors are controlled by the internal FSM. Transistors M1, M2, M5, and M6 were sized ten times larger than transistors M_10, M9, M8, and M7 to produce the current needed to stimulate the neurons. Transistors M2, M5, M8, and M9 are used as cascode devices. These transistors are used to bias the drain-to-source voltages of transistors M1, M6, M7, and M10 so that they remain just above the triode region. Holding the drain voltages just above the triode region allows for a larger output swing voltage at the output node while maintaining near-constant current operation. The operating range for the output is between $\pm$2 V. Transistors M3 and M4 determine whether we are sourcing or sinking current, respectively. Though all of the transistors are operating in the saturation region, second-order effects will cause a slight mismatch between cathodic and anodic output currents (see Fig. 9). Monte

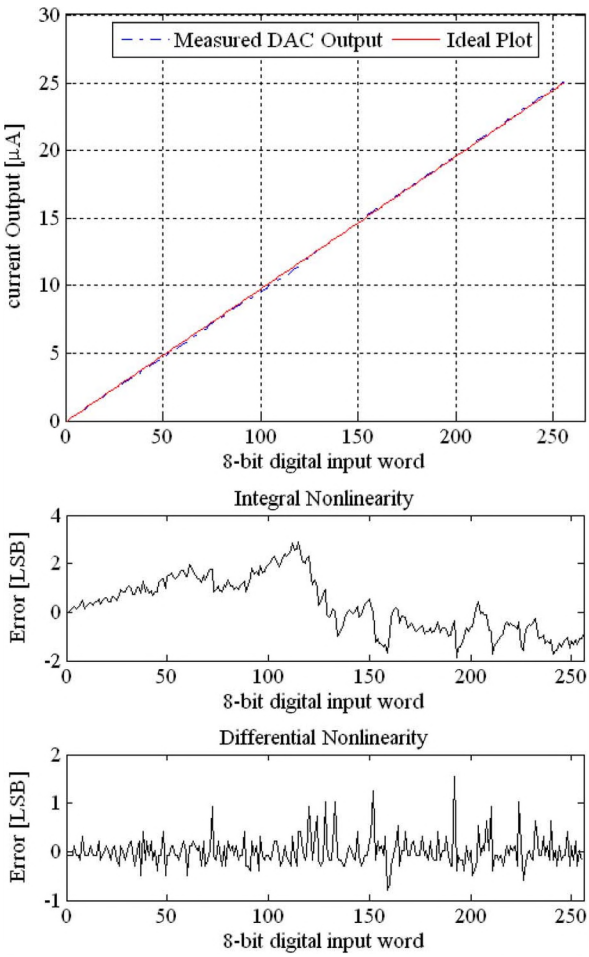
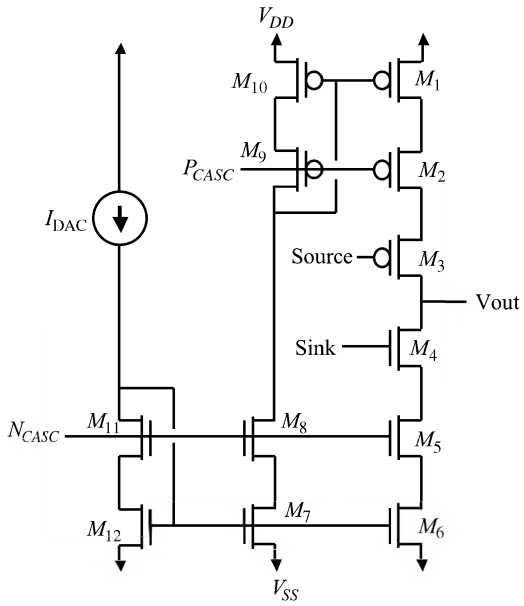


Fig. 7. Measuremnt results from the $R-2R$ DAC: $R-2R$ DAC output range (top) INL and DNL (bottom).



NMOS (W/L)	PMOS (W/L)	M1, M2, M5, M6	M3, M4, M7 - M13
12/1.8	24/1.8	M = 10	M = 1

Fig. 8. Schematic and transistor sizing of the wide-swing cascoded output stage.

Carlo simulations ($N = 1000$) predict current mismatch with a standard deviation of $\sigma = 2.8\%$ at maximum output current; measurements from fabricated stimulators show $\sigma = 1.5\%$ at maximum output current and a $\sigma = 3.2\%$ at minimum current ($N = 40$). This small offset requires an active charge-recovery circuit to bleed off remaining excess charge. The charge balancer must be able to recover the maximum mismatch charge that occurs at the maximum output current (see Fig. 9). We use an operational transconductance amplifier (OTA) configured as a buffer and biased in the subthreshold region to implement a weak charge-recovery operation.

The active charge-recovery circuit in Fig. 10 is used to bleed off or supply excess charge in the surrounding tissue after stimulation. The recovery circuit acts as a small secondary sink or source dependent on the residual charge remaining in the tissue. The more the voltage on the electrode differs from the reference voltage, the more current is sunk or sourced to the electrode. The active recovery circuit is implemented on each individual stimulation site and runs in parallel while other simulation sites may be activated. A residual charge of 1.7 nC would result from a mismatch of 3.5 μA of current (see Fig. 9). A current of 220 nA would be required to remove the excess charge if the fastest repetition (168 Hz) were programmed. The basic current-mirror transconductance amplifier was designed to have a maximum current output of $\pm$235 nA. The time constant of the recovery circuit is highly dependent on the electrode tissue interface impedance. A resistive and capacitive model of an electrode developed by [29] was used to measure the time constant. The recovery circuit has a time constant of 76 ms and an effective resistance of 500 kΩ for small voltage deviations, while current is safely limited to $\pm$235 nA for large voltage excursions (Fig. 11). This effective resistance acts to remove any charge remaining on the electrode capacitance after stimulation. Typical resistive components of stimulation electrodes are much less than 500 kΩ, and will have little effect on the discharge time constant. The recovery amplifier consumes only 2100 μm^2 compared to the 7500 μm^2 needed to implement a passive 500-kΩ resistor. Using a passive resistor for charge recovery would require additional control circuitry to limit currents at high electrode voltage excursions, while the recovery amplifier limits recovery current without the need for explicit control circuitry. The analog stimulation components on INIS (DAC, output stage, and charge-recovery circuits) consume 10.8% of the 25 mW dissipated by the chip during worst-case operation (all electrodes stimulating at maximum current in round-robin fashion).

The digital components on a single stimulator store and control the parameters of the biphasic current pulse. The communication to the external world happens via the global FSM. The global FSM decodes the incoming command bits to obtain a specific site address as well as preparing the data to be stored in the registers for the individual electrode. The global FSM routes the command data to the correct stimulator location. It also serves as a handshaking tool that ensures that the data are properly stored before allowing access to another site. The internal FSM for each site is used to store the data transmitted

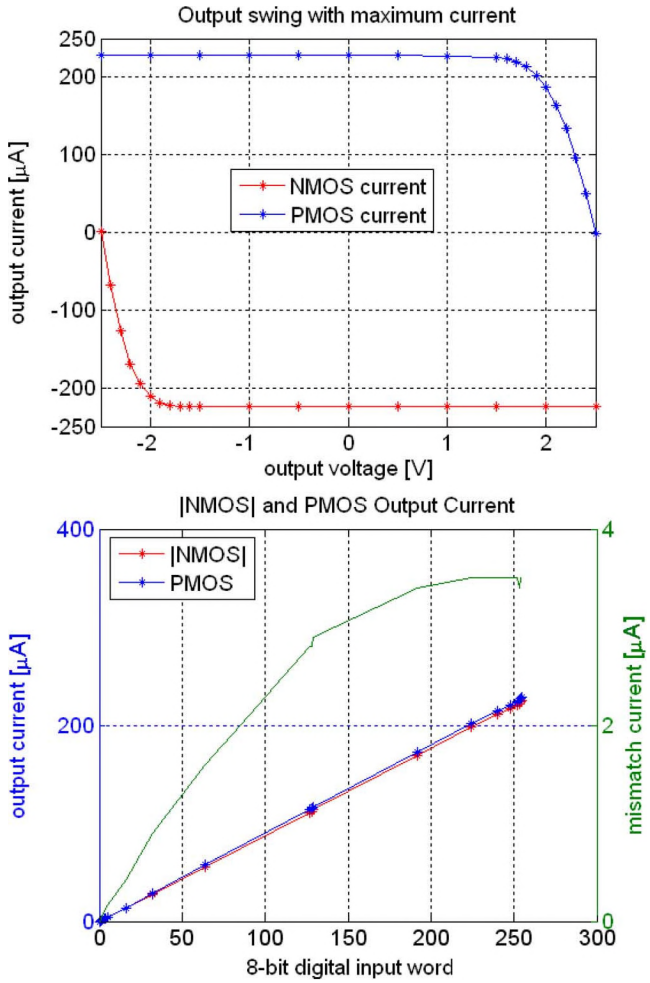
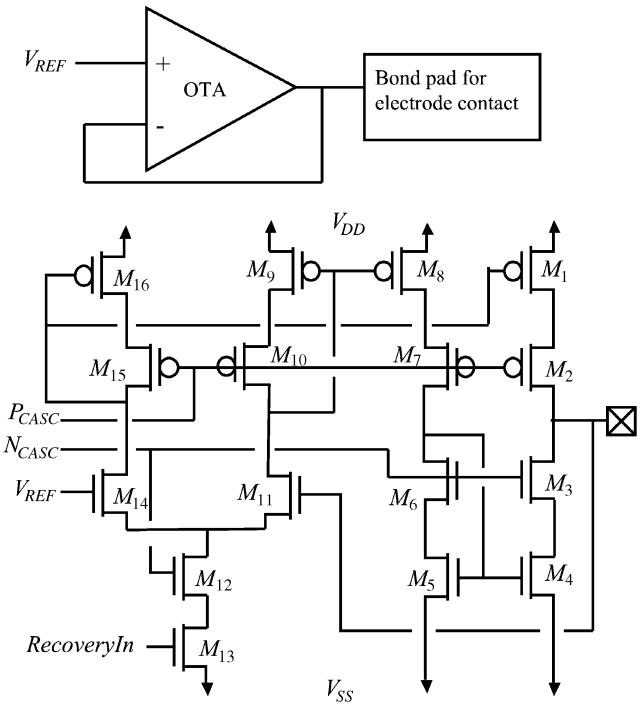


Fig. 9. Measurement results from silicon for the outputs stage showing the output swing voltage (top) and output current range and typical mismatch current from anodic and cathodic currents (bottom).



NMOS (W/L)	PMOS (W/L)	M11 and M14 (W/L)
12/1.8	24/1.8	6/1.8 M = 8

Fig. 10. Schematic of charge-recovery circuit with transistor sizing.

from the global FSM to the site registers. The onsite FSM, along with a counter, controls the timing for the biphasic pulse. Each stimulator contains four registers to store the amplitude, duration, interphasic delay, and repetition rate. Each stimulator has independent parameters that, once programmed, are self-maintained and that may be reprogrammed (changes will take effect next time a firing sequence occurs) or shut down at anytime with a global reset. The amplitude register consists of 8 b, and allows the current to range from 1–255 μA with a resolution of 1 μA. The duration register consists of 9 b, allowing the duration to range from 1.45–370 μs with a resolution of 725 ns. The interphasic delay register has the same scale and resolution as the duration register. The repetition register consists of 9 b, but the highest order bit is used to determine whether the cell is active or not. The actual repetition rate range is 0.66–168 Hz, with a repetition period resolution of 6 ms. Having the registers on-chip and local to each stimulator gives precise, reproducible control over each biphasic pulse. With all 100 stimulators active (in round-robin fashion) at maximum output current, the digital components on INIS consume 82.8% of the total chip power. The switching gates of the local FSMs consume most of this power. Much of this power dissipation could be circumvented by implementing clock gating to reduce switching activity in unused stimulators.

An important system-level digital component in our chip is the token cell. If all of the stimulators were firing simultaneously, the power dissipation would exceed a safe limit, given thermal safety considerations for the surrounding tissue. As a safety precaution, a token method was implemented to coordinate chip-wide stimulation patterns. Individual stimulation cells may fire a pulse only if the token is present in the current cell. When the token enters the cell, the internal FSM checks to see whether the firing sequence needs to be executed. If a current pulse is due, the cell performs the firing sequence and then immediately passes the token along to the neighboring stimulator. If a current pulse is not due at a particular stimulator, then the token is simply passed to the next site with a delay of one clock cycle, with the final cell passing the token back to the first cell. This token system prevents two electrodes from firing simultaneously. This limits power dissipation to safe levels, and prevents having overlapping currents that are generated simultaneously by different electrodes acting at a common neuronal site. However, these advantages come at the expense of true simultaneous multielectrode stimulation; affecting the stimulation frequency; and limiting truly independent stimulation patterns at each electrode. In the (unrealistic) upper limit in which all 100 electrodes are activated with the maximum pulse width of 370 μs, the maximum stimulation frequency for any one electrode would be 9.1 pulses/s.

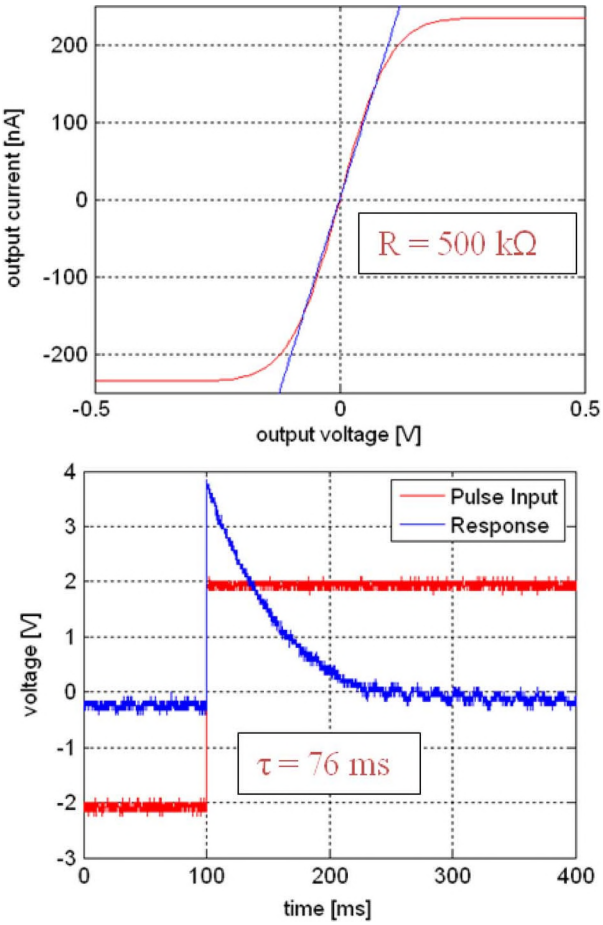


Fig. 11. Measurements of charge-recovery circuit showing measured IV characteristics (top) and time constant (bottom).

TABLE I
INIS SIMULATED AND MEASURED SPECIFICATIONS

Parameter	Simulated Value	Measured Value	Units
Duration	1.45 – 370	1.45 – 370	μs
Interphasic Delay	1.45 – 370	1.45 - 370	μs
Repetition Rate	0.66 – 168	0.66 - 168	Hz
Amplitude	1 - 255	0.85 - 216	μA

III. BENCHTOP TESTING

After fabrication, the INIS chips were first tested for basic functionality in a benchtop configuration. In general, the actual specifications of the fabricated chips were close to the simulated values. However, because of process variations, the on-chip bias generators produced slightly smaller currents than the nominal simulation values. This limited the total output current to a range of 0.85 to 216 μA. Table I shows a summary of INIS specifications from benchtop testing.

Several specifications that were designed and subsequently achieved in the fabricated chip make the chip well suited for mating with a USEA or UEA and provide advanced stimulation capabilities suitable for a neuroprosthetic device. For example,

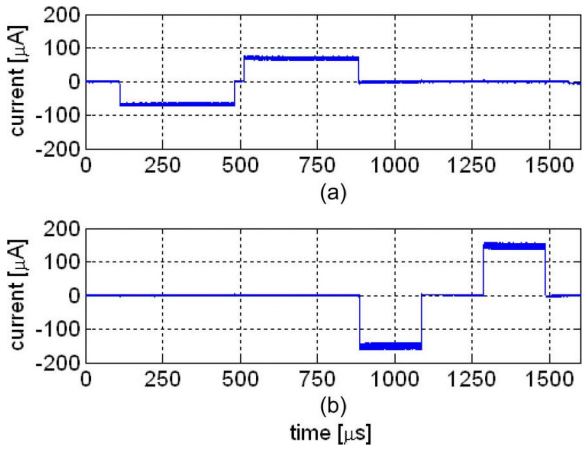


Fig. 12. Stimulation pulses over 10-kΩ resistive load with the following parameters: (a) electrode 1 programmed with amplitude of 75 μA, duration of 370 μs, and interphasic delay of 30 μs and (b) electrode 2 programmed with an amplitude of 150 μA, duration of 200 μs, and an interphasic delay of 200 μs.

1) having 100 different stimulators on the chip allows each USEA electrode to be activated individually. In turn, having multiple stimulation sites provides relatively comprehensive access to the different pools of sensory and motor nerve fibers, resulting in finer sensory discrimination and motor control. Having 100 stimulation sites also allows the use of more biologically realistic, combinatorial patterns of activation of different nerve fibers. 2) The 1-μA, 725-ns, 8-b resolution allows fine gradations of stimulus strength, which is helpful when recruitment curves are steep, or when the desired stimulus strengths are small due to the use of intrafascicular electrodes (e.g., Fig. 16). 3) The relatively wide range of stimulus strengths (controlled by stimulus amplitudes and durations) further allows for activation ranging from single fibers or very small numbers of fibers to activation of all or nearly all of the fibers in a given nerve fascicle. 4) The ability to provide a short interphasic delay can lower stimulation thresholds for biphasic stimulation by avoiding suppressing action potentials that would otherwise be recruited by the first pulse, while still preventing the potential accumulation of undesirable Faradaic processes [30]. 5) The repetition rates of the chip fall within the range of normal physiological firing frequencies. However, as noted before, a limitation of the token system is that these maximal firing rates may not be achieved if multiple different stimuli need to be delivered together. Advantages of the token system and preventing two electrodes from firing simultaneously include keeping power dissipation to safe levels, and preventing summation of stimulation currents that would recruit additional, unwanted nerve fibers.

Figs. 12 and 13 show (at different time scales) biphasic pulses generated during a benchtop experiment with power, clock, and command signals delivered wirelessly over an inductive link. The experiments were performed with a simple 10-kΩ resistor acting as a simplified electrode model. Electrodes 1 and 2 were successfully programmed with pulses of different current amplitudes, durations, interphasic delays, and repetition rates. Note

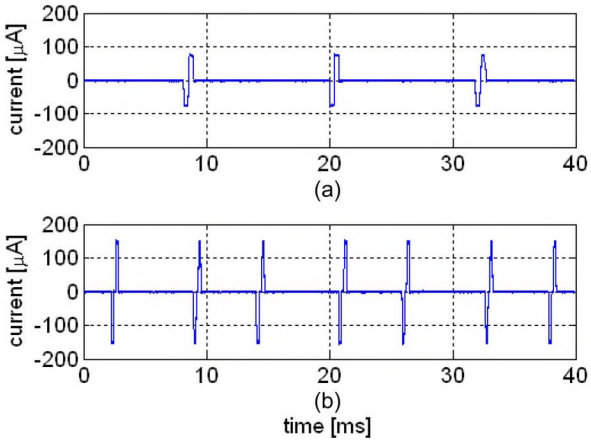


Fig. 13. Stimulation pulses from Fig. 12 viewed on a wider time scale: (a) electrodes 1 was programmed with a repetition of 88 Hz and (b) electrode 2 was programmed with a repetition rate of 166 Hz.

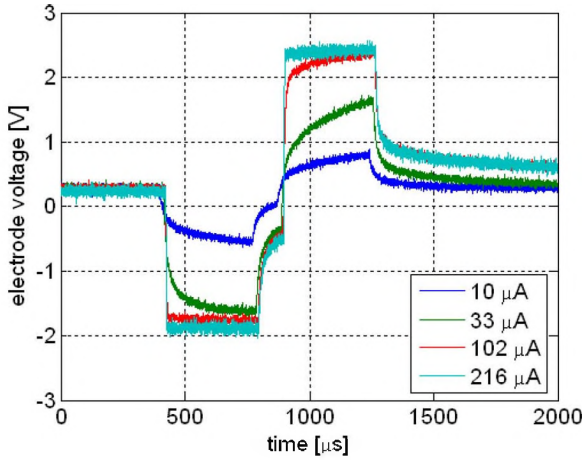


Fig. 15. Electrode voltage curves *in vivo*, captured while stimulating the sciatic nerve of an anesthetized cat.

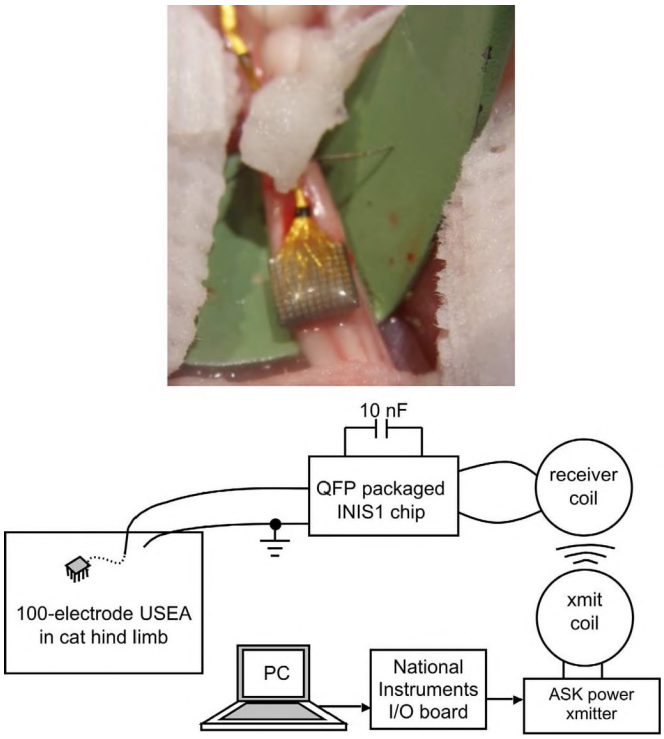


Fig. 14. Diagram showing the *in-vivo* stimulation setup (bottom) using a 100-electrode USEA inserted in the sciatic nerve in cat hind limb (top).

that electrode 2 begins to fire as soon as electrode 1 finishes its firing sequence, because of the token method described earlier.

IV. *In-Vivo* Experiments

In brief, to validate the operation of the INIS chip with biological tissue, we performed *in-vivo* nerve stimulation experiments. A conventional, wired USEA was first inserted into the sciatic nerve in the left leg of an anesthetized cat. Subsequently (Fig. 14), the INIS chip was connected to the wired array and was used to stimulate the nerve through various individual electrodes in the array. The most important finding is that the INIS was able to activate motor and sensory nerve fibers via multiple different electrodes.

Since complete flip-chip integration is not yet complete, all experiments were performed using an INIS chip on a small circuit board. A single stimulator channel from the chip was connected to an electrode on the wired USEA that had been implanted in the sciatic nerve, and the chip ground was wired to a platinum reference wire near the array (see Fig. 14). Although we could have connected the chip's outputs to multiple different electrodes, we typically stimulated only one electrode at a given time, to allow a straightforward interpretation of the evoked responses. The only other off-chip components connected to the chip were a 10-nF capacitor and a 5.8-cm power receive coil (a resonating capacitor is not needed while using the larger receive coil). Power, clock, and command signals were sent wirelessly from a 5.8-cm transmit coil positioned 1.8 cm from the receive coil.

As expected, the measured voltage on a USEA electrode during INIS stimulation co-varied with the current amplitude (Fig. 15) and duration. The shape of the electrode voltage curves reveals the resistive and capacitive elements of the electrode-tissue interface. When stimulation was delivered through this electrode with a pulse duration of 370 μs, current amplitudes greater than 15 μA evoked observable muscle twitches in the leg. At current levels between 33 and 100 μA, the electrode and tissue impedance limited the amount of charge that could be injected into the tissue given our limited compliance voltage, as indicated by the curves in Fig. 15. This constraint may impose important practical limitations on stimulation capabilities for high-impedance electrodes, or in chronic preparations in which the impedance of tissue near the electrodes may rise.

We tested the ability of INIS to recruit physiological responses on 10 of 74 USEA electrodes that had previously been demonstrated to be capable of evoking motor responses via 2.2-V, 370-μs monophasic negative pulses delivered by a conventional stimulator connected to the implanted wired array. On all 10 electrodes, stimulation via INIS was able to recruit motor responses, as monitored visually and via EMG wires implanted in four leg muscles. Motor responses evoked by INIS were studied more systematically for two electrodes by varying the duration (Fig. 16) or the amplitude (Fig. 17) of the stimulus

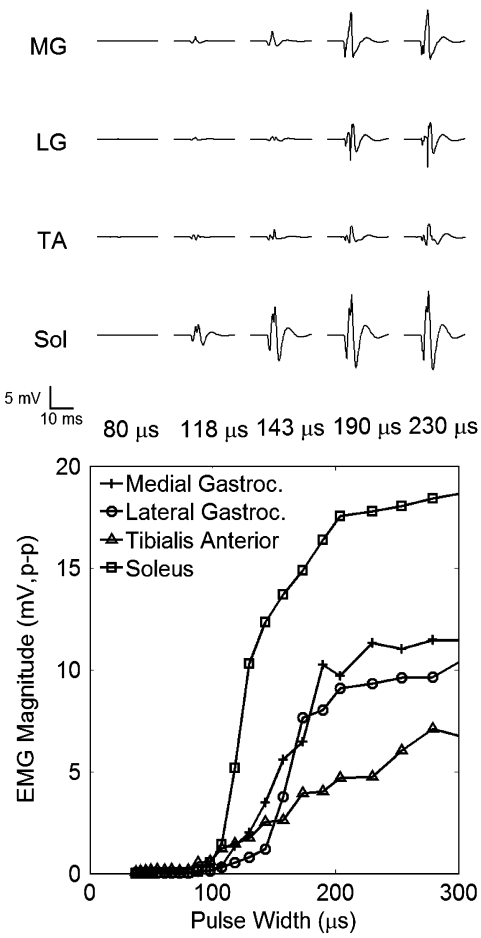


Fig. 16. Evoked raw (top) and quantified (bottom) EMG activity resuling from INIS 216-μA pulses with durations as indicated.

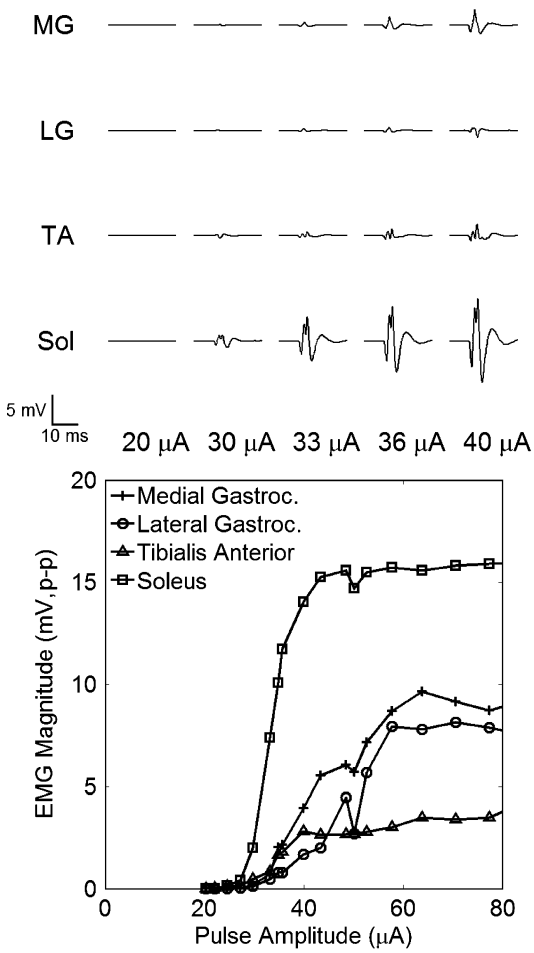


Fig. 17. Evoked raw (top) and quantified (bottom) EMG activity resulting from INIS 370-μs pulses with amplitudes as indicated.

pulses, and measuring the amplitude of the results evoked compound muscle action potentials. For both electrodes, the evoked responses grew systematically with increasing stimulus strength (either amplitude or duration), and the activation of muscles showed a high degree of selectivity. In some instances, EMG responses saturated below 100 μA perhaps because of INIS's limited compliance voltage. Nonetheless, strong muscle contractions were produced at this level of stimulation. These results indicate that the wireless chip, via modulation of either the amplitude or duration of pulse stimulus pulses delivered to array electrodes implanted in nerve, can evoke selective, finely graded motor responses. These capabilities could be used, for example, to restore coordinated, fatigue-resistant movement to paralyzed muscles after spinal cord injury, by activating the motor nerve fibers that still innervate the muscles but no longer receive commands from the brain.

Stimulation via INIS also elicited evoked potentials (EPs) in primary somatosensory cortex, as monitored by recordings from screws in the overlying skull. EPs exhibited a short onset latency (5 ms) and were spatially localized over somatosensory cortex (Fig. 18). Further, cortical EPs persisted after severing the nerve distal to the array, which abolished muscle contractions and, hence, possible secondary activation of sensory systems. These results indicate that INIS can also directly activate

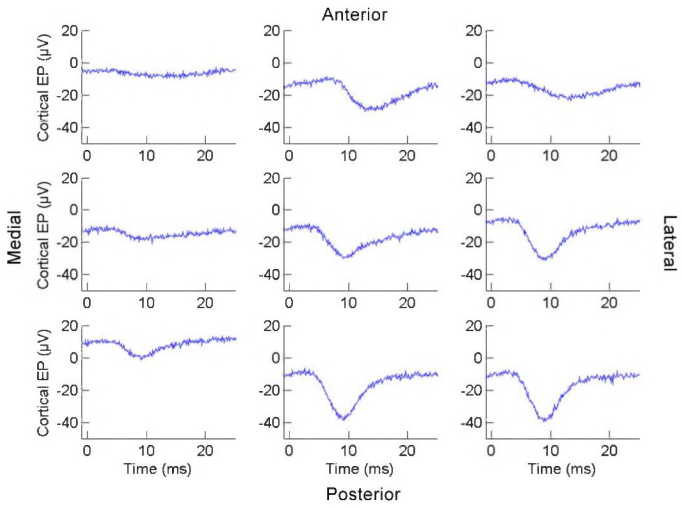


Fig. 18. Wireless stimulation of the sciatic nerve evokes potentials localized over primary somatosensory cortex. Each trace represents the averaged EP recorded from one of nine skull screws in a 3 × 3 grid with ~5-mm spacing.

sensory nerve fibers and, thus, may be able to provide illusory tactile or proprioceptive information. These capabilities could be used, for example, to restore somatosensory sensation after

limb loss or spinal cord injury by activating peripheral or central neural tissue in response to signals received from sensors in prosthetic limbs, or signals from the peripheral nervous system, respectively.

V. Conclusion

We have demonstrated *in-vivo* functionality of a programmable wireless neural stimulation chip that produces biphasic current pulses with an active recovery circuit. The precise and reproducible digital control of the nerve stimulator allowed us to elicit continuously varying muscle contractions from nerve stimulation. Wireless operation provided isolation and remote configurability of the IC. This chip ultimately will be bonded to the back of a USEA or UEA, producing a fully implantable neural interface capable of nerve or cortical stimulation.

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