Temperature Dependence of Equivalent Circuit Parameters Used to Analyze Admittance Spectroscopy and Application to CZTSe Devices

A.E. Caruso[1], D.S. Pruzan[2], V. Kosyak[2], A. Bhatia[2], E.A. Lund[1,3], C. Beall[4], I. Repins[4],and M.A. Scarpulla[1,2]

[1] Electrical and Computer Engineering Department, University of Utah, Salt Lake City, UT, USA
[2] Materials Science and Engineering Department, University of Utah, Salt Lake City, UT, USA
[3] Chemical Engineering Department, University of Utah, Salt Lake City, UT, USA
[4] National Renewable Energy Laboratory (NREL), Golden, CO, USA

***Abstract* — We present a device physics and equivalent circuit model for admittance spectroscopy of CZTSe based photovoltaic devices. The experimental variations of the capacitance and conductance in the depletion width are reproduced for state of the art coevaporated CZTSe devices. We will show that simple Arrhenius analysis of the main capacitance step seen in CZTSe results in erroneous values for the dominant acceptor energy. We will also show that the bulk resistivity in the quasi-neutral region (QNR), even in the presence of the dominant acceptor freezeout, cannot account for the observed increase in series resistance which is responsible for the temperature dependent frequency shift of the capacitance step. Thus, we suggest that dopant freezeout must affect another component of the lumped series resistance such as a non-Ohmic back contact.**

***Index Terms* – admittance spectroscopy, CZTS, CZTSe, equivalent circuit, capacitance methods**

I. Introduction

Temperature admittance spectroscopy (TAS) is typically used to characterize majority-carrier trap levels within thin film photovoltaic devices, but it has also been shown capable of measuring band offsets and dopant freezeout [1], as well as the origins of majority carrier mobility, non-Ohmic contacts, and minority carrier lifetimes [2]. There have been multiple proposed methods for accurately analyzing admittance data, many of which are centered on the creation of a minimal equivalent AC circuit representative of the device [3]–[7].

Here we develop an RC equivalent circuit representing the depletion width, quasi-neutral region, and lumped series resistance of single junction solar cells. The circuit parameters are coupled through the device physics of a one-dimensional p-n junction, reducing the number of free parameters. Through device physics we will propose that the coupled circuit parameters have non-negligible temperature dependencies that to our knowledge have yet to be examined. We apply the model to data taken for copper zinc tin selenide (CZTSe) devices. The behavior of CZTSe is complex due to freezeout of its dominant acceptor at relatively high temperatures [8]. CZTSe is illustrative of the behavior of many vexing yet technologically important materials including also GaN [9] and CdTe for which shallow acceptor doping is difficult.

The widely-observed temperature dependence of the main depletion-width-related capacitance step for CZT(S,Se) devices has been fairly-commonly erroneously analyzed as a trap state [10]. More correct analyses attribute the temperature/frequency shifts of this step to the temperature dependence of the lumped series resistance (R_S). [3], [11]. While Ref. [3] measured R_S empirically without seeking to explain it, the mathematical form assumed in [11] and citing works assumes that R_S is dominated by the freezeout (temperature dependent ionization) of holes from the valence band to the non-shallow acceptor within the quasi-neutral region. We demonstrate here that such assumptions do not stand up to careful scrutiny and instead suggest that the temperature dependence of the capacitance step is driven by the effects of acceptor freezeout on a non-Ohmic back contact as has been suggested for the N1 defect in some CIGSe devices [12]. This may be explained by the shared Mo/metal chalcogenide back contact interface in both device types.

II. Model

Throughout the literature on capacitance measurements for CZT(S,Se) there is agreement that the depletion width (W_d) should be represented by the three parameter equivalent circuit first described by Schofield [4]. Additional circuit elements and corresponding explanations have been used for other types of thin film devices [4]–[7]. We utilize an equivalent circuit that combines properties of these prior models and incorporates device physics. Fig. 1 shows the proposed base circuit consisting of series resistor and two parallel RC loops which represent the depletion region and the quasi-neutral region (QNR) since any device having a depletion width (W_d) and quasi-neutral width (W_{QNR}) should always exhibit an equivalent circuit having two separate, but coupled loops. Whether both loops are observable in admittance data will depend on parameter values.

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The physical interpretation of any equivalent circuit used to fit TAS data should account for parameters associated with the junction and quasi-neutral region first and only later ascribe effects to further elaborations of the circuit such as traps and back contact depletion widths, which we will discuss in more detail.

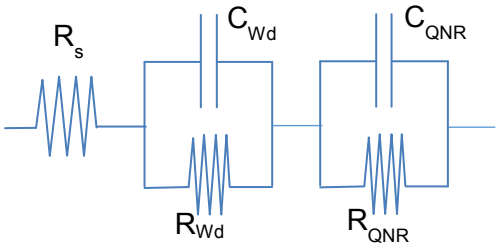

Fig. 1. Equivalent AC circuit, R_{QNR}, C_{QNR}, R_{Wd}, and C_{Wd} are the resistance and capacitance of the quasi-neutral region (QNR) and depletion width (Wd) respectively. R_s represents all series resistances arising outside of the QNR.

Since the thickness of the device (L) is constant and W_d + W_{QNR}=L, the R and C parameters of these two regions are coupled. This dependence allows us, instead of fitting the data with ambiguous circuit parameters, to constrain the circuit parameters to fundamental device parameters such as the built-in voltage (V_{Bi}) and valence band hole concentration (p). These constraints should allow for more physically accurate results because they are governed by basic device physics.

III. Device Physics Analysis

In order to most accurately relate the elements of the circuit to the physics of the device we must first gain an understanding of the response of these elements at different temperatures. It has previously been assumed that the junction capacitance is independent of changes in temperature [3], however this cannot be strictly true. Even in the absence of carrier freezeout, the junction capacitance of p-n homojunctions increases substantially over the typical temperature range of admittance measurements (50-350 K) meaning that, in general, devices will always exhibit temperature dependent junction capacitance. The temperature dependence of the junction capacitance was first modeled for a Si p-n long diode for which the p-type doping was held constant at 10^{16} /cm^3 and the n-type doping varied to near-degeneracy.

The qualitative behavior, shown in Fig. 2, is that the junction capacitance reaches its lowest value at 0 K and increases approximately 50% between this value and room temperature. The same analysis was done, with the appropriate modifications, for an n^+p heterojunction (where n^+ implies degeneracy) such as n^+-Cds/p-CZTSe. The n^+p heterojunction shows an increase of about 15% between 0 K and 400 K which is substantially less than that of the homojunction example but nonetheless shows temperature is a contributing factor that can be taken into consideration. The case of dominant p-type dopant freezeout in heterojunctions was also studied. The results are similar outside of the step-like feature added by the dopant freezeout.

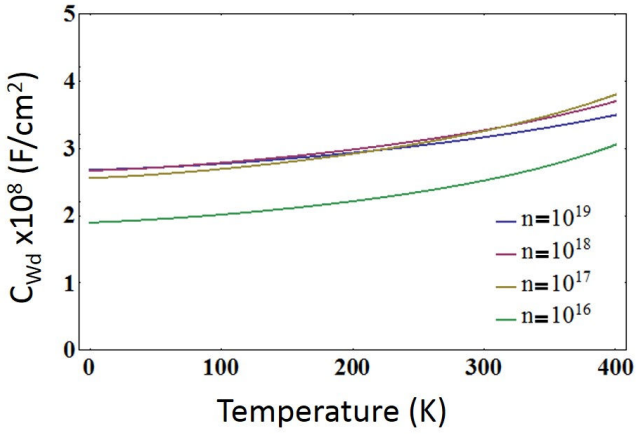

Fig. 2. Temperature dependence of junction capacitance as modeled for a Si p-n junction with constant p-type doping of 10^{16} /cm^3 and n-type doping varied to near degeneracy

In the 1D n^+p heterojunction model, the depletion width is expressed as (including the Debye tail on the p-side)

$$W_d = \sqrt{\frac{2\varepsilon(V_{bi}+V-k_BT/q)}{q(N_A-N_D)}} \quad (1)$$

where ε is the permittivity of the absorber layer, V is the DC bias voltage, T is the temperature, N_A - N_D is the net ionized carrier concentration in the p-type layer and V_{bi} is the built in voltage. The built in voltage for an n^+ window/ p absorber junction can be expressed as

$$V_{bi}(T) = E_g(T) + \Delta E_c + k_BTlog\left[\frac{N_A-N_D}{N_V(T)}\right] \quad (2)$$

in which E_g is the band gap energy of the absorber layer, ΔE_c is the conduction band offset and N_v is the absorber valence band effective density of states. Temperature dependences were included for the density of states, using the accepted $T^{3/2}$ relationship, and for the band gap energy, using the Varshini model. Dopant freezeout will also cause additional temperature dependencies but this is not considered at this stage.

Dopant and dielectric freezeout in p-n junction devices are distinct processes that will be briefly discussed. Dielectric freezeout occurs when the RC time constant of the sample becomes longer than the period of the probing frequency, for a p-n junction device an example where this can be observed is when the $C_{Wd}R_S$ product becomes too large [11]. Essentially the sample's capacitance cannot be charged and discharged through its own resistance fast

enough. Dopant freezeout, although it may result in increased R_S and thus drive dielectric freezeout, is the process of thermal ionization of dopants to band states.

The net carrier concentration, N_A - N_D, was calculated for a Type I band alignment of CdS to CZTSe with varying acceptor ionization energies (E_A) and compensation ratios $\kappa \equiv N_D/N_A$. For the case of strong compensation ($\kappa \geq 0.5$), which may be present in CZTSSe materials [9], the net hole concentration from an acceptor is given for all temperatures as [13]

$$p(T) = \frac{N_A(1-\kappa)}{1+\left(\frac{\kappa N_A}{\beta N_V}\right)\exp\left(\frac{E_a}{k_B T}\right)} \quad (3)$$

in which β is a degeneracy factor taken to be ¼ for CZTSe. It must be noted that the valence band structure may be more complicated for CZTS(Se) compounds than for more common semiconductors and therefore the degeneracy factor may change [14].

IV. Experiment & Results

For this study n^+p type CZTSe devices were examined. CZTSe is useful for this analysis because of the dopant freezeout observed at relatively high temperatures. The devices were fabricated using coevaporation with an efficiency range of 2.1% to 8.6% the results described below are from a cell with 7.8% efficiency though similar behavior was seen in each. Temperature dependent admittance spectroscopy (TAS) was done using a Quadtech 1920 Precision LCR meter. The magnitude of the oscillating voltage was set to 50 mV and no DC bias was applied meaning that changes in the depletion width were exclusively due to temperature effects. A frequency range of 20 Hz-1 MHz and a temperature range from ~100 – 335 K were studied. The device physics model discussed above, with the addition of a trap in the form of a resistor and capacitor in series with the depletion width, was then used to fit the data. The inclusion of a single trap is representative of any possible levels within the CZTSe bandgap while minimizing the number of free parameters within the model.

The measured parallel capacitance of CZTSe along with the fitted behavior obtained from the device physics model are shown in Fig. 3. As is shown in the figure, CZTSe exhibits a single strong capacitance step that shifts to higher frequencies with increasing temperature. The slope in the data occurring before the step (at temperatures below 195 K) may be attributed to a smearing effect caused by a distribution of parameters such as traps' energy and film thickness. The large step is also associated with dielectric freezeout because the geometric capacitance is observed at higher frequencies.

The effect of each equivalent circuit parameter on the modeled capacitance was observed within the three parameter model by changing each parameter independently to see its effect on the capacitance. This analysis showed that the characteristic capacitance step for CZTSe was most strongly affected by changes to the series resistance. This

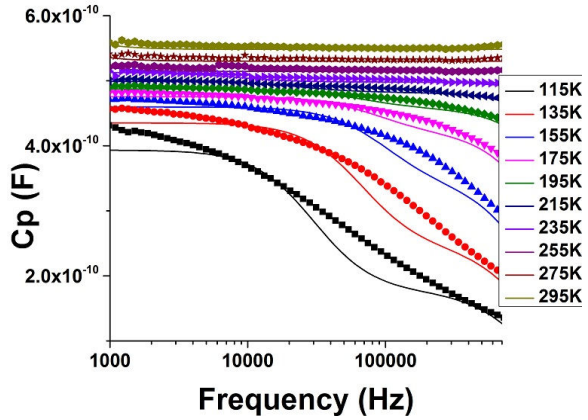

Fig. 3. Measured and modeled parallel capacitance of CZTSe.

result is also supported if we look at the relationship between the characteristic frequency of the capacitance data and the characteristic time constants within the five parameter equivalent circuit model, as shown in Fig.1.

The five-parameter model has six characteristic time constants associated with it corresponding to the three resistors and two capacitors. From the mathematical analysis the only time constant that could be attributed to the capacitance step comes from $C_{Wd}R_s$. This would suggest that the step is not due to effects from the QNR region. Fig. 4, which shows the fitted device resistances from the model shows the changes in R_{QNR} to be negligible when compared to R_s.

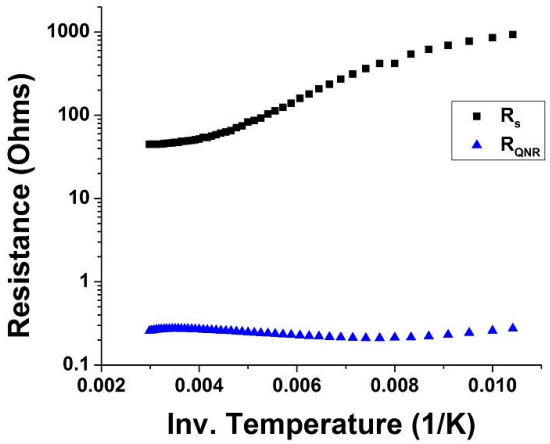

Fig. 4. Device resistances vs. temperature as derived from the fitting based on the equivalent circuit described by Fig. 1. The QNR resistance is negligible compared to the others and therefore will have little effect on overall R_s.

When we look at the contributions to the time constant from C_{Wd} and R_s independently, it is apparent that the series

resistance is the dominant term that causes changes. Series resistance includes any resistances not within the absorber layer of the device. We quantitatively estimated the magnitude of the QNR resistance given its thickness determined by L and W_d. Assuming a mobility near 20 cm^2/Vs and the best-fit (N_A-N_D) at all temperatures, R_{QNR} is simply too small (by a few orders of magnitude) to account for the observed R_S. Thus, it must be concluded that another RC-like component in the system such as a non-Ohmic back contact dominates the R_S. These issues are the subject of our ongoing work.

V. Conclusions

Herein we have presented a method for analyzing admittance spectroscopy from short diode p-n junction devices such as thin film solar cells. We use an equivalent circuit model with more elements than typical, however we constrain their values using the temperature dependent device physics of the junction and quasi-neutral regions. TAS was done for CZTSe and the behavior of the device was investigated. In the case of a CZTSe devices, the resistance of the QNR for reasonable parameter assumptions is simply too small to account for the observed temperature dependent R_S (as is assumed by many). This suggests that the observed freezeout of the main junction capacitance step may be in fact driven by another series resistance contribution such as a non-Ohmic back contact which is also affected by the dopant ionization in the absorber.

Acknowledgements

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