MICRO-ELECTRO-MECHANICAL-SYSTEMS-BASED SINGLE-DEVICE DIGITAL LOGIC GATES FOR HARSH ENVIRONMENT APPLICATIONS

by

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ABSTRACT

This dissertation describes the design, fabrication, testing, reliability, and harsh environment performance of single-device Micro-electro-mechanical-system (MEMS)-based digital logic gates, such as XOR and AND, for applications in ultra-low-power computation in unforgiving settings such as high ionizing radiation and high temperatures.

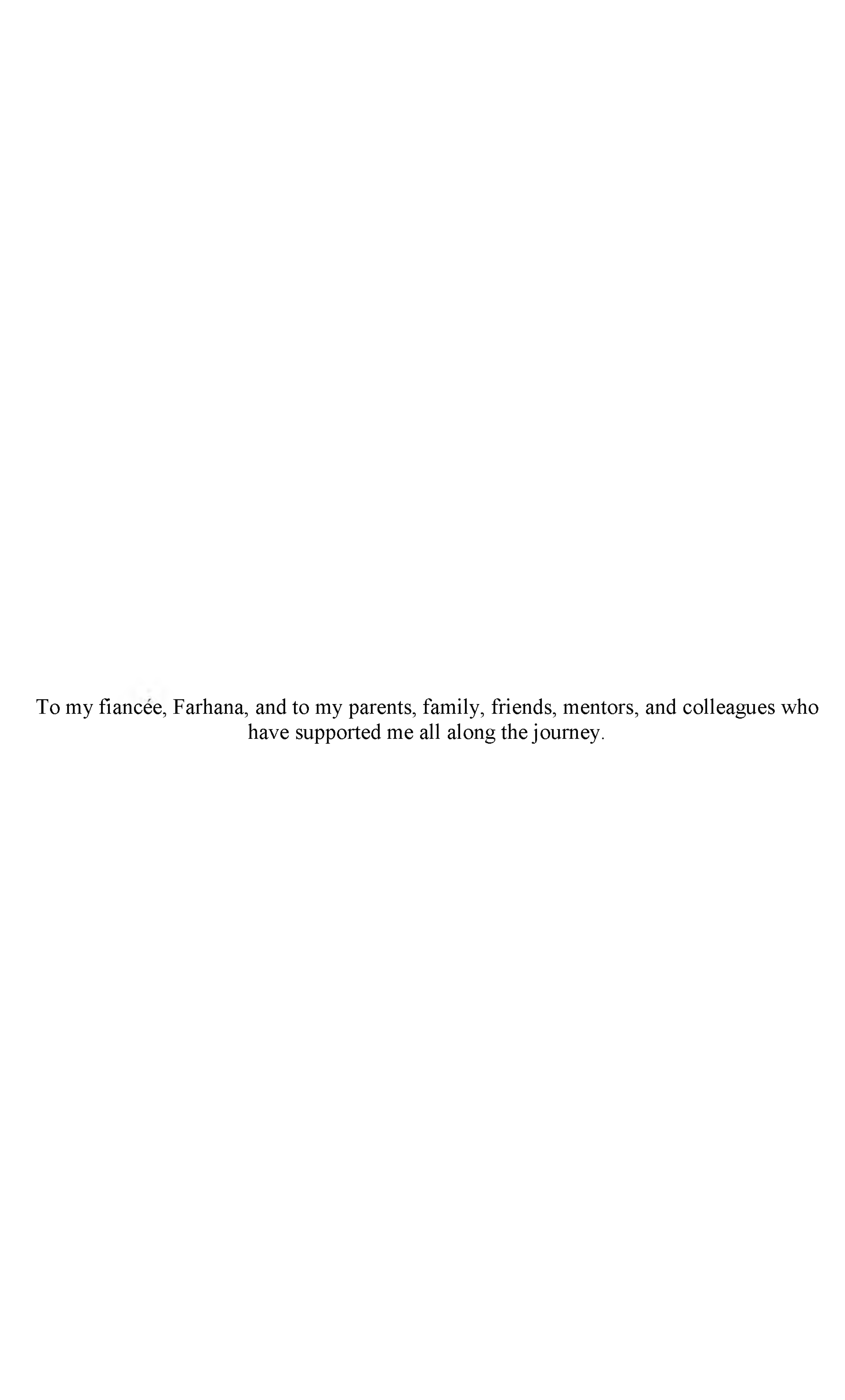
Within the scope of this dissertation are several significant contributions. First, this work was the first ever to report the evolution in logic design architecture from a CMOS-paradigm to a MEMS architecture utilizing a single functional device per logic, as opposed to multiple relays per logic. This novel approach reduces the number of devices needed to implement a logic function by approximately 10X, leading to better reliability, yield, speed, and overall better characteristics (subthreshold characteristics, smaller turn-on/off voltage variations, etc.) and it simplifies implementation of MEMS-based circuits. The logic gates illustrate ~1.5V turn-on voltage at 5MHz with $>10^9$ cycles of reliable operations and low operational power consumption (leakage current and power $<10^{-9}$A, <1μW).

Second, this work is the first ever to report an intensive study on the cycle-by-cycle evolution of contact resistance (R_c) up to 100,000 cycles, on materials such as, Ir, Pt, W, Ni, Cr, Ti, Cu, Al, and graphite, which are materials commonly used in MEMS switches. Adhesion forces between contacts were also studied using a contact-mode-

AFM, force vs. displacement, experiment. Results show that materials with high Young's modulus, high melting temperatures, and high density show low initial contact resistances and low adhesion forces (such as Ir, Pt, and W).

Third, the devices were interrogated separately in harsh environments where they were exposed to high doses of ionizing radiation (90kW) in a nuclear reactor for a prolonged time (120 min) and, separately, at high temperatures (409K). Here, results show that solid-state devices begin to deteriorate almost immediately to a point where their gate can no longer control the drain-to-source current, whereas MEMS switches survive such ionizing radiation and temperatures portraying clear ON and OFF states for far longer.

In terms of the applications empowered and the breadth of topics covered to accomplish these results, the work presented here demonstrates significant contributions to an important and developing branch of engineering



To my fiancée, Farhana, and to my parents, family, friends, mentors, and colleagues who have supported me all along the journey.

"It's about the journey, not the destination."
– Farhana M.

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Attending graduate school has, by far, been the most challenging and, at the same time, the most rewarding period of my life. I have learned valuable lessons on transcending challenges that I previously felt were insurmountable. I learnt to appreciate that failure was an option, sometimes, and realized very quickly that determination and resilience were fundamental to achieving success in all walks of life.

To my advisor, Prof. Massood Tabib-Azar, for whom I have profound respect and admiration: I will be eternally grateful for the opportunity you gave me and the confidence you placed upon me. Through your wisdom and impeccable mentoring, you have always inspired me deeply and guided me on the best path. You perhaps understand better than I the significance of what you have done for me. Thank you.

To my fiancée: You have always been there through thick and thin. Your friendship gives me strength to get back up when I fall and your love gives me courage to fight harder and longer until I succeed. Thank you for being so wonderful! To my parents: Thank you for your high values in education. Had it not been so, I would not have made it this far.

My life, in a sense, is a sum of the influences, large and small, yet, significant, of all those who have played a role in it. This dissertation would not have been possible without all the little pieces in this magnificent puzzle falling together. Thank you, all.

CHAPTER 1

INTRODUCTION

Over the past decade, increasingly greater efforts are being made to maintain semiconductor industry growth in line with Moore's law [1]. Continued progress is speculated to become exponentially complex as various critical issues are foreseen as limiting factors for further scaling. Quiescent power dissipation is one of the most critical factors that are gaining traction as power dissipation increases exponentially with continued scaling. This trend culminates in issues such as limited battery life and inability of cooling systems to remove excessive heat generation. Since 2003, the industry's approach on maintaining Moore's law has seen a diversion from a device scaling down paradigm to one that addresses improvements on the circuit level such that significant circuit modification and performance overhead for leakage reduction was introduced [2]. Nevertheless, this approach mainly targeted the subthreshold leakage while largely ignoring gate and pn-junction leakages, which are now comparable and possibly exceeding subthreshold leakage values as further scaling into the nanometer Complimentary Metal-Oxide-Semiconductor (CMOS) regime continues. These techniques were designed to address advancements in gate leakage reduction; they remain viable into the technology nodes currently in use today (45nm, 32nm, and 22nm). However, the leakage power from other means imposes terminal limitations on CMOS Very-Large-

Scale-Integrated (VLSI) circuits by way of power efficiency, cooling system requirements, and effects from ambient environmental changes. As CMOS is scaled further into the nanometer regime, the intrinsic physical limitations associated with CMOS technology, such as short-channel effects and leakage currents, will result in unmanageable leakage power culminating in reliability issues [3, 4]. If appropriate steps are not taken now, the road to semiconductor technology evolution stops here.

It is obvious now that there is an impending need to seek out other technologies that can facilitate further improvements, preferably, one that is compatible with current CMOS technology, addresses its inherent limitations such as power/energy efficiency and scalability, and is immune to performance deterioration due to ambient environment changes. Some alternative technologies recently developed include Spintronics [5], Carbon Nanotube Electronics [6], and Quantum Dots [7]. Spintronics is a very new realm in electronics that is based on detecting the intrinsic spin of an electron to define binary state. This technology is very promising in terms of reducing power consumption, increasing data processing speeds, and increasing integration densities compared to existing CMOS. Nevertheless, the challenge it faces currently is paramount and requires a colossal research effort to determine effective and reliable ways to detect electron spin. Furthermore, there is no controllable manufacturing technique to reliably fabricate spintronics-active materials or devices feasibly. Much work is needed to advance this field and as a result, these factors hinder the progress in spintronics. Carbon nanotube electronics are promising alternatives to CMOS as they have at least 20-30x higher ON current; however, their metal contact formation and mass fabrication techniques are far from developed to compete with CMOS. The issues with quantum dot technology are

overlapping with those faced by the spintronics and CNT technology as it is still in the experimental stage and requires more time to mature into a commercial competitor.

Microsystems of the "More than Moore" era calls for miniature devices with exceedingly higher performance, functional diversity, reliability, low power consumption, and higher efficiency [8]. Micro/Nano-Electro-Mechanical Systems (MEMS/NEMS) technology can fulfill this need through innovative research techniques coupled to modern technology developed for CMOS. One particular MEMS device that is highly beneficial to microsystems of the future is the MEMS switch [9-12]. Such devices have critical applications for use in phase shifter circuits, tunable RF filters, bio-implants and devices, radiation-hard and harsh environments such as outer space, e.g., space-radars, processors, etc. [9-16].

Simple micro-electro-mechanical switches (MEMS) have been reported for several decades now and this technology poses numerous inherent advantages such as its virtually zero leakage current, no subthreshold conduction resulting in power loss during inactivity, compatibility with existing CMOS technology, possibility to integrate with CMOS circuits on the same chip, scalability, and ability to operate in a multitude of harsh environments, such as high temperatures and high Ionizing Radiation (I-R). MEMS have been reported in the past for applications in processors and to address power management in scaled VLSI, programming interconnect in FPGAs, biomedical devices where it is desirable to reduce leakage power to prolong implanted battery life, and other applications in harsh environments where CMOS cannot operate due to high temperature or radiation [9, 10, 13, 14, 17-21]. One such case includes operation in the presence of I-R in troubled reactors like Chernobyl and Fukushima or at high temperatures encountered

inside combustion engines. In these cases, silicon channel in CMOS becomes highly conductive due to thermal generation of carriers or due to lattice defect generation caused by I-R radiation over prolonged exposure [9]. Space applications also require radiation-hard devices and materials. In some electronic materials such as SiC, the energy required to produce lattice defects is high, enabling these materials to withstand I-R longer than Si. In other materials such as InP, defects heal at relatively low temperatures, enabling them to recover quickly.

NEMS/MEMS devices are based on mechanical elements that are inherently insensitive to I-R. The I-R causes lattice defects in these devices, but these defects do not alter their characteristics the way they affect channel resistance in CMOS. Eventually, large defect densities created over extended I-R exposure leads to embrittlement that may affect NEMS/MEMS electrical and switching characteristics. NEMS/MEMS devices also have very low leakage power, making them very desirable in biomedical implant devices or other applications requiring very long battery lifetime.

Despite their very high off-to-on resistance (100 GΩ to 10 mΩ) ratios, and very low off-state leakage currents ($<10^{-14}$A), MEMS switches tend to be slow (<1 MHz), large (>40 μm^2), and unreliable with limited lifetime of $\sim 10^6$ operation cycles [2-4, 6, 9, 10, 13, 17]. In addition, MEMS/NEMS switches have many interesting and challenging issues, including: a) contact reliability, b) stiction problem related to release during fabrication and micro-welding during hot-contact operation, c) reliability of flexure structures usually used as part of the switch, and d) particulate problems that occur during repeated operations that can lead to switch failure. To address some of these issues, the approach presented here has shifted away from the CMOS paradigm that uses individual

p- and n-MOSFET (PMOS and NMOS) as complementary switches for implementing logic gates to single device functional structures, creating a platform for improved density, reliability, speed, and fabrication yield. The devices are based on a composite Si_3N_4/Polysilicon cross-bridge platform with metal contacts designed to provide XOR or AND capability from a single actuating structure. The following sections elaborate on the functional structure design, fabrication process, testing, and the results of these novel single device XOR and AND logic gates.

1.1. Significance of this Work: MEMS Logic Circuits and Microprocessors

To enable computation using MEMS, individual MEMS relays have been combined in the CMOS paradigm (P-NEM and N-NEM) to create logic functions [13, 17, 21-23]. There are clear advantages of MEMS switches over solid state transistors, as discussed earlier. Nevertheless, designing computational circuits with MEMS switches using the CMOS circuit design paradigm would imply combining a group of MEMS transistors to perform a single logic function and multiple such groups to form a computational circuit. The disadvantages of such an approach are rather apparent. There will be several mechanical delays within each logic operation, which is further exacerbated as the complexity of the circuit increases. The reliability drops exponentially as the number of mechanical transistors increases. The need for larger driving voltages to account for fan out voltage drops is also of significant concern. Additionally, the area required to set up the circuits is fairly large and the overall speed of the circuit is very low.

Now, consider changing the circuit design paradigm such that instead of grouping the MEMS switches to form simple gates, as is done with CMOS, the MEMS switches are combined together to operate in parallel such that a single mechanical delay results in a single logic operation. Furthermore, if this were extended to create a universal structural form that offered a single logic operation per switching cycle, along with a design so flexible that merely changing the electrode pattern offers an altered logic gate, it stokes the possibility of a mechanical microprocessor that eliminates the obvious disadvantages of MEMS-CMOS paradigm computation and runs at a fraction of the power that is required by current CMOS microprocessors. Additionally, such a paradigm will offer a savings on semiconductor real estate, translating to a much lower cost per chip. Of course, the speed will be lower compared to CMOS circuits; however, what the MEMS logic gates lack in speed, they more than make up for in terms of energy efficiency. By only requiring a fraction of the energy to run a circuit, one can dream up a whole gamut of new ultra-low-power applications that can run off scavenged energy from acoustic vibrations, light, or ambient radio signals on the fly. In terms of competing with CMOS scalability, studies have shown that MEMS and NEMS relays are scalable down to the deep submicron regime where current CMOS technology nodes are operating, and struggling to scale further [19, 20, 22, 24]. NEMS will not be limited by the adversities that plague CMOS at these nodes and beyond.

Another realm to which MEMS-based computation contributes significantly is that of enabling applications in harsh environments such as high temperatures and ionizing radiation. Such are the cases inside combustion engines, technologies facilitating rescue efforts in adversity stricken nuclear reactors, (like Chernobyl in 1986 and

Fukushima in 2011), deep outer space exploration, etc. Current techniques of radiation hardening of VLSI devices include utilizing insulating substrates instead of semiconductors, such as SiO_2 or sapphire, or even wider band gap semiconductors such as silicon carbide or gallium nitride, using shielding, designing circuits with BJTs instead of MOSFETS, as the former is less vulnerable to I-R, using MRAMs for memory, parity bits for logical error correction, etc. Nevertheless, these solutions are only slightly more reliable in harsh environments compared to their traditional non-rad-hard equivalents. The damage caused by I-R is by inducing displacement charges and ionization charges that, in CMOS, form mid-gap states, facilitate charge trapping at interfaces and oxides, and change doping characteristics amongst many other complications. A high temperature environment also generates detrimental charges in a similar fashion. A MEMS-based microprocessor solution, on the other hand, provides significant improvement, as the principle of operation here is based on requiring a physical connection between two contacts (separated by an air or vacuum gap) and not on the requirement of a solid-state conducting channel for its operation, like in CMOS. MEMS switches are not detrimentally influenced by the stray charges generated by I-R or high temperatures in the same way that they are in solid-state transistors. Such circuits benefit from not requiring additional resources for shielding and protection from harsh environments. One can even extend speculation that a future MEMS-based portable computer be self-powered by scavenging energy from such harsh environments.

As a result, based on the discussions presented in this section, it is evident that MEMS-based logic gates and their concomitant computational circuits are a significant

contribution to the development of ultra-low-power computers of the future that can also inherently survive harsh environment operation.

1.2. State of the Art MEMS Switches and Logic (Literature Review)

CMOS technology has driven the semiconductor industry to produce astounding devices for the past few decades. No matter how great the strides of technological advancement were in the past, it is getting harder to cope with the power and energy density needs of next-generation devices. Today, the requirement of ultra-low-power devices is far more pressing than ever before. It is gradually becoming universally evident that MEMS-based switches reveal potentially zero leakage current in the off-state, extremely low resistances in the on-state, and a much steeper subthreshold switching slope. In addition, it is known that MEMS RF switches have advantages in high isolation and low insertion losses compared to solid-state devices. Currently, there is a demand for a new technology that is not adversely affected by the scaling effects seen in CMOS, while, preferably, remaining compatible with multibillion dollar semiconductor industry fabrication lines. The field of MEMS has seen recent advances in their use as switches (or relays), logic gates, memory components, variable capacitors, RF device components, and wireless communication components. MEMS and NEMS devices are gradually but surely achieving the status quo of devices relying currently on CMOS and VLSI and are a strong contender for transition into microsystems of the "More than Moore" Era.

This study summarizes the most recent advances in the area of MEMS and NEMS devices, their working principles, and a brief discussion of their features, parameters, and performances.

1.2.1. MEMS Switches and Logic Devices

There has been increasing interest in the area of MEMS switches as logic gates for ultra-low-power applications. A single-step fabricated, symmetric, laterally actuated, platinum-coated-polysilicon cantilever beam and fixed-fixed beam NEM relay has been reported [14, 25]. Fig. 1.1 provides some SEM images of the fabricated device, and its operational characteristics. This design incorporates stiffened beams and serpentine structures to reduce actuation voltage and also report overdrive voltages over 100% without failure. Actuation gaps of 500nm and voltages of ~12V for clamped-free and ~26V for clamped-clamped structures are reported. The devices are said to show 3kΩ contact resistance and operations as high as 10^8 cycles. In addition, they report testing the device in ambient environments, as well as immersed in oil – showing lowered actuation voltages.

An analytical model on suspended gate-FETs (SGFET) has been developed and published [26]. These devices are a combination of an electrostatically actuated NEMS switch and a MOSFET (Fig. 1.2). The clamped gate electrode allows the MOSFET to circumvent high current limitation in lowering the threshold voltage in order to lower standby power consumption. As this technique is CMOS-compatible, SGFETs can be mass fabricated alongside CMOS.

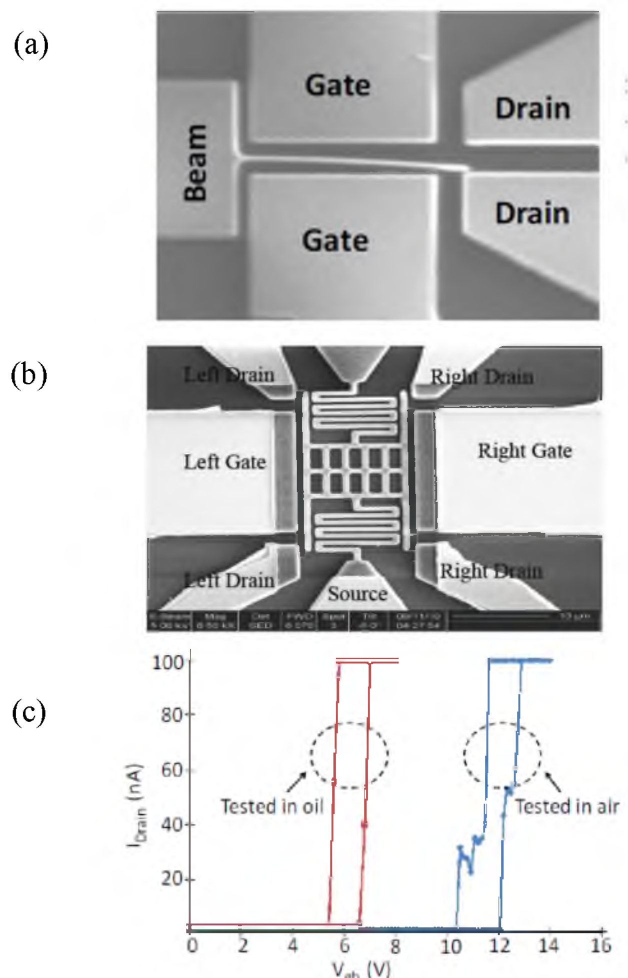

Figure 1.1: Single-step fabricated, symmetric, laterally actuated, platinum-coated-polysilicon NEM relay's (a) SEM showing with 14.2μm-long beam. (b) SEM showing clamped-clamped serpentine design (c) I-V results of the device being tested in air and in oil [14, 25].

In order to provide a thorough understanding of the device operation, the authors delve into details of the relationships governing pull-in, pull-out, and stable travel range (Fig. 1.3) based on the depletion approximation as a function of structural parameters. Also, the article develops a relationship between a movable MEMS gate alongside standard MOSFET models and highlights the potential of using SGFET as an ultra-low-power switch.

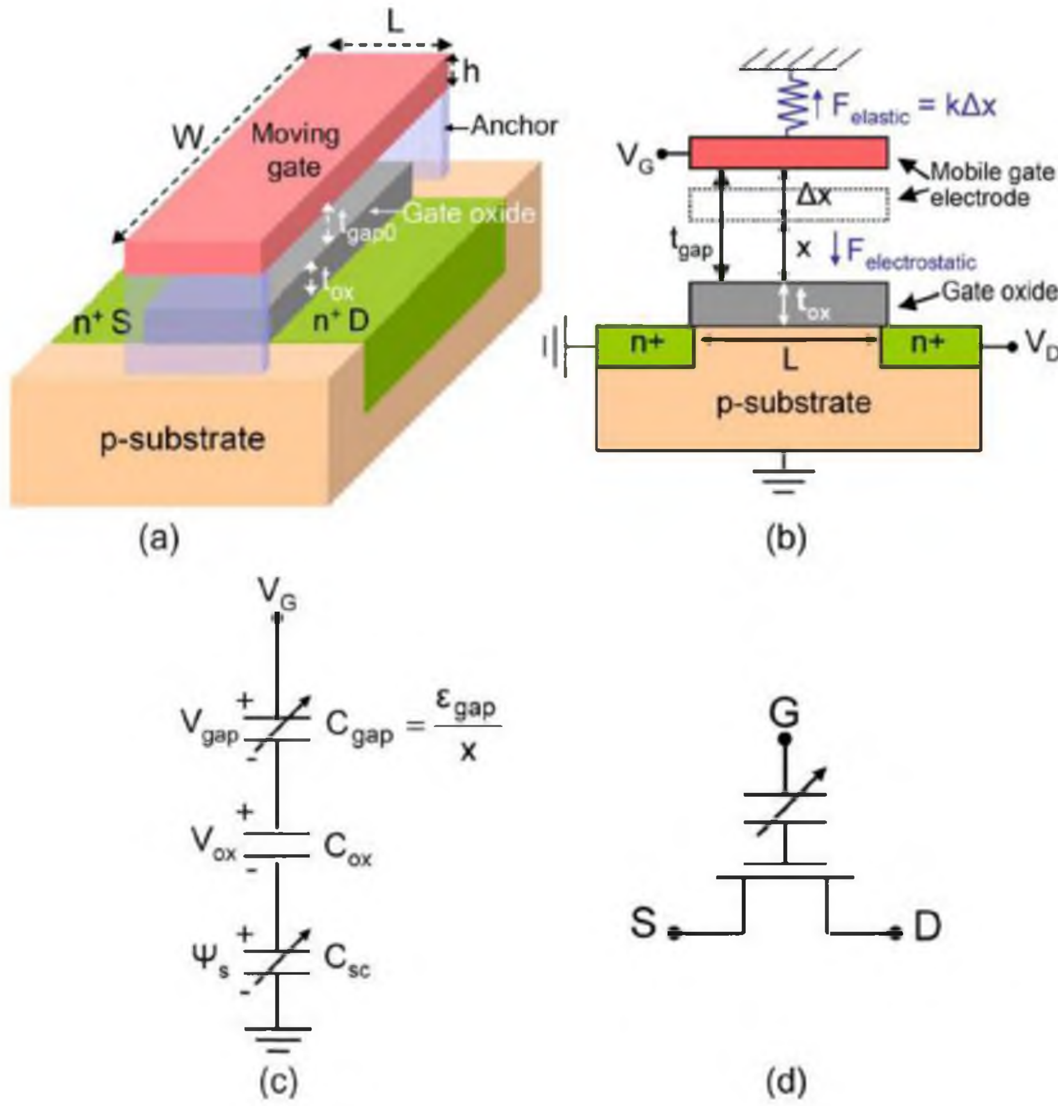

Figure 1.2: N-channel SGFET. (a) 3D structure. (b) CS view parallel to channel length. (c) Equivalent circuit. (d) Circuit symbol [26].

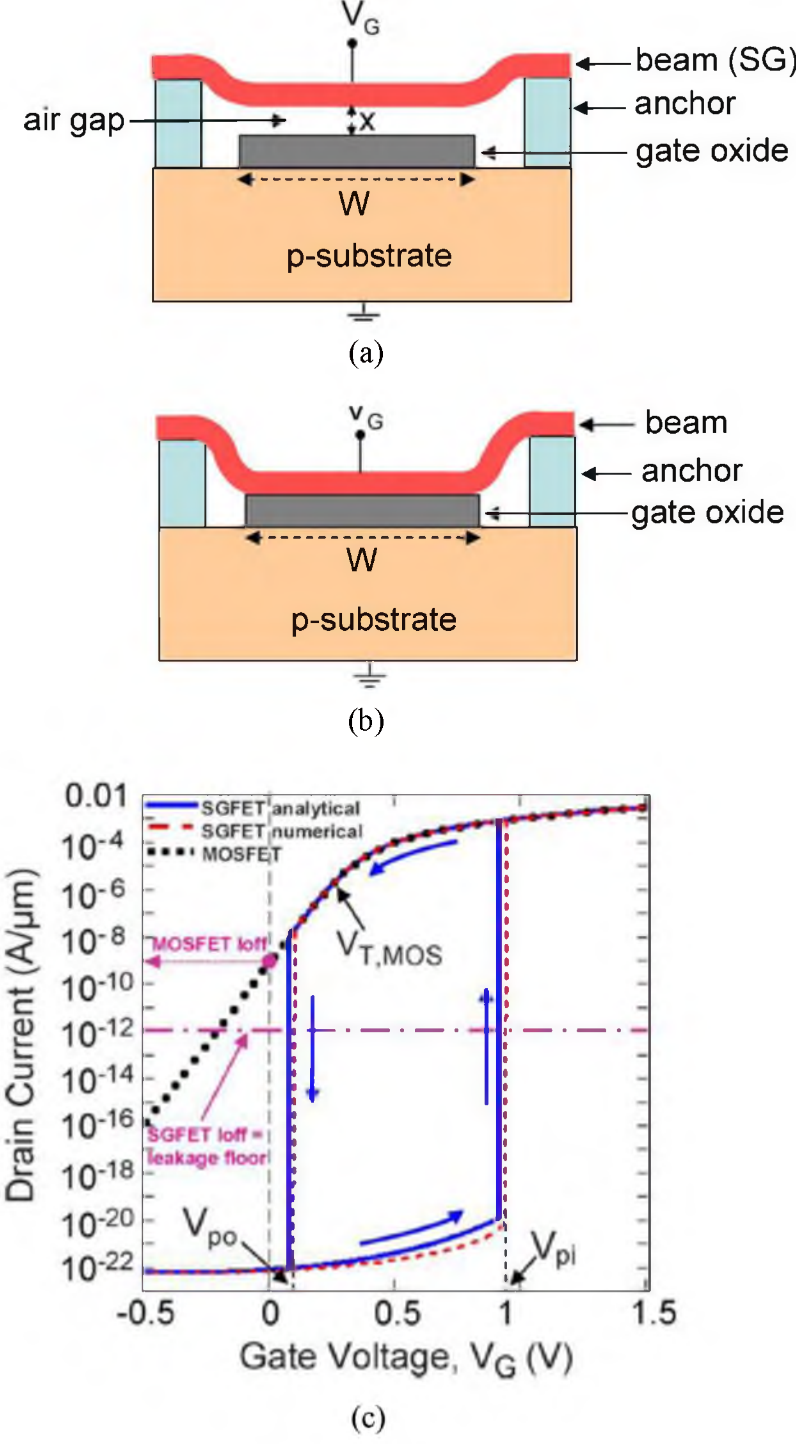

Figure 1.3: CS view of SGFET across device width (a) Gate up ($V_{FB} < V_G < V_{pi}$, $t_{gap0} > x > x_{pi}$). (b) Gate down ($V_G \geq V_{pi}$, $x = 0$). and (c) Analytically and numerically calculated SGFET and MOSFET transfer characteristics. W=500 nm, L=100 nm, h=10 nm, E= 170 GPa (Si), t_{gap0}=10 nm (k=4.35 N/m), t_{ox}=2 nm (SiO_2), V_{FB}=-1.1 V, $N_A=10^{18}$ cm^{-3}, V_D=1.5 V, μ= 250 $cm^2/(V \cdot s)$, Γ=45 $\mu J/m^2$, and D_0=0.2 nm. Leakage floor is assumed equal to 1 pA/μm [26].

Additionally, there has been a report on design considerations for NEMS-based logic gates (CNEM) (Fig. 1.4) [19]. The authors present design predictions for NEMS devices 2-3 orders of magnitude smaller than those generally reported currently. They also present designs for CNEM inverters and CNEM NAND gates utilizing laterally and vertically actuated cantilever beams with 10nm gaps, nanosecond pull in delay, ~0.1fJ switching energy, and 1.5V actuation voltages (Fig. 1.4).

Other work on using MEMS to design logic gates is presented in [27]. The device shown in Fig. 1.5 is capable of implanting either a NAND or NOR function, depending on its electrical interconnects. The device is a 2-layer structure and the operation depends on the see-saw motion of a shuttle electrode on top creating a connection to the fixed electrodes at the bottom. Table 1.1 summarizes its performance metrics and it is seen that for a plate dimension of 250μm x 100μm, it achieves an actuation voltage of 10/0V.

A 4-terminal relay technology was reported in [23] where a single MEMS platform was utilized to mimic solid-state transistors either as a p-channel or n-channel. This was done by exploiting the available terminals to electrically adjust the switching voltage. Fig. 1.6 provides a schematic of the device and its key dimensions. They report performance metrics such as I_{on} > 700μA for V_{DS} = 1V, zero off state leakage, low-voltage switching (< 2V), low switching delay (100ns), and endurance in excess of 10^9 on/off cycles.

Other variants of MEMS logic gate designs reported use piezoelectric materials such as AlN (Fig. 1.7). These complimentary logic switches are reported as having less than 1.5V actuation and by using opposite body biasing, allows the same switch to operate as an n-type and a p-type device [21, 28].

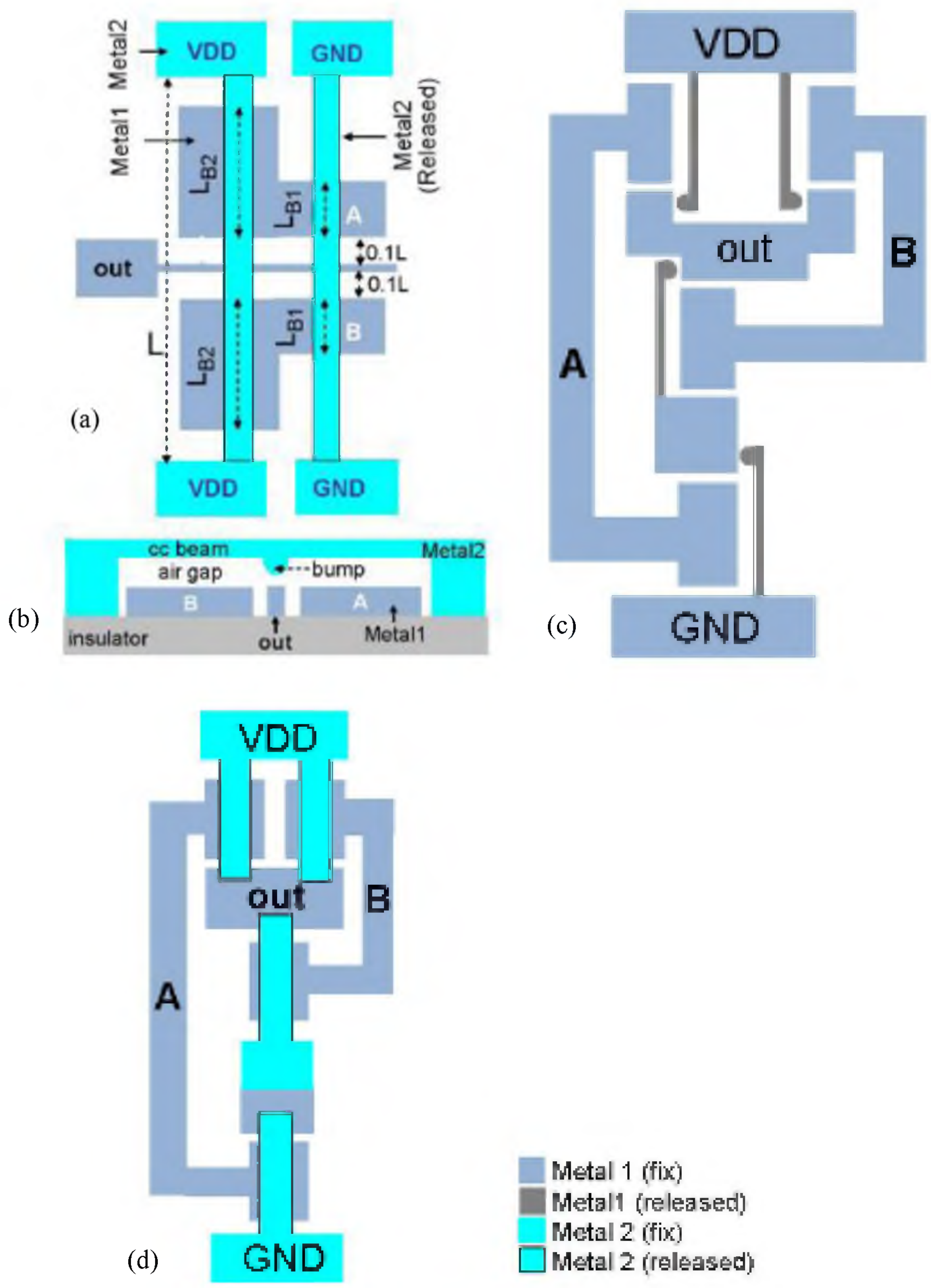

Figure 1.4: CNEM NAND gate (a) "Dual-beam" layout (b) CS view along beams (c) CMOS-equivalent CNEM NAND gate lateral and (d) vertical design [19].

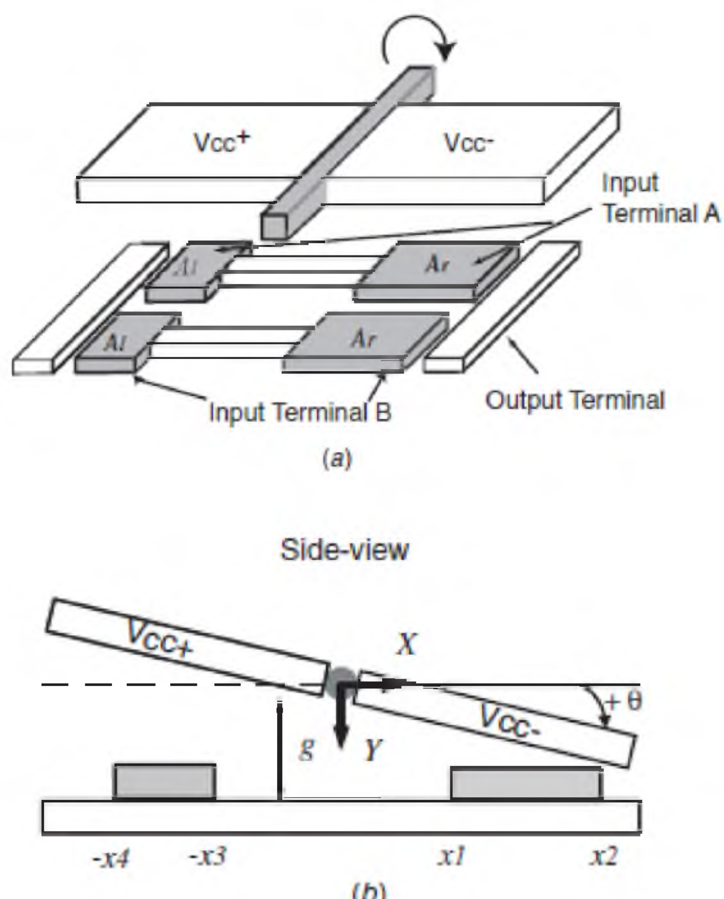

Figure 1.5: Torsional MEM Logic gate (a) 3D view and (b) CS view [27].

Table 1.1: Parameters and performance metrics of device shown in Fig. 1.5 [27].

Plate length	250 µm
Plate width	100 µm
Electrodes locations	50 µm, 100 µm
(x1, x2, x3, x4 shown in figure 3)	85 µm, 100 µm
Actuation voltages Vcc+, Vcc-	10, 0 V
Gap (g)	1 µm
Dimple height	0.5 µm
Max. plate angle	4 × 10-3 rad
Pull-in voltage (1,1) and (0,0) -- 3µm	4.15/6.32 V
Pull-in voltage (1,1) and (0,0) -- 4µm	5.13/7.82 V

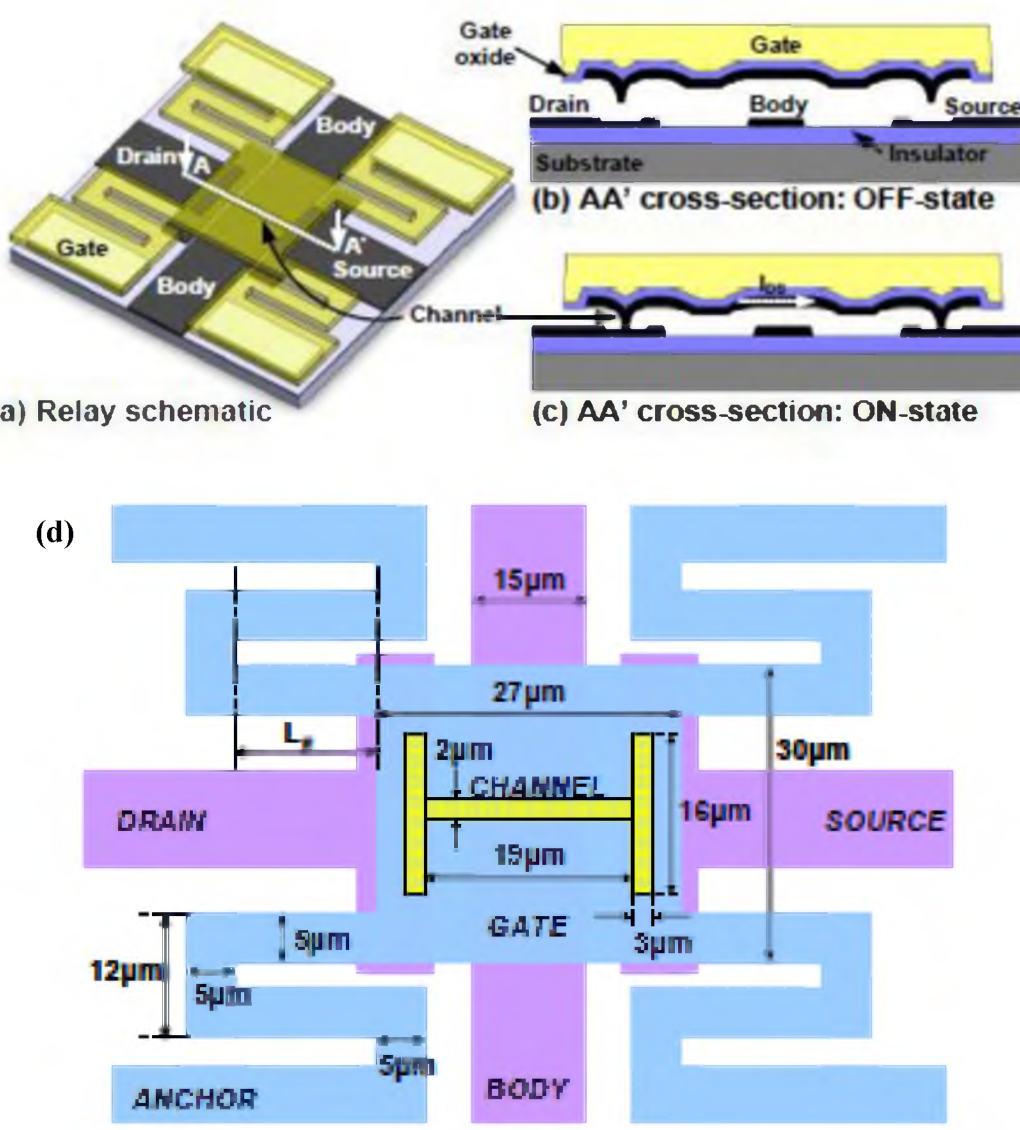

Figure 1.6: 4-terminal MEMS relay structure. (a) isometric view. Cross-section along A-A' in the (b) OFF state and (c) ON state. (d) Key dimensions [23].

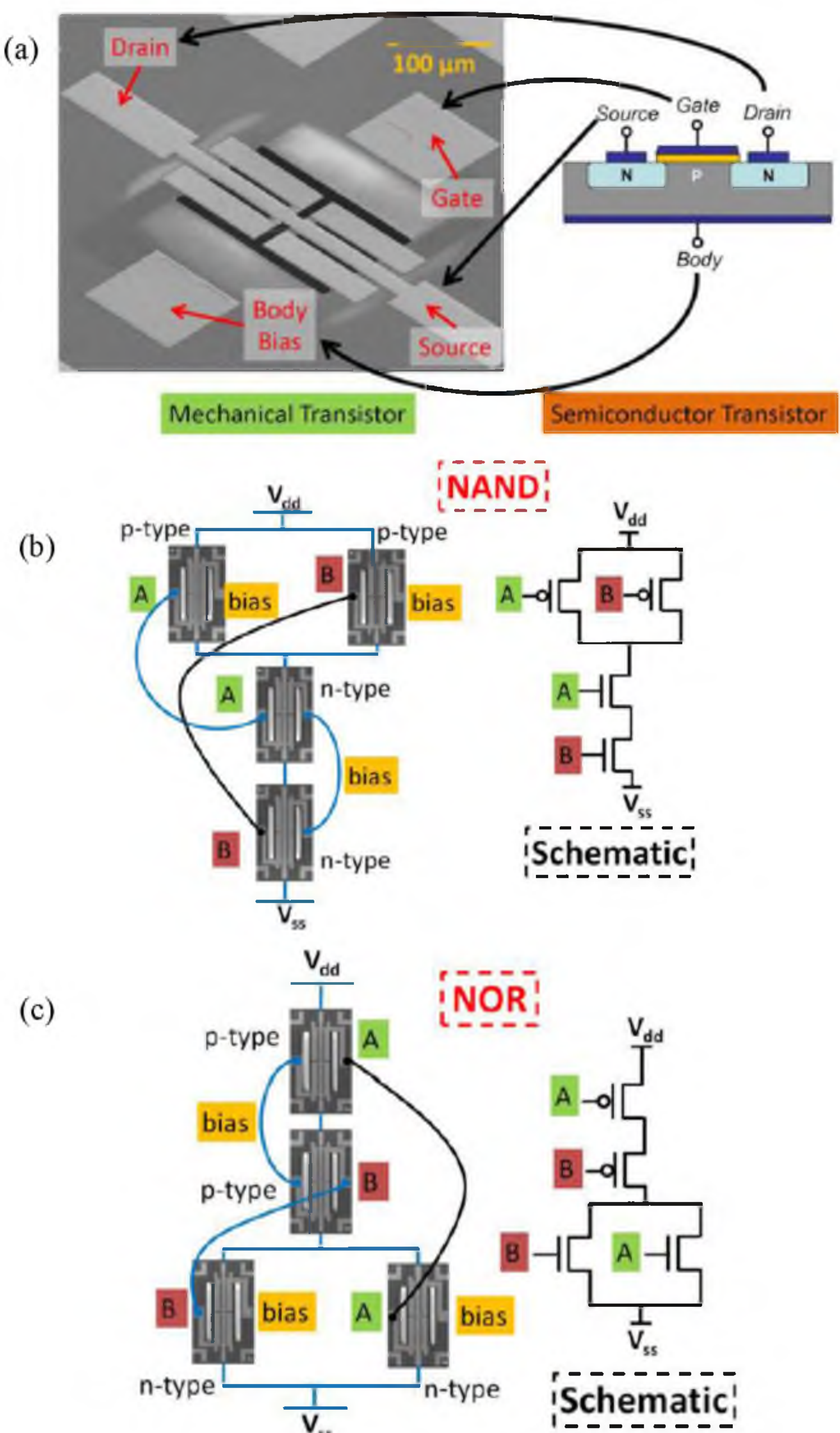

Figure 1.7: AlN-based three-finger dual beam transistor (a) SEM of 250nm thickness variant. (b) Layout of the NAND and (c) NOR complimentary logic operation [21, 28, 29] .

The device is reported to show very small subthreshold slopes (0.8mV/dec), threshold voltage (30mV), operation cycles in excess of 10^9, and contact resistances as high as ~1MΩ. Also, they demonstrate the use of logic elements such as NAND and NOR using a body-biased complimentary structure and using 250nm thick AlN switches [29]. Four complimentary AlN switches were used to form the logic gates having ± 2V swing, and body-bias of <8V.

The switches reported have illustrated their operation as logic gates, some using complimentary P-NEM and N-NEM combinations to operate as NAND or NOR, while others have relied on either piezoelectric actuation or the use of multiple voltage levels to induce complimentary switch functions. However, there are problems with the approaches presented thus far, such as, (1) the fabrication of these devices are complex, (2) several of these devices have a high operating (turn on) voltage, (3) using a combination of MEMS switch and solid-state device, like a MOSFET, will render the device inoperable in harsh environments, and (4) the power consumption of these devices are not really measured at a circuit level whereas this is paramount to evaluate performance when compared to CMOS VLSI.

The work presented in this thesis will present an entirely new paradigm in MEMS logic circuit design – one that does not follow the trend seen in literature that heeds to the CMOS circuit design paradigm by using complimentary switches, and this will overcome all of the shortcomings of the previous work in MEMS-based logic gates.

1.3. Novel Single-Device MEMS Logic Gates

The cross-bridge platform shown in Figs. 1.8 and 1.9 forms the basis for both XOR and AND gates. It illustrates the electrode design for an XOR gate where metal traces overlap at the intersection area of the bridges and the bridges are actuated by electrostatic attraction between the gate electrodes. Other logic gates can be constructed using similar structures but different metallization/contact patterns, as shown in Fig. 1.9 for an "AND" gate. In Fig. 1.10, the diagram has the two bridges, Gate 1, Gate 2, Drain, and Source labeled.

When both gates are low ("00") or when both gates are high ("11"), there is no electrostatic attraction (see XOR in Fig. 1.8). When either one of the gates are high ("10" or "01"), electrostatic attraction causes the drain and source to collapse towards each other and thereby make contact. This is the XOR function (refer to truth table in Table 1.2). A minor modification of the electrode design produces a function corresponding to AND logic (Fig. 1.9). The AND gate requires that both G1 and G2 be high at the same time to enable the top bridge to experience sufficient electrostatic attraction to cause the bridge to collapse towards the bottom bridge and thereby make a S-D connection. This is the ON state. All other conditions translate to OFF state. In the XOR gate, to prevent the drain-source electrodes from causing the attraction between the two bridges, their overlapping area is designed to be 4 times smaller than that of the gate electrodes. The same is true for the AND gate with the ratio being slightly lower. Other gates such as NAND and NOT can also be realized in a similar manner. An XOR gate can be converted to NOT gate by fixing one of its inputs at "1". A NAND gate can be produced by NOT(AND) or by using a different device structure.

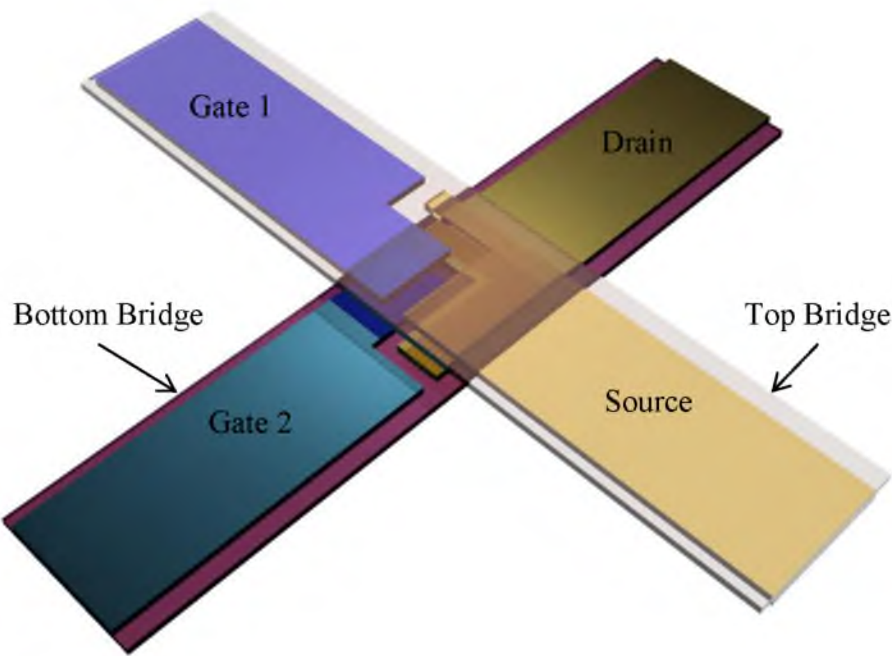

Figure 1.8: Schematic of MEMS single-device XOR gate. The metallization patterns at the top surface of the bottom bridge (Gate 2 and Drain) and at the bottom surface of the top bridge (Gate 1 and Source)

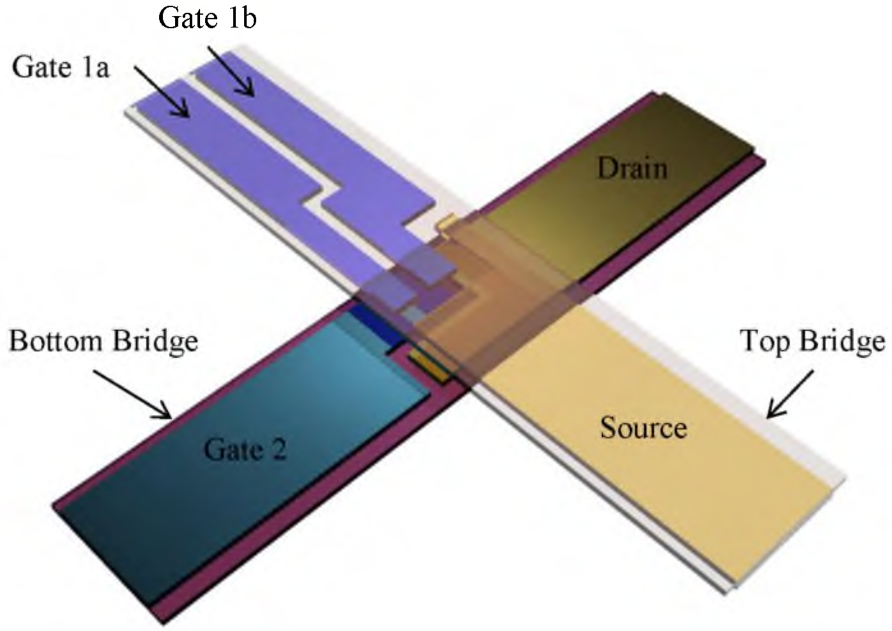

Figure 1.9: Schematic of MEMS single-device AND gate. The metallization patterns at the top surface of the bottom bridge (Gate 2 and Drain) and at the bottom surface of the top bridge (Gate 1a, Gate 1b, and Source).

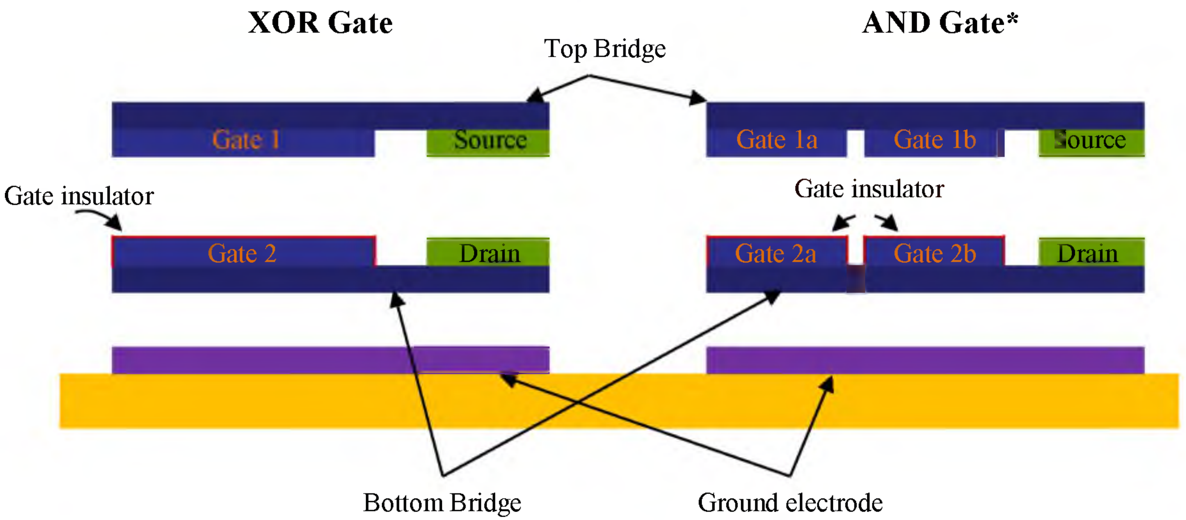

Figure 1.10: Cross-section of XOR and AND gates.

Table 1.2: Truth tables for XOR and AND function (with reference to Fig. 1.10)

XOR Gate Truth Table

Gate 1	Gate 2	S-D
1	1	OFF
1	0	ON
0	1	ON
0	0	OFF

AND Gate Truth Table*

Gate 1a	Gate 1b	S-D
1	1	ON
1	0	OFF
0	1	OFF
0	0	OFF

***Gates 2a and 2b are grounded**

The common implementation of XOR using 8 individual switches as used in CMOS implementation of XOR is shown in Fig. 1.11 [30]. The factor 8 reductions in device count and associated reductions in number of moving parts and areas lead to 8 times better reliability, at least 4 times faster overall logic gate speed, and proportionately higher yields. It must also be noted that multi-input (>2) gates can also be designed using the cross-bridge geometry with two or more metal traces for multiple contact electrodes. A 4-input XOR gate will reduce the device count by ×24.

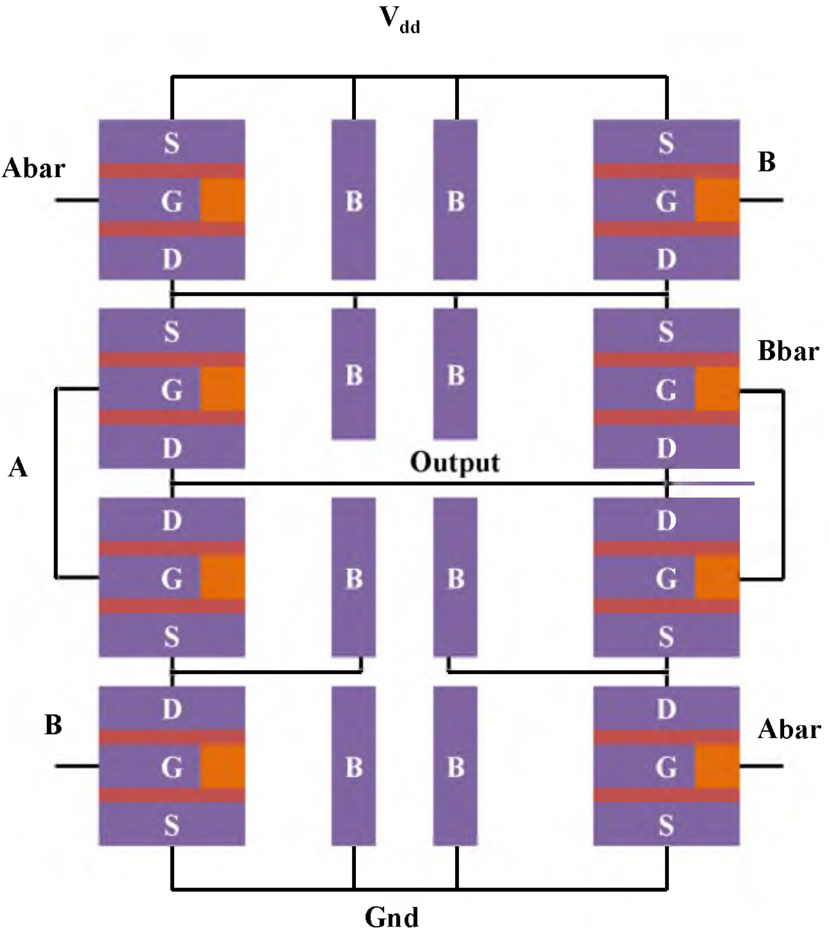

Figure 1.11: XOR implemented using individual CMOS switches require 8 devices each $25\mu m^2$ while our single XOR device requires only $25\mu m^2$ area.

1.4. Summary

This chapter highlights the increasing need for developing new technologies that are not adversely affected by scaling factors affecting CMOS. One of the biggest drawbacks from scaling down CMOS is the rapidly increasing power dissipation, resulting in dramatically reduced efficiencies. Some of the potential successors that promise to overcome these drawbacks have been identified as spintronics, carbon nanotubes, and quantum dots. However, each of these has its own set of limitations and is far from a mature technology. It can be argued that, due to its inherent zero-leakage current at OFF-state and other favorable characteristics, MEMS switches are a viable alternative, or a companion for hybrid MEMS-CMOS devices that reap the best benefits from both technologies. This chapter also compares the state of the art in MEMS switches being used in a combinatorial fashion as logic gates and presents their setbacks. Thereafter, a novel single-device MEMS logic gate is presented that reaps all the benefits of a traditional MEMS switch and is also designed such that each operation cycle produces a functional logic (such as AND or XOR). As a result, this new technology overcomes the drawbacks for a CNEMS paradigm followed by others in the field to date. Other significant contributions, such as contact resistance evolution and harsh environment performance (high temperature and high ionizing radiation), are also outlined here.

The proceeding sections of this thesis is divided into seven chapters. The first chapter discusses the motivation, background, state-of-the-art MEMS, and significant contributions of this work to the field. Chapter 2 deals with theoretical modeling (mechanical, electrical, and reliability), along with simulation and calculations relevant to

the device described in this thesis. Chapter 3 covers an in-depth reliability and contact resistance evolution investigation on eight different metals and one nonmetal generally used as contact electrodes in MEMS. Following that, Chapter 4 provides details on the fabrication procedure of the single-device MEMS logic gates. Chapter 5 elaborates on the testing schemes utilized to characterize this device. Chapter 6 discusses the future work in this area, and finally, Chapter 7 completes this dissertation with a conclusion section.

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CHAPTER 2

DESIGN CONSIDERATIONS

2.1. Theoretical Aspects in Device Design

In most cases, MEMS devices, e.g., electrostatic switches, harness the power of multiple energy domains, such as, electro-mechanics, optical electricity, thermoelectricity, and electromagnetism, into a single device. As such, their operation is highly nonlinear and requires complex analysis. Due to its virtually zero power consumption, small electrode size requirements, thin layers used, relatively short switching time, 100s of μN achievable contact forces, the possibility of biasing using high-resistance bias lines, ease of integration with existing fabrication techniques, and the overall simplistic design, the electrostatic mode of operation is the most preferred and commonly employed technique in MEMS-based sensing and actuation modules [1, 2]. Nevertheless, due to the interaction between electrostatic and structural domains in electro-mechanical systems, it results in compound influences by multiple physical parameters ranging from thin film stresses to electrical fields, resulting in a highly nonlinear and unstable system that is prone to "pull-in" phenomena. The consequences of this are catastrophic failures by way of fatigue, charge migration, dielectric charging, stiction, micro-welding, wear, surface pitting, and/or asperity generation – amongst many others that evolve as a function of operation cycles. In order to mitigate such detrimental

processes and successfully design a structure that reaps benefit out of a potentially unstable system, a thorough understanding of the concepts behind the failure modes is necessary. Using a mechanical lumped model and an electrical circuit equivalent, this chapter covers the modeling mechanisms of the quasi-static pull-in voltage, transient behavior during a pulsed signal, and reliability (electrical contact and others) of MEMS switches, all of which are fundamentally important to understanding the operation of a MEMS switch. Additionally, numerical calculations on optimum switch dimensions and corresponding COMSOL simulation results are discussed.

2.1.1. Mechanical Lumped Model: Pull-in Voltage

The origins of the electrostatic charge build up culminating in "snap-down" in MEMS devices are rather well known. Considering a typical MEMS fixed-fixed bridge connected to a substrate via anchors, as shown in Fig. 2.1, whenever there is an electrical potential difference between two surfaces separated by a dielectric (bridge, substrate, and air gap, in this case), electric charge builds up, resulting in an electrostatic attractive force. This induces bending of the beam towards the substrate (downward), while the structural (elastic) properties of the beam continually try to restore the beam to its original disposition (upward force). In essence, the combination of the two results in an equilibrium state.

However, an increase in the applied voltage results in an increased deformation on the beam. Consequently, as the surface electrostatic charges redistribute, so does the electric field, resulting in a stronger attractive force and therefore more deflection of the beam until a new equilibrium is achieved by the counter-action of the elastic restoring

force. The illustration in Fig. 2.2 represents a physical model of that shown in Fig. 2.1, which consists of a spring-loaded parallel plate capacitor. The figure also includes a simplistic electrical circuit model of the MEMS capacitor.

The parallel plate capacitance is given by equation (1):

$$C = \frac{\varepsilon_0 A}{g}[\alpha] \quad (1)$$

where ε_0 is the dielectric permittivity, A is the area of the parallel plate capacitor, g is the gap between the plates, and α is the fringing field factor.

The energy stored in the MEMS capacitor is a function of an electrical variable (charge) and a mechanical variable (displacement or gap). As a result, the electrical equivalent model shown in Fig. 2.2 is a two-port device. This two-port device is a single capacitor with a single stored energy given by equation (2):

$$W(Q,g) = \frac{Q^2 g}{2\varepsilon A} \quad (2)$$

Consequently, the effort variables are partial derivatives of W, respectively

$$F = \frac{\partial W(Q,g)}{\partial g}\Big|_Q = \frac{Q^2}{2\varepsilon A} \quad (3)$$

$$V = \frac{\partial W(Q,g)}{\partial Q}\Big|_g = \frac{g}{\varepsilon A} \quad (4)$$

where, F is the spring restoring force and V is the applied voltage.

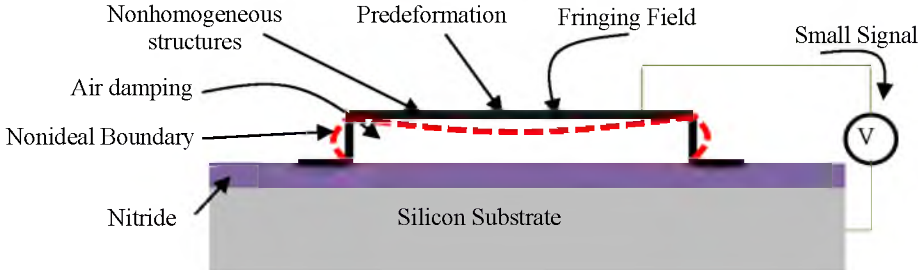


Figure 2.1: Schematic representation of nonlinear electro-mechanical system

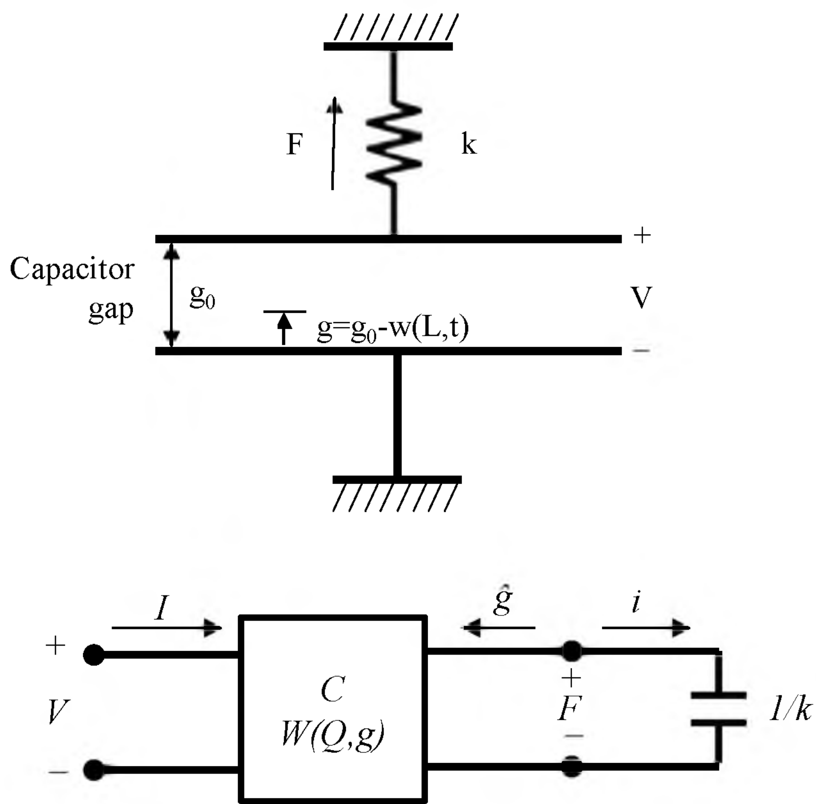


Figure 2.2: A lumped parameter model using a spring-loaded parallel plate capacitor (left) [3] and an electrical circuit equivalent (right). F is the spring restoring force, g0 the nominal gap height, g the gap as a function of voltage. The energy stored in the electrical model, $W(Q,g) = \frac{Q^2 g}{2\varepsilon A}$, where Q is the charge stored and g is the gap height.

Now, the electrostatic force, F_E, that is generated on the plates is given by equation (5):

$$F_E = \frac{1}{2}V^2\frac{dC(g)}{dg} = -\frac{1}{2}\frac{\varepsilon_0 A V^2}{g^2} \tag{5}$$

Equating this to the spring restoring force, (F_E=F), and rearranging the variables results in a rudimentary relationship between V and g given by equation (6):

$$V = \sqrt{\frac{2k}{\varepsilon_0 A}g^2(g_0 - g)} \tag{6}$$

Using the relation F=kg (hookes law), Fig. 2.3 illustrates a graph that summarizes the behavior of an electromechanical system coupling electrostatic forces and spring forces versus the deformation of a MEMS beam.

The graph is plotted with the abscissa labeled as the ratio of the beam deformation (g_0-g) to the initial gap (g_0) between the beam and the substrate, while the ordinate axis illustrates the force. It is clear from the graph that the mechanical domain is a linear function of the deformation of the beam, while the electrical domain is proportional to the square of the same parameter. When a small driving voltage is applied, the electrostatic forces and the elastic forces are sufficiently equal to maintain the system at a stable equilibrium point. However, with further increment in the drive voltage and consequent redistribution of charges and electric fields, the electrostatic attractive force is sufficiently larger such that the spring restoring forces can no longer contend with the former, resulting in instability and therefore radical collapse of the beam.

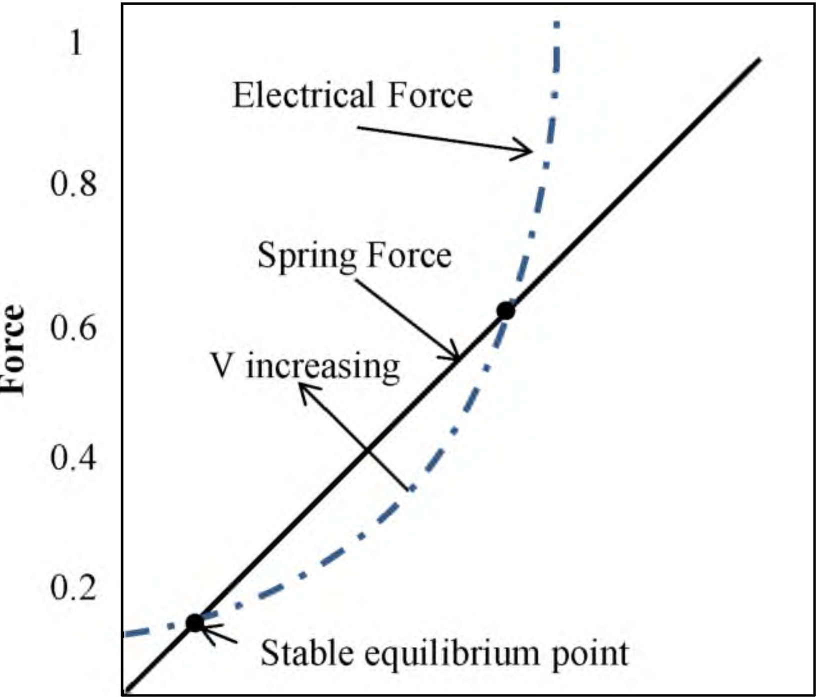


Figure 2.3: Electrostatic force and elastic restoring force characteristics on a parallel plate electrostatic actuator [2]

This is known as "pull-in" voltage and is based on a positive feedback cycle of capacitive charge buildup between the parallel plates of the MEMS "capacitor". The pull-in occurs at one third of the nominal gap height and a crude form is given by equation (7):

$$V_{PI} = V\left(\frac{2g_0}{3}\right) = \sqrt{\frac{8k}{27\varepsilon_0 A}g_0^3} \tag{7}$$

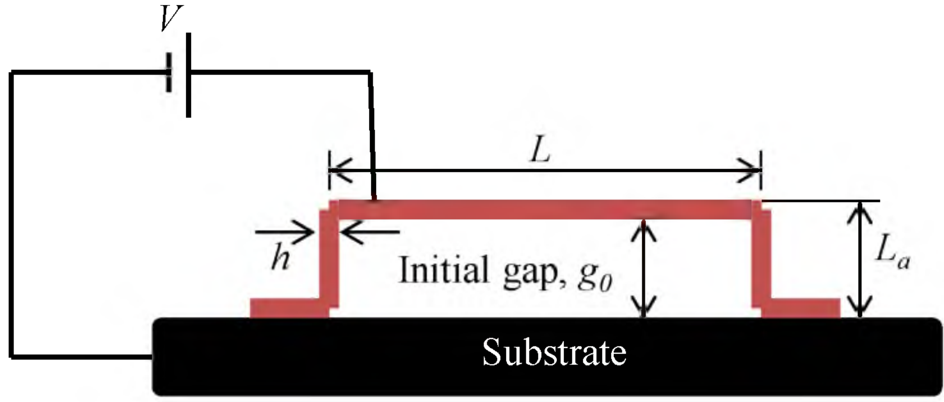
The development of this lumped model began from 1994 when Senturia et al. began publishing their research on the electro-mechanics of a MEMS device based on the model described previously (Fig. 2.2) [4] in order to mathematically evaluate the

fundamental functional forms of the pull-in voltage, geometric dimensions, and material parameters. Over the course of the first decade thereafter, much work was focused on fabrication and simulation of electrostatically actuated micro-beams and their characterization [5-8]. Various effects, including fringing capacitance, efficiency of plate-like phenomenon, and different boundaries, were also accommodated as the models evolved. The difference between the simulated characteristics (spring constant, pull-in voltage, etc.) and the fabricated device was reduced from 18% in 2002 to about 4% in 2005 by virtue of improved modeling [9]. During 2004-2008, Krylov et al. published their research findings on pull-in behavior of microstructures [10-13]. They focused on the transient nonlinear dynamics that electrostatics impose on microbeams and developed a model that considered effects around distributed nonlinear electrostatic forces, nonlinear squeezed film damping, and rotational inertia of a mass on the beam.

Furthermore, from 2006 to 2009, Hu et al. developed on these models by incorporating inherent (initial) stresses, fringing capacitance effects, and elastic boundaries [14-18]. The conceptualization of treating a beam with elastic boundaries as having torsional springs at both ends is illustrated in Fig. 2.4. The beam length is denoted by L, anchor height L_a, width b, thickness h, and initial gap g_0.

From their derivations, the equation representing equivalent torsional spring constant k can be expressed as [15]:

$$k = \frac{M}{\theta} = \frac{4E(2I_a^2 L + I \cdot I_a L_a)}{2I_a L_a L + I_a L_a^2} \tag{8}$$



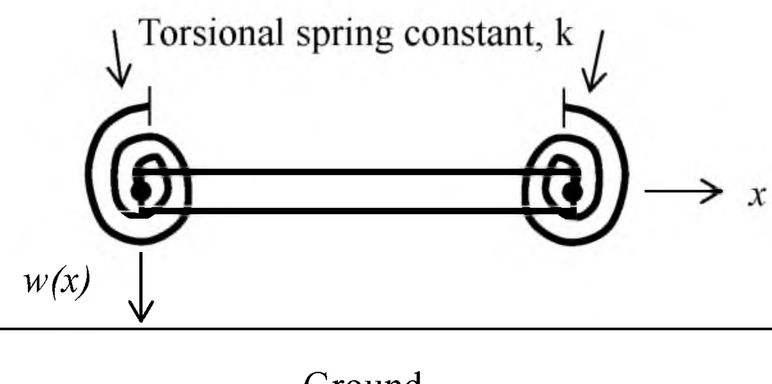


Figure 2.4: Physical and analytical model of a micro-bridge treated as having a torsional spring at both ends [15].

where I is the moment of inertia, subscript a denotes the anchor, and E the Young's modulus. Fig. 2.5 illustrates a state where a beam is subjected to load, P_0, applied uniformly across its surface.

The reactive bending moment M, and the rotation angle θ, for the uniform load of Fig. 2.5 can be derived as follows:

$$M = \frac{P_0 L^2}{12\left(1+0.5\frac{I}{I_a}\frac{L_a}{L}\right)} \tag{9}$$

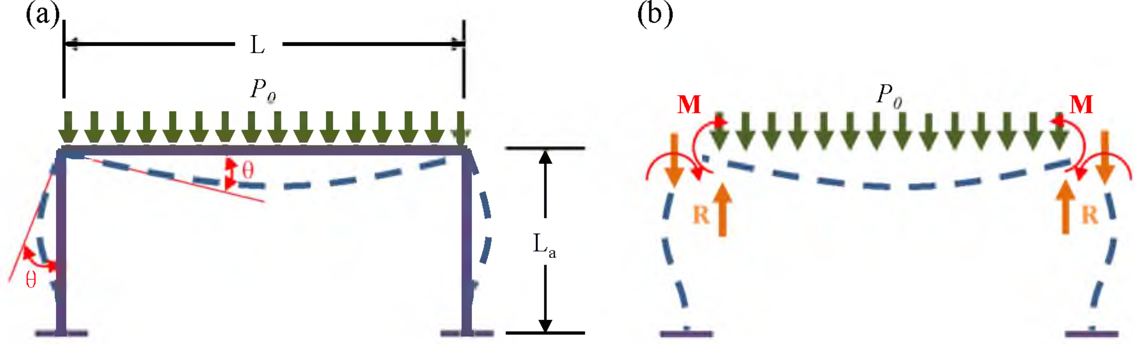


Figure 2.5: Schematic illustrating loading effects: (a) uniform load P_0 over a beam and (b) its free body diagram [15].

$$\theta = \frac{P_0 L^2}{24E\left(2\frac{I_a}{L_a}+\frac{I}{L}\right)} \tag{10}$$

The pull-in voltage, V_{PI}, of such a beam was calculated, using Euler's beam model and the minimum energy method, to be [15]:

$$V_{PI}^2 = \frac{\sigma_0 \int_0^L 2bh(\emptyset')^2 dx + E\int_0^L 2I(\emptyset'')^2 dx + (\frac{8EI_a}{L_a})(\emptyset')_{x=L}^2}{\varepsilon(c_1 + 2c_2\eta_{PI} + 3c_3\eta_{PI}^2)} \tag{11}$$

where the initial stress is denoted by σ_0 and the first natural mode of the beam having torsional springs at both ends is represented by ϕ [19].

$$\phi(x) = \left[sin\left(\frac{\beta x}{L}\right) - \sinh\left(\frac{\beta x}{L}\right)\right] + \gamma\left[cos\left(\frac{\beta x}{L}\right) - \cosh\left(\frac{\beta x}{L}\right) - \frac{\beta L_a}{2L}\sinh\left(\frac{\beta x}{L}\right)\right] \tag{12}$$

$$\gamma = \frac{sinh\beta - sin\beta}{cos\beta - cosh\beta - \frac{\beta L_a}{2L} sinh\beta} \tag{13}$$

Also, β, must satisfy the following equation:

$$\left(\frac{kL}{EI}\right)^2 + \frac{kL}{EI}\frac{2\beta(sin\beta cosh\beta - cos\beta sinh\beta)}{1 - cos\beta cosh\beta} + \frac{2\beta^2 sin\beta sinh\beta}{1 - cos\beta cosh\beta} = 0 \qquad (14)$$

From the three terms in equation (11), we can deduce an obvious physical meaning; the first term indicates that the pull-in voltage is dependent on initial residual stress, the second term illustrates dependency on flexibility, and the third denotes dependence on elastic boundary conditions.

2.1.2. Electrical Circuit Equivalent Model

The MEMS logic gates can be represented using electrical circuit components such as resistors and capacitors corresponding to those that are contributed by the gates and drain/source contacts as shown in Figs. 2.6 and 2.7 in the OFF and ON states.

The XOR gate equivalent circuit in the OFF state shown in Fig. 2.6(a) has G1 and G2 representing gates 1 and 2. D and S correspond to the Drain and Source terminals. R_{G1} and R_{G2} and R_D and R_S correspond to the fixed resistances associated with the gates and Drain and Source, respectively. The fixed capacitances C_{G1S} and C_{G2S} are associated with capacitance between Gate 1 and Source, while the latter is that between Gate 2 and Drain. The variable capacitance C_{DS} and resistance R_{DS} is that between the Drain and Source and represents the changing capacitance (and resistance) prior to snap-down. R_{DS} is derived from the reciprocal summation of the tunneling current, calculated using the Fowler-Nordheim tunneling current expression.

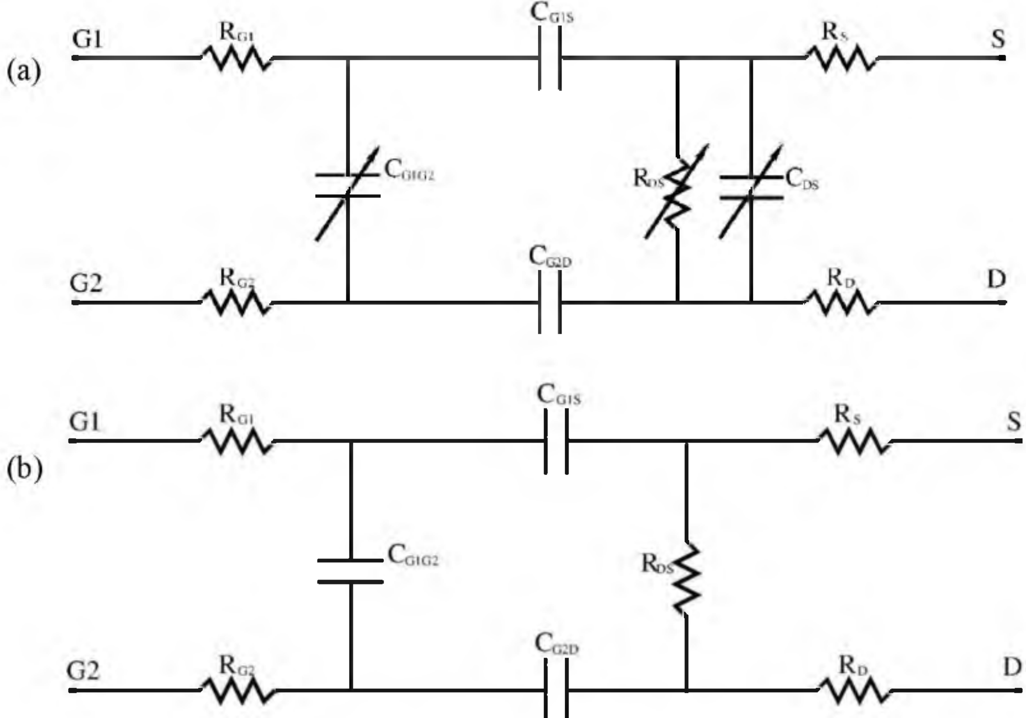


Figure 2.6: Electrical circuit model of XOR gate in the (a) ON and (b) OFF state

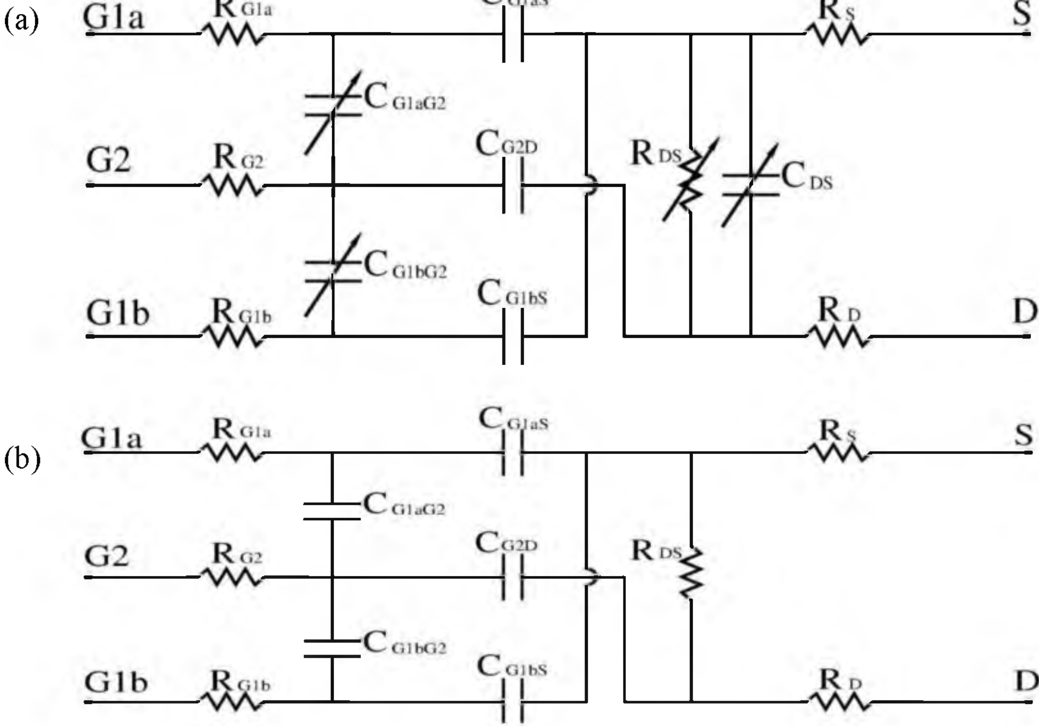


Figure 2.7: Electrical circuit model of AND gate in the (a) ON and (b) OFF state.

The surface current and the switching current are obtained from the experimental measurements. The variable capacitances C_{G1G2} and C_{DS} are calculated by the summation of the capacitances between corresponding bridges elements using the parallel plate model where the gap distances between each segment is calculated from the mechanical lumped model.

In the ON state (illustrated in Fig. 2.6(b)), the circuit model changes to account for the fact that there is no longer a separation between D-S – C_{DS} is eliminated. The gate capacitance C_{G1G2} is that between G1 and G2 separated by a thin insulator at snap-down. Furthermore, the variable resistance R_{DS} is now a fixed resistor representing the contact resistance between the electrodes and can be calculated either by the Sharvin or the Maxwell model (as described in the following section).

Fig 2.7(a) illustrates the electrical circuit model of the split gate AND device. Gate 1 is divided into G1a and G1b while gate 2 (G2) and Drain (D) and Source (S) are similar to the XOR gate. The fixed contact resistances associated with G1a, G1b, G2, D, and S are represented by R_{G1a}, R_{G1b}, R_{G2}, R_D, and R_S. The fixed capacitances between G1a and S, G1b and S, G2 and D are represented by C_{G1aS}, C_{G1bS}, and C_{G2D}. Furthermore, the variable resistance and capacitance between D and S is indicated by R_{DS} and C_{DS}.

Additionally, the variable capacitance between G1a, G1b, and G2 are indicated by C_{G1aG2} and C_{G1bG2}. In Fig 2.7(b), during the ON state, the circuit is modified to account for the fixed contact resistance R_{DS} and thereby, the absence of capacitance between the D-S (as they are now shorted). Additionally, capacitances C_{G1aG2} and C_{G1bG2} are now fixed with their insulators acting as the dielectric contributing to the capacitance. The fixed contact resistance at the D-S electrodes after snap-down is given by R_{DS}. The

capacitances and resistances here can be determined in a similar fashion to that of the XOR gate.

2.1.3. Modeling a Digital Pulse Across a MEMS Switch

A traditional switch (or relay) can be considered to be a 1-terminal device driven between its ON and OFF states by an actuating contact. In a similar fashion, a general MEMS switch can be also be modeled as a 1-terminal relay, as illustrated in Fig. 2.8.

The physical model above can be analyzed in an electrical equivalent model, as given in Fig. 2.9. The model consists of a resistor that is equivalent to the resistance imposed upon the flowing current when the switch is in the ON state and a capacitor that impedes flow of direct current between the electrodes when the switch is in the OFF state. The value of the resistor depends on material properties (resistivity) and surface area of contact, while the capacitance is related to the gap height, its dielectric properties, and the overlapping surface area of the electrodes.

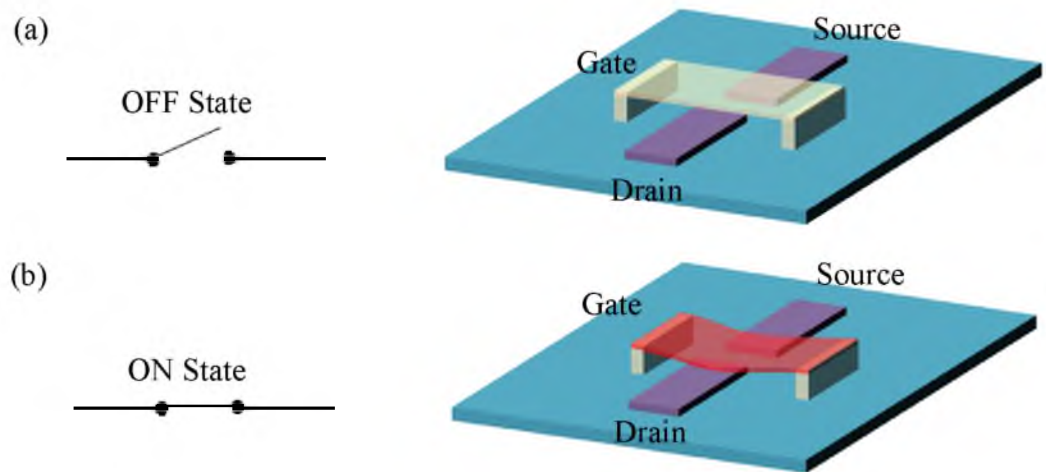
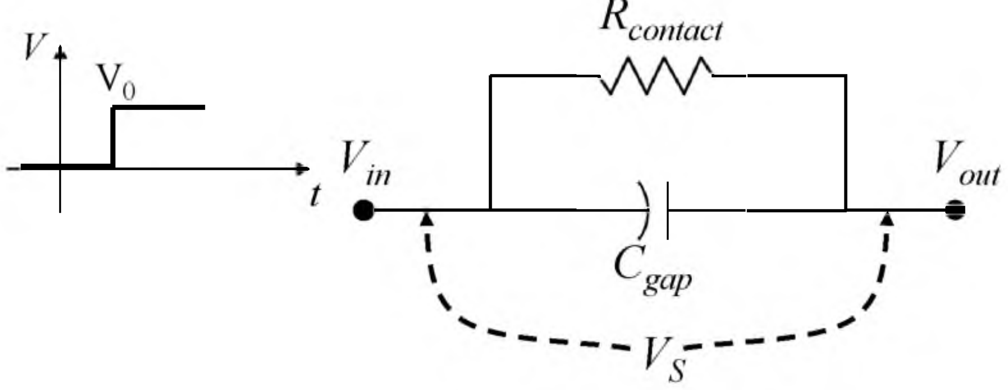
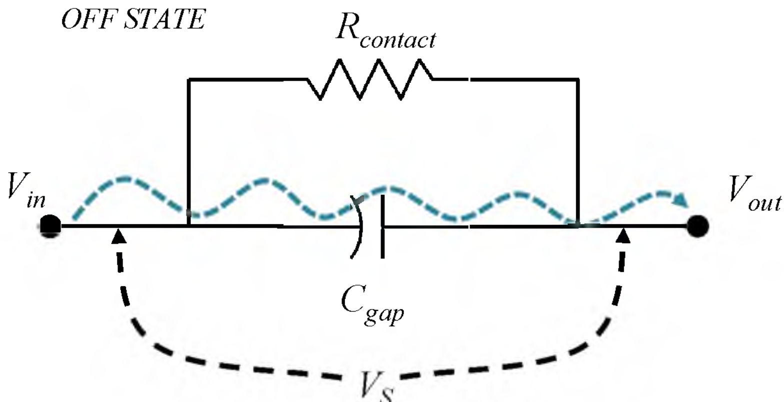


Figure 2.8: MEMS relay model (a) OFF state, (b) ON state





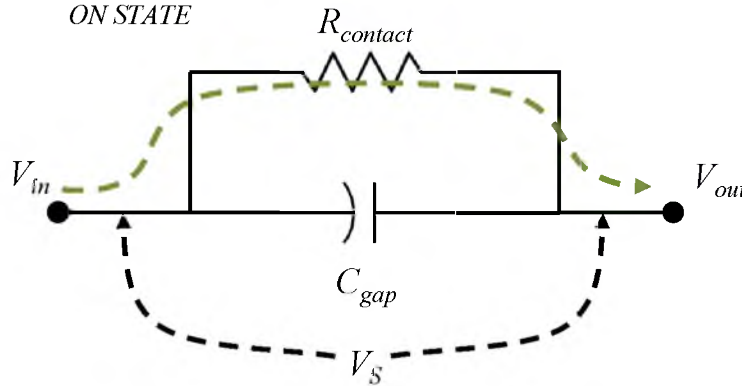


Figure 2.9: Electrical model of a simple MEMS relay

When a single digital pulse is applied to a MEMS switch, there are three associated voltages that are of interest: input voltage V_{in}, voltage across the switch V_s, and an output voltage V_{out}.

$$V_{in} = V_S + V_{out} \tag{15}$$

$$V_S = V_{in} - V_{out} \tag{16}$$

A MEMS switch can be considered to be a fusion between a traditional mechanical relay, and a previously charged fixed plate capacitor. The transient behavior of a MEMS switch in this case can be understood by examining the case of a relay switch and a (precharged) fixed capacitor, separately. The transient input voltage (when a digital pulse is applied) is shown in Fig. 2.10(a). For the case of a relay, the switch is considered to be a purely resistive device upon closing (Fig. 2.10(b)). The delay associated with the voltage stabilizing at V_S is the time constant (τ_R) that is due to the inertia of the mechanical bridge attributable to its mass. The dynamic equation of motion governing this is given in equation (17).

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = f_{ext} \tag{17}$$

where x is the bridge displacement, m is the mass, b is the mechanical damping coefficient, k is its spring constant, and f_{ext} is the external (electrostatic) force applied to it.

In the purely capacitive case, the charge on the capacitor results in a pre-existing voltage across its leads (Fig. 2.10(c)). The analogy here is that when a voltage is imposed upon a MEMS switch, electric charges gradually build up across the two plates but are not sufficient to create a strong electrostatic field that will result in snap-down. When the voltage is further increased (application of a pulse) such that there is a sufficiently large increase in electric field between the plates generating larger forces to just overcome mechanical restoring forces and instigate a closed loop feedback between increasing capacitance and increasing electric field, it results in snap-down. The voltage across the capacitor during charging and discharging is given by equations (18) and (19), respectively.

$$V_C(t) = V_0 + V_{in}(1 - e^{-t/RC}) \tag{18}$$

$$V_C(t) = V_0 + V_{in}e^{-t/RC} \tag{19}$$

The delay associated with stabilizing at V_0 is the capacitive time constant, τ_C, related to the R*C value.

Fig. 2.10(d) shows the MEMS transient behavior that combines both capacitive and resistive features. Both time constants are illustrated together and the super-posed effects are what are visible in a typical MEMS relay. It is worth noting that only when $V_S \geq V_{th}$, where V_{th} is a threshold voltage (a.k.a V_{PI}), will the transient behavior swing away from capacitive (open switch) to resistive (closed switch).

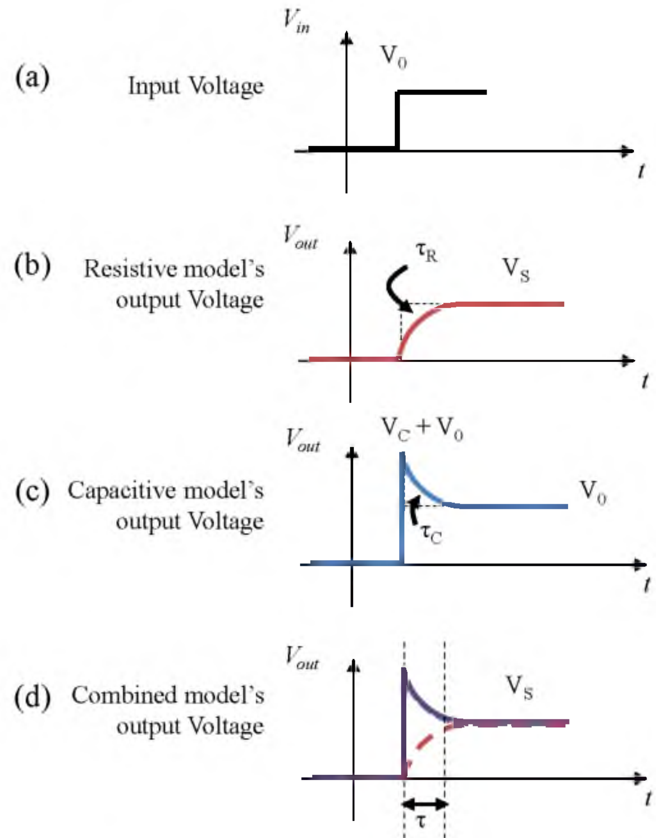


Figure 2.10: Wave forms depicting transient behavior through MEMS switch

Now, in equation (17), f_{ext} is generated by electrostatic forces resulting from the applied voltage. At the moment the pulse is applied, the capacitor (i.e., MEMS switch in OFF state) is shorted out briefly and the voltage across the device is 0V. This results in f_{ext} =0. With time, however, charges build up, on the capacitance and the voltage across the device builds up, which consequently builds up the electrostatic attractive force between the two plates, as given in eq. (20).

$$f_{ext} = \frac{1}{2} V^2 \frac{dC(g)}{dg} \tag{20}$$

When the voltage-induced electrostatic force is sufficiently large, it results in snap-down, and the capacitance now drops to zero again, and so does the voltage across the switch (although the voltage now is, strictly speaking, not zero – it is proportional to the contact resistance value).

It is seen that at the two instances when voltage across the switch is 0V, eq. (17) turns into a homogeneous second-order ordinary differential equation, with the right-hand term equal to zero (eq. (21)). The solutions (or roots) for this equation are given by r_1 and r_2 below (eq. (22)):

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = 0 \tag{21}$$

$$r_1 = -\frac{b}{2m} + \sqrt{(b + 2\sqrt{m})(b - 2\sqrt{m})}$$

$$r_2 = -\frac{b}{2m} - \sqrt{(b + 2\sqrt{m})(b - 2\sqrt{m})} \tag{22}$$

It is understood that both roots are real as there are two points on the loci of 'x' at which the ODE equates to 0. The resulting solution can be written as

$$x = C_1 e^{r_1 t} + C_1 e^{r_1 t} \quad (23$$

Or,
$$x = C_1 e^{\left\{-\frac{b}{2m} + \sqrt{(b+2\sqrt{m})(b-2\sqrt{m})}\right\}t} + C_1 e^{\left\{-\frac{b}{2m} - \sqrt{(b+2\sqrt{m})(b-2\sqrt{m})}\right\}t} \tag{24}$$

Finally, values for the constants C_1 and C_2 can be obtained by substituting $x=g_0$ and $x=0$ corresponding to the positions of the switch during which $f_{ext}=0$.

2.1.4. Reliability

MEMS and NEMS switches require reliable "hot" contact materials for $>10^{12}$ switching cycles without changing contact resistance, stiction, and micro-welding. It was seen from experimental extrapolations that if a microprocessor is built using similar MEMS switches that lasts $\sim 10^{15}$ operational cycles, it translates to 10 years of operating lifetime at 100MHz (and 1% switching probability) [20]. There are many NEMS-based switches reported in the literature that report operational lifetimes ranging from 10^8 - 10^{10} cycles [21-27]. However, our understanding of the contact resistance and how it is affected by many DC and RF switching cycles is still very limited in spite of several attempts made by groups in universities and industry to investigate the performance of contact materials for applications in MEMS switches [28-33]. These past studies suggest that ideal contact materials for MEMS applications should have high melting points, high Young's modulus, low contact resistance, low diffusivity in each other, dissimilarity between the two contact materials (i.e., they should have different crystal structure, conductivity, etc.), and in some cases, the ability to "replenish" or "heal" itself over time.

Various models have been devised to study the switching and reliability issues greatly associated with MEMS. The most common failure mechanisms include mechanical fracture, stiction, wear, delamination, vibration and shocks, electrostatic discharge and dielectric charging, radiation effects, temperature, humidity, and particulates. The device discussed in this thesis is a fixed-fixed multilayered bridge structure which is prone to several of the above modes of failure that are design-limited such as hot-contact switching degradation (stiction, wear, ESD, dielectric charging) and fatigue at hinges (mechanical failure, delamination, inherent stresses).

2.1.4.1. Contact Resistance Failure

Fig. 2.11 illustrates a schematic that emphasizes the region that makes electrical contact between two electrodes (fixed-fixed bridges, in this case). For simplicity, if it is assumed that the bottom bridge is completely flat, while the top bridge possesses finite asperities that contribute to the actual electrical contact, we can further qualify that only few tens of such asperities will make intimate contact with the bottom bridge, with each asperity having a tip radii of 50-200nm. As soon as electrostatic forces are sufficiently high to initiate snap-down, these asperities on the surface of the bridges contact and begin deformation. This distorts the asperities into circular contact spots.

The number of these contact spots can be determined by the well-known "Asperity-based model" introduced by Greenwood and Williamson [34] and developed by Chang et al. [35].

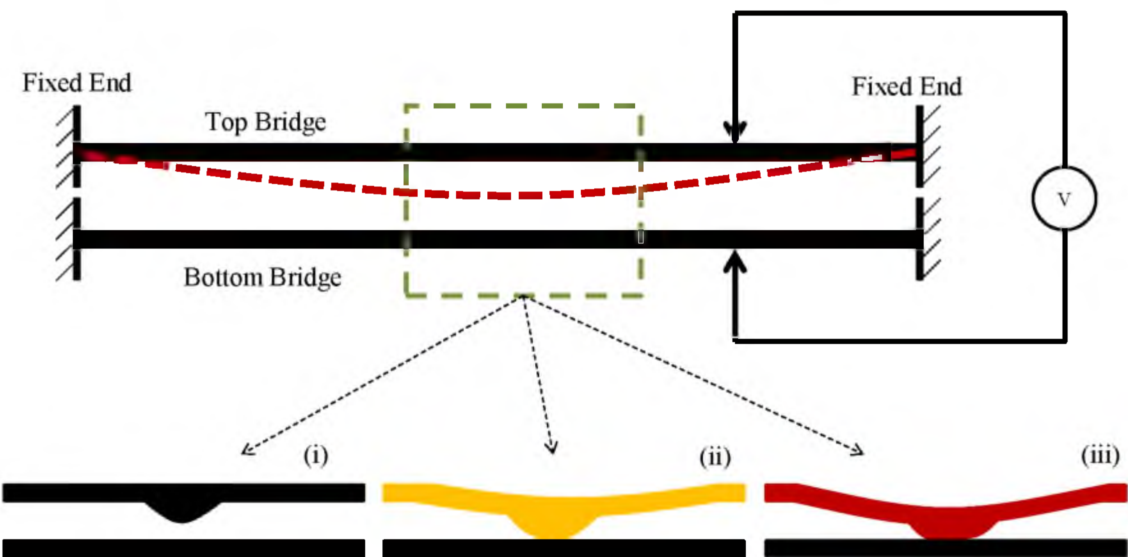


Figure 2.11: Modeling contact resistance

Their theories explain that a rough surface can be represented by a collection of independent spherical asperities with identical radii having a statistical height distribution. On the model proposed in [35], the deformation is calculated on the basis of volume conservation of the asperity under observation. These theories were applied to electrostatic switches by S. Majumder et al. [36] and are utilized in the simplified modeling presented here.

The effective modulus of elasticity is given by:

$$\frac{1}{E'} = \frac{1-v_1^2}{E_1} + \frac{1-v_2^2}{E_2} \tag{25}$$

where E_1 and E_2 are the moduli of elasticity if the contacting surfaces, v_1 and v_2, are their Poisson's ratios, respectively. For an elastically deformed asperity, the relationship between radius of the contact spot and the contact force is given by

$$r = \left(\frac{3FR_t}{4E'}\right)^{1/3} \tag{26}$$

Here, R_t represents the end radius of curvature of the asperity. The contact radius r can be related to its vertical deformation, α, by

$$r = \sqrt{R_t \alpha} \tag{27}$$

It is assumed that plastic deformation commences when the maximum pressure at the contact interface exceeds 0.6 x hardness (H) of the contacting material. Thus, the vertical deformation qualifies to

$$\alpha_c = \left(\frac{0.3\pi H}{E'}\right)^2 R_t \tag{28}$$

Assuming an average pressure of $0.6H$ in the plastic region, the contact force is evaluated out to be

$$F = 0.6\pi H r^2 \tag{29}$$

So, taking into account the conservation of asperity volume, the contact radius per asperity is

$$r = \sqrt{R_t \alpha \left(2 - \frac{\alpha_c}{\alpha}\right)}, \qquad \alpha > \alpha_c \tag{30}$$

As a result, the force on each asperity as well as the radius of each can be calculated when the vertical deformation is known.

When applied to a real-world problem comprising a surface with "finite roughness", say n asperities, each with a postdeformation (end) radius R_t, and heights $z_1>z_2>\ldots z_n$, with separation d between them and a given contact force F such that

$z_n > d > z_{n+1}$, then the asperities numbered 1, 2, …, n come into contact and the vertical deformation of asperity i is given by

$$\alpha_i = z_i - d \tag{31}$$

To relate the deformation radius change to the contact resistance change, we can assume that a single spot (asperity) with radius r separates two semi-infinite bodies of resistivity ρ. The resistance is dominated by the Sharvin mechanism [37] provided that the spot radius is small compared to the electron mean free path l_e. In this case, electrons are projected ballistically through the contact asperity without scattering. The resistance is now given by

$$R = \frac{4\rho l_e}{3\pi r^2} \tag{32}$$

Conversely, if the radius r is much larger than l_e, the resistance is dominated by diffuse scattering mechanism given by the Maxwell resistance formula [38]

$$R = \frac{\rho}{2r} \tag{33}$$

For a solution that accounts for the transition between the Maxwell and Sharvin regions, Wexler [39] used the variational principle for resistance of a circular contact spot separating semi-infinite bodies and has produced a solution of the Boltzmann equation

$$R = \frac{4\rho l_e}{3\pi r^2} + v\frac{l_e}{r}\frac{\rho}{2r} \tag{34}$$

Essentially, on a real surface, there are multiple asperities of varying sizes that make contact with the surface. The resulting effective contact resistance depends on, both, the radii of the asperities as well as their distribution. To evaluate a range of the contact resistance, we can imagine the lower bound to be determined by a situation where each asperity, i, is independent of one another and separated such that they conduct in parallel, such that

$$\frac{1}{R_{lb}} = \sum_i \frac{1}{R_i} \tag{35}$$

where R_i is the contact resistance of a spot. The upper bound is consequently a state where all the asperities can be assumed to form one unanimous contact with an effective circular spot with radius r_{eff}. In this case, the contact resistance evaluates out to

$$R = \frac{4\rho l_e}{3\pi r_{eff}^2} + v\frac{l_e}{r}\frac{\rho}{2r_{eff}^2} \tag{36}$$

It is reported that on a model with one asperity, all contact resistance characteristics (bounds) are identical at low contact forces (<1µN) [36]. The upper and lower bounds of resistance are very tight. This, however, becomes progressively looser as the model accommodates for an increased number of asperities. Additionally, there is a considerable discrepancy between theoretically predicted and experimentally determined contact resistance characteristics at low contact forces [36]. The agreement between

theory and experiment, however, is significantly better at larger contact forces (>10μN). This can be attributed to several factors, such as the model here does not account for adhesive forces between contacts, an insulating film is generally present at the interface, and that the interfacing asperities deform plastically at low contact forces so that the contact resistance at the next cycle is influenced by it.

2.1.5. Discussions

The complexity of a MEMS switch lies in its ability to harness multiple energy domains such as electro-mechanics, optical electricity, thermoelectricity, and electromagnetism into a single device. These render the design and operation of MEMS switches anything but trivial. As seen from the discussions presented in this section, various models can be employed to understand and exemplify aspects of the operation of a MEMS switch. Here, a lumped-mechanical model, electrical equivalent circuit model, and theories behind contact resistance leading to reliability issues are discussed. These models/theories combine a multitude of interdisciplinary parameters ranging from thin film stresses, spring constants, capacitances, resistances, etc. and require intimate understanding in the areas of materials science, mechanical engineering, physics, and mathematics combined rendering the analysis multidisciplinary. A thorough understanding of the quasi-static pull-in voltage, dynamic response, and reliability, amongst others, is critical to being able to successfully design a MEMS switch that performs up to required specifications.

2.2. Theoretical Analysis

2.2.1. Calculations

Based on relatively well-developed mathematical models of fixed-fixed MEMS beams, switching time, frequency, and pull-down voltages were calculated (using equations 37-40) [1] for various thicknesses of silicon nitride, polysilicon, and tungsten. The results are shown in Fig. 2.12(a)-(c). Equations (37)-(40) were used in a MATLAB program to plot the relationships.

$$k_a = k_a' + k_a'' = 32Ew\left(\frac{t}{l}\right)^3\left(\frac{27}{49}\right) + 8\sigma(1-v)w\left(\frac{t}{l}\right)\left(\frac{3}{5}\right) \tag{37}$$

$$V_p = V\left(\frac{2g_0}{3}\right) = \sqrt{\frac{8k_a}{27\varepsilon_0 Ww}g_0^3} \tag{38}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_a}{m}} \tag{39}$$

$$t_s = 3.67\frac{V_p}{V_s\omega_0} \tag{40}$$

where,

k_a = Overall spring constant

k_a' = Spring constant component due to material properties

k_a'' = Spring constant component due to biaxial residual stress

E = Young's Modulus

l, w, t = Beam dimensions (length, width, thickness)

σ = Biaxial residual stress

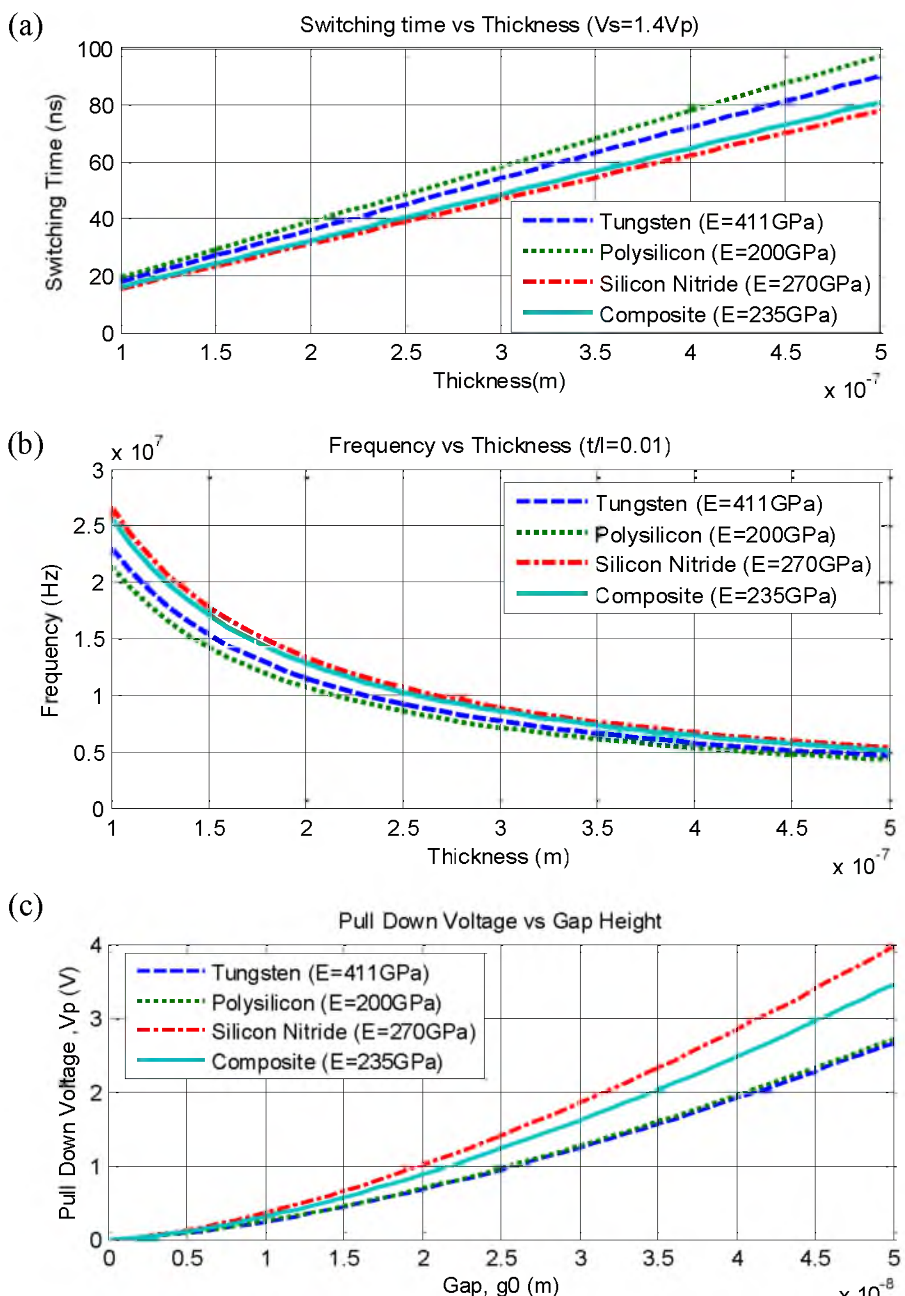


Figure 2.12: Graphs showing calculated a) switching time vs thickness for fixed length using Tungsten, Silicon Nitride, Polysilicon, and a composite of SiN and PolySi used in existing device. f_0~MHz range, b) resonant frequencies corresponding to various bridge thicknesses at thickness/length ratio = 0.01. Bridge width is fixed at 12µm, c) pull down voltage vs gap height (g_0) for l=30µm, w=12µm.

v = Poissons ratio

V_p = Pull-down voltage

ε_0 = Permittivity of free space

g_0 = Beam actuation gap height

f_0 = Resonant frequency

m = Effective mass

V_s = Applied external switching voltage

t_s = Switching time

It is seen from Fig. 2.12(a) that silicon nitride-based devices have faster switching speeds than polysilicon or tungsten as a function of bridge thickness, with the bridge length fixed at 30 µm and width fixed at 15 µm. This is mainly due to the large stress built into the nitride layer during deposition.

However, it was experimentally observed that to structurally reinforce the silicon nitride throughout the fabrication process, a composite structure of silicon nitride (100nm) and polysilicon (200nm) was preferable – the nitride being placed on the inner side of the cross-bridge platform. The resulting composite bridge had a performance very comparable to one built using silicon nitride alone (<10% difference in switching time, frequency, and actuation voltage for 300nm combined thicknesses and 30nm gap height), with the added benefits associated with processing Polysilicon in BOE (buffered oxide etchant) without deteriorating the silicon nitride.

Actuation voltage for each material was also calculated and is shown in Fig. 2.12(c). It can be predicted based on calculation results that sub-1V actuation is possible

with the appropriate combination of bridge dimensions and an air gap of 10nm. These results were used to further design and simulate the logic gate devices.

2.2.2. COMSOL Simulation

COMSOL simulation for the XOR and AND gates was carried out at Case Western Reserve University and the processes are detailed in the Ph.D. dissertation of Dr. Sijing Han [40]. Fig. 2.13 illustrates a 3D FEA simulation carried out on the XOR gate. With permission, the most relevant results are extracted and compiled in Tables 2.1 and 2.2 in this section. The dimensions of the various parts are provided in Chapter 4. The simulations were programmed to terminate at $(2/3)g_0$ and the tunneling current was modeled using Fowler-Nordheim tunneling approximation.

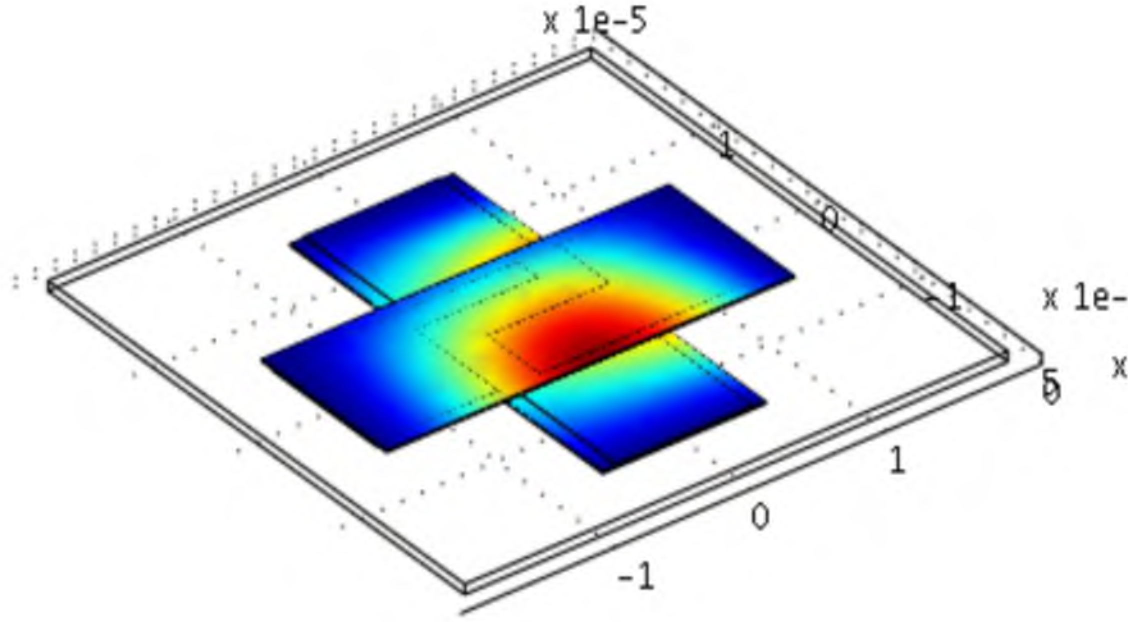


Figure 2.13: 3D FEA modeling of "XOR" gate.

Table 2.1: COMSOL simulation results for the "XOR" switch.

Device Characteristic	**FEA Modeling Result**
Pull-in Voltage	
Switching time	
Frequency	

Table 2.1 continued.

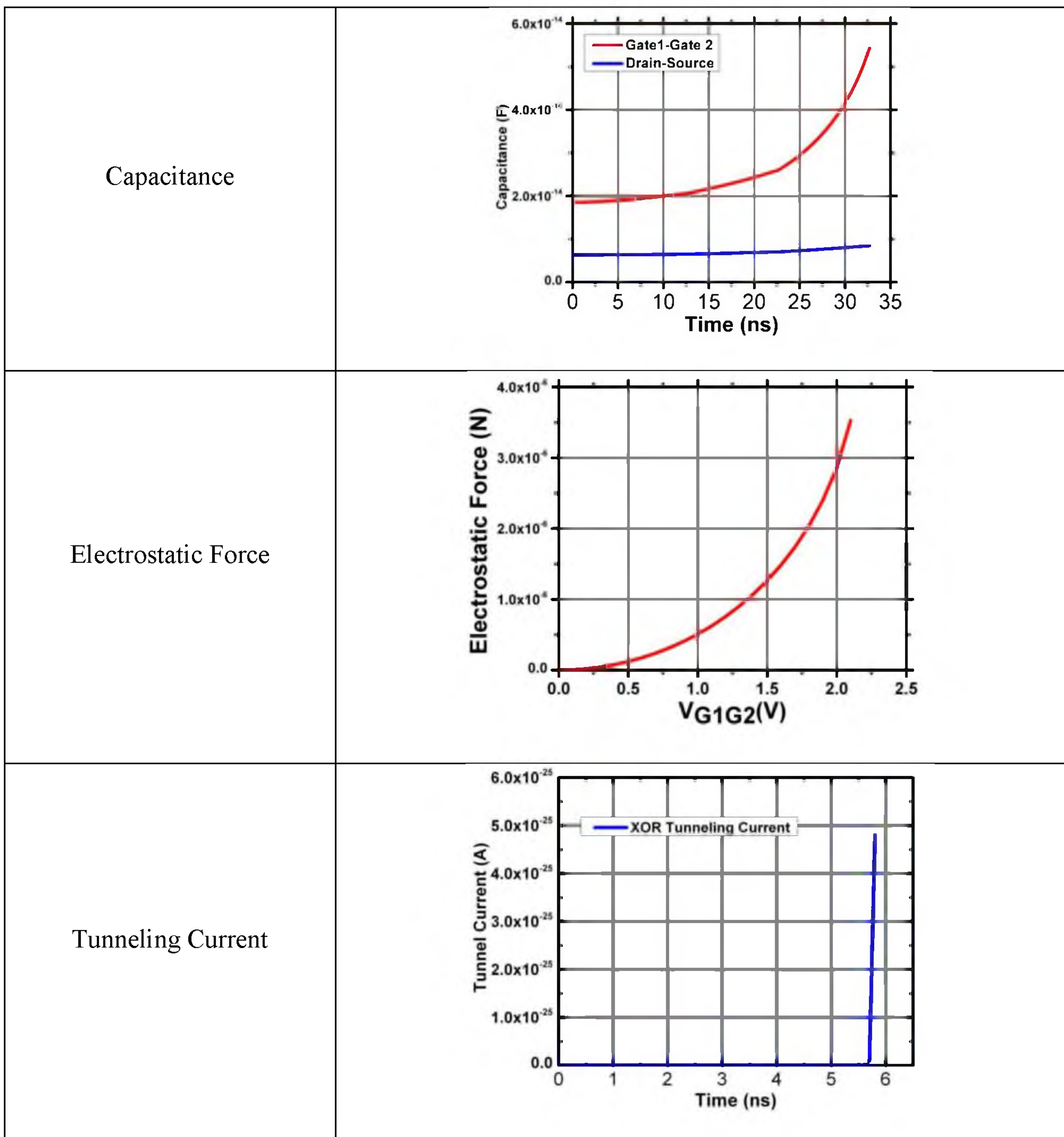
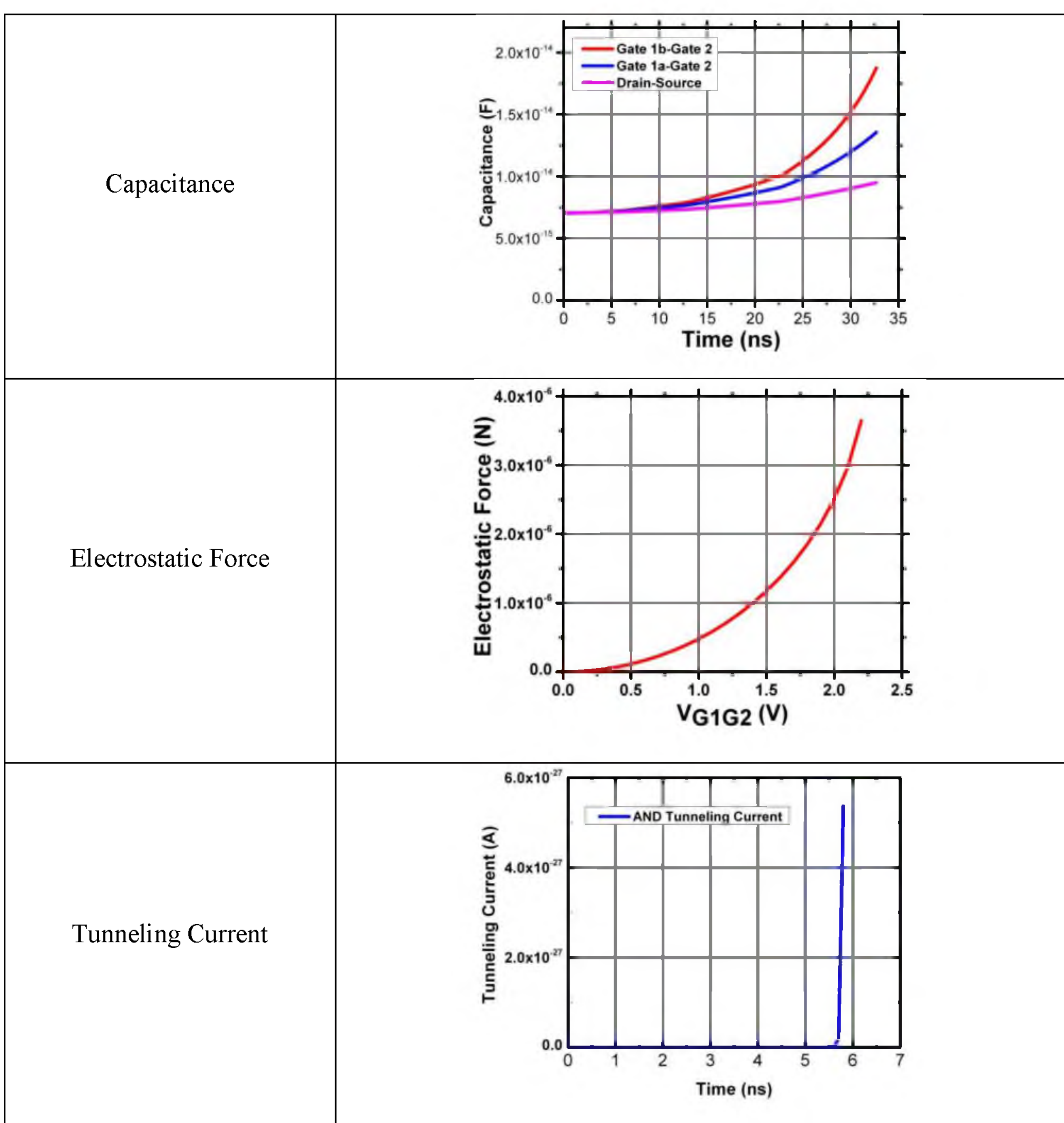


Table 2.2: COMSOL simulation results for the "AND" switch.

Device Characteristic	**FEA Modeling Result**
Pull-in Voltage	
Switching time	
Frequency	

Table 2.2 continued.



From Tables 2.1 and 2.2, the simulation results reveal pull-in voltages of roughly 2V, switching times approximately 30ns, maximum electrostatic forces of 350μN, and the leakage currents are infinitesimally small, even just before snap-down. These are for single-device logic gates having dimensions described in Section 4.2.1 of this thesis.

2.3. Summary

This chapter discusses the significance of understanding the dynamics involved and the complexity associated with modeling a MEMS switch. These are attributed to the multiple energy domains involved such as electro-mechanics, optical electricity, thermoelectricity, and electromagnetism.

Due to the interaction between electrostatic and structural domains in electro-mechanical systems, various physical parameters are involved and lead to a highly non-linear and unstable system. The chapter uses a mechanical lumped model and an electrical circuit equivalent model to evaluate the quasi-static pull-in voltage, transient behavior during a pulsed signal, and reliability of MEMS switches. Furthermore, approximate numerical calculations are discussed that evaluate performance of various dimensions of the MEMS logic gates. Finally, COMSOL simulation results are included that confirm the calculated operation values.

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CHAPTER 3

CONTACT RESISTANCE EVOLUTION

This chapter presents an investigation of the evolution of contact resistance (R_c) of electrical contacts over 100,000 cycles. A contact-mode atomic force microscope connected to a current versus voltage (I-V) measurement system was used and successive I-V measurements between a Cr-coated AFM conducting tip and Ir, Pt, W, Ni, Cr, Ti, Cu, or Al thin-film metals on silicon in a nitrogen ambient were done. Additionally, a similar experiment was conducted on layers of graphite also. The contact regions were subsequently imaged using SEM and contact-mode AFM to correlate changes that occurred in the surface morphology, roughness, $V_{pull-in,}$ and R_c. Adhesion forces between the conducting AFM tip and the thin-film material substrate was also measured. Three different regimes were observed in the evolution of R_c (=dV/dI) as a function of switching cycles. The first or initial regime lasted up to a few 100 cycles. In some cases, the contact resistance in this regime went down (improved, perhaps, due to clearing of the oxide layers or anodic etching), but on the average, the contact resistance was nearly constant. The second or middle regime started at a few 100 cycles and lasted up to 30,000 cycles. In this regime, the contact resistance changed gradually as a function of switching cycles and become larger in most metals tested here. The surface morphology of the contact area changed rapidly in this regime. The third or final regime started from ~30,000 cycles and

went up to 100,000 cycles. In this regime, the contact resistance usually reached its maximum value and remained constant in most cases. Additionally, the surface morphology of the contact area also remained constant. The initial R_c of Ir, W, Pt, Cu, Al, Ti, and graphite were low (10^6-10^8 Ω) compared to other metals (Ni~$10^{11}\Omega$ and Cr~$10^{12}\Omega$). The best cyclic I-V performers were Ir, Pt, W, and graphite. The trend in changing R_c seen here was similar and can be attributed to one of several factors, including their high Young's modulus, high melting temperatures, and high density along with low adhesion forces. The worst were Ni and Cr, showing large contact resistance throughout experimentation but having midrange material properties (conductivity, density, melting temperature, and adhesion forces). Ti illustrated an interesting behavior where contact resistance improved as a function of cycling. Between Cu and Al – both high conductivity metals – Cu developed abrupt failure, while Al gradually developed failure over repeated I-V cycling.

3.1. Overview

It is known that cycling MEMS switches deteriorate the contact area as a function of time due to a multitude of phenomena, including surface pitting, fatigue, asperity generation, charge migration, stiction, and micro-welding and other physical damages. MEMS switches that require reliable "hot-contact" should have their materials suitably selected to survive >10^{12} switching cycles without degradation due to the above-mentioned phenomena. In spite of the numerous reports of 10^8 - 10^{10} successful switching cycles reported in literature [1-8] and the large research interest from several groups in academia and industry [9-18], efforts made to unravel the metrological secrets of repeated

cycling still remain fairly short of achieving a clear understanding of what really governs the "perfectly reliable" MEMS/NEMS switch. Some general guidelines for the ultimate contact material have been determined and include high melting temperature, high Young's modulus, low contact resistance, low diffusivity, dissimilarity between the two contact materials (i.e., they should have different crystal structures, conductivity, etc.), and in some cases, the ability to "replenish" or "heal" itself over time.

It is important to optimize parameters of contacting materials in hot-contact switching and understand the degradation of the contact areas over a function of time, current densities, switching cycles, and peak versus average electric power per switching event (P=IV), etc. In a hypothetically perfect MEMS switch comprised of minimal asperities (and therefore minimal "hot-spots"), operating at low voltages and limited to low currents, one can significantly reduce the possibility of micro-welding. Similarly, the issue of stiction due to electrostatic or ambient origins can be addressed using dissimilar metal contacts on the two electrodes as studies have shown that materials with dissimilar crystal structures result in large repulsive Casmir forces and are beneficial to prolonged MEMS switch lifetime. Dissimilar metals with dissimilar crystal structures also hinder the possibility of solid diffusion in the "hot-spots" and, as a result, can reduce stiction-related failure [12]. Other properties, such as a high Young's modulus, contribute by way of large mechanical restoring forces within the structure of the switch and may be directly related to high melting temperatures of the contact materials that usually reduce the diffusion coefficient and, hence, reduce the possibility of micro-welding.

The ideal contact material can be envisioned to have very low contact resistances to begin with, be highly immune to oxidation or its oxide is highly conductive. Some

interesting materials, like graphene (or graphite), are difficult to oxidize or create defects into due to their 2D structures. Additionally, graphite, if processed appropriately, can be made to "flake" off a few thin layers of graphene after a predetermined number of switching cycles, revealing a pristine contacting surface with low contact resistance over its lifetime. This may be undesirable in MEMS environments due to particulate generation; however, from a purely electrical-contact perspective, it could render graphite to be highly reliable. Other variants include using materials that are softer in nature, such as Au, and can be made to "flow" and restore their contact surface under certain conditions. An extension of this can be the use of liquid metal contacts for MEMS such as Hg or Ga where the metals are liquid at room temperature and provide a fresh contact after every switching activity.

In order to investigate the origin of changes that occur in surface morphology of MEMS switches, extensive voltage vs. current cycling was carried out on a range of materials generally employed for MEMS, such as, Iridium, Platinum, Tungsten, Nickel, Chrome, Titanium, Copper, and Aluminum (all 100nm thickness), using a specially modified AFM setup for contact mode I-Vs. Apart from these metals, layers of graphite were also tested in a similar way. The setup used Silicon AFM tips coated with 100nm Cr as one electrode and the other material (material 'X'; X corresponding to metal on the list above) as the second electrode. Their electrical properties were recorded as a function of time while cycling voltage between them. Their surface morphology after repeated I-V cycling was examined by SEM and AFM studies and was analyzed. The initial R_c of Ir, Pt, W, Cu, Al, Ti, and graphite were low (10^6-10^8 Ω) compared to other metals (Ni~$10^{11}\Omega$ & Cr~$10^{12}\Omega$). The trend in changing R_c seen in Ir, Pt, W, and graphite are similar and can be

attributed to one of several factors, including their high Young's modulus, high melting temperatures, hardness, high density, and their dissimilarity in crystal structure, especially emphasized in graphite and Ti. In addition to re-arrangements of metal atoms near the surface, possible oxidation, and micro-welding in the contact region, we also see "clearing" of the contact region from thin-film metal in some cases. This may be due to the lateral motion of the contacting AFM probe. In addition, adhesion forces for each material were also computed by force vs. displacement measurements using an AFM setup. There is a relationship between adhesion forces and defect generation in the contact region and the results of both sets of experiments are detailed here.

3.2. Experimental Setup

3.2.1. Cyclic I-V

The I-V experiments were carried out using eight different metals as follows: Iridium, Platinum, Tungsten, Nickel, Chrome, Titanium, Copper, and Aluminum and one nonmetal: graphite. All metals were deposited to a thickness of 100nm via DC sputtering over a 4" Silicon wafer coated with LPCVD silicon nitride (500nm). Iridium and Platinum required an adhesion layer of Cr (~8nm). The wafers were diced into 1cm^2 pieces for convenience during experimentation. In addition, chromium, out of the eight metals under investigation, was chosen to coat the AFM tips to a thickness of 100nm. As a result, the experiment was conducted with Metal X vs. Cr-coated AFM tip, where X represents the respective metal under investigation. Each sample was coated with photoresist (PR) (thickness 2um) during storage. Immediately prior to experimentation, this PR was stripped using Acetone/Methanol/DI water and dried using a N_2 gun. This

step ensured that minimal surface oxidation due to ambient conditions during storage contributed to our cyclic I-V experimentation. The graphite sample was prepared by extracting layers of graphite (graphene) from bulk graphite using double-sided tape and transferred to a silicon nitride coated silicon wafer. The experiment was set up as shown in Fig. 3.1.

Due to its simple design and relative ease of use, a TT-AFM system was employed to mount the AFM tip and the metal substrate. The entire experimental setup was housed inside a plexi-glass enclosure with a constant N_2 flow, temperature controlled to 26℃ and humidity to 35%. External to the controlled chamber was a Keithley 236 Source Measure Unit (SMU) and a computer that was used to control and record readings off the SMU.

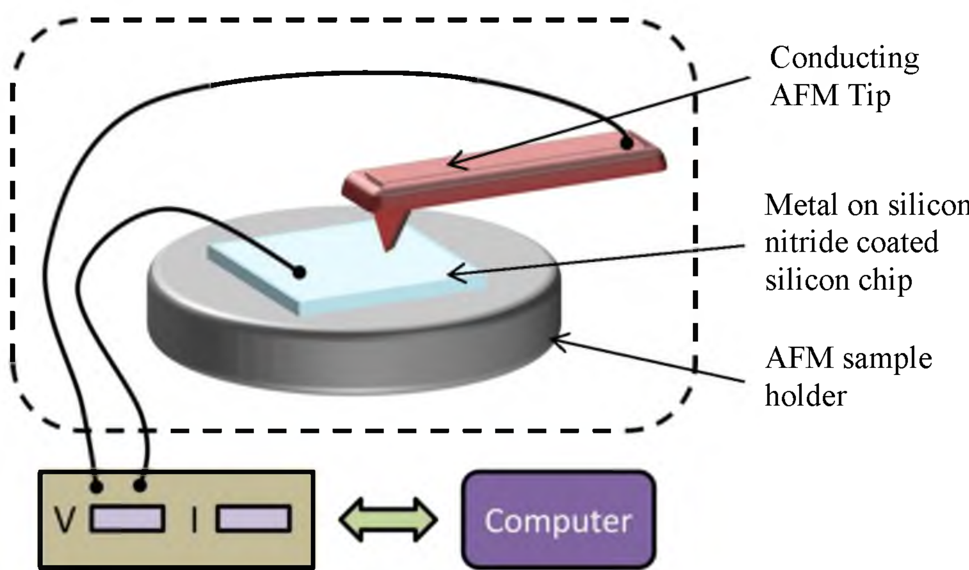


Figure 3.1: Experimental setup for I-V. A Keithley 236 Source Measure Unit was controlled via a computer (LabView program) to operate the cyclic voltage and record corresponding current

The LabView program used to control the cyclic voltammetry was programmed to run from +3V to -3V at 0.25V steps indefinitely. A counter was used to keep track of the nth cycle that was being run. A closed circuit was set up between the SMU, AFM tip, and the metal substrate whereby the change in I-V characteristics due to repeated cycling of voltage and current was recorded.

After the experiment was successfully set up, the program was run and allowed to record the I-V characteristics indefinitely over a period of approximately 9-12 days. At an operating frequency of about 500 I-V cycles per hour, this allowed sufficient time to exceed 100,000 cycles of operation.

3.2.2. Adhesion Force Measurement

Here, the adhesion force of an AFM-tip to different materials was measured as this can be considered to be a reasonable substitute to model the behavior of MEMS and NEMS switches. The adhesion force is a result of various physical and chemical forces, such as, electrostatic and van der waals [19]. Several methods for obtaining adhesion forces of thin films to their substrates exist, such as peeling, shearing-off, pulling-off, centrifugal means, scratching, and twisting [20] and each method has its own respective advantages and disadvantages.

In this case, a Veeco Atomic Force Microscope was used to obtain adhesion forces between the nine samples and a silicon tip. The samples were mounted on AFM discs using conducting silver paste and were placed over the magnetic holder of the Piezo stage. To successfully obtain a force curve, first, the voltage to displacement sensitivity of the Position Sensitive Detector (PSD) sensor was calculated by ramping down the

flexible probe on a hard sample (steel disc); second, the stiffness of the cantilever was calculated using the thermal-tune option of the AFM or external nano-indenters in order to confirm the values reported on the AFM tip packaging. Using these two conversion factors, the voltage-displacement was converted to deflection-displacement and, consequently, force-displacement curves. In this manner, the force was obtained from the voltage difference generated by the laser spot movement on the PSD sensor. The horizontal axis was the vertical displacement of the sample piezo stage (Fig. 3.2).

Prior to touching the sample surface, the AFM tip was not deflected. This was also the case during the tip-approach phase; hence, the force curve was horizontal (Fig. 3.2, region A). Upon making contact with the surface, the sloped part was formed and this was due to the compliance of the probe and the contact regions of the sample and the tip (Fig. 3.2, region B). The retracting curve was almost the same, apart from the hysteresis behavior generated because of the adhesion between the probe and sample materials (Fig. 3.2, region C). To calculate the adhesion forces, the vertical length of the triangular hysteresis section of the force curve was measured accurately, by extracting F-Z data points of the force curve from the AFM software (Fig. 3.2, region D).

Each force curve for each metal was plotted at least 6 times from different parts of the sample in order to capture the mean value and standard deviations of measured values. These data are included in the results in Section 3.4.2. It is known that a thin layer of native oxide covers the silicon tip so that the graph is actually indicative of the adhesion forces between silicon oxide and the tested materials.

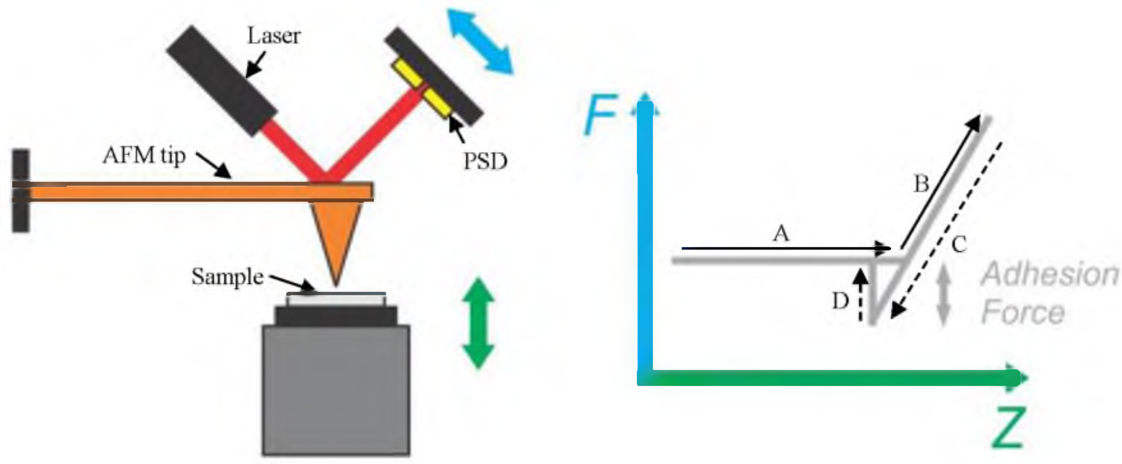


Figure 3.2: Schematic diagram illustrating the experimental setup of the AFM system used to capture a force curve

3.3. Results and Analysis

3.3.1. Cyclic I-V

The cyclic I-V data from each metal under investigation was obtained and metrology studies on the surface of the metal and AFM tip was carried out via AFM roughness measurements and SEM imaging. Fig. 3.3(a)-(i) illustrates the change in contact resistance as a function of number of cycles for each metal. Figs. 3.4 – 3.12 demonstrate the cyclic I-V data obtained for each metal: Ir, Pt, W, Ni, Cr, Ti, Cu, and Al and a nonmetal, graphite, respectively, at particular stages in their I-V cycling experiment. Each graph that illustrates the cyclic I-V characteristic at the particular cycle number illustrates a snapshot of the contact resistance at that particular instant. The sequence of six I-V graphs on each figure (Figs. 3.4 – 3.12) provides a birds-eye manifestation of how the contact resistance evolves as a function of operating cycle. These data were used to plot the resistance as a function of number of cycles, as shown in Fig. 3.3.

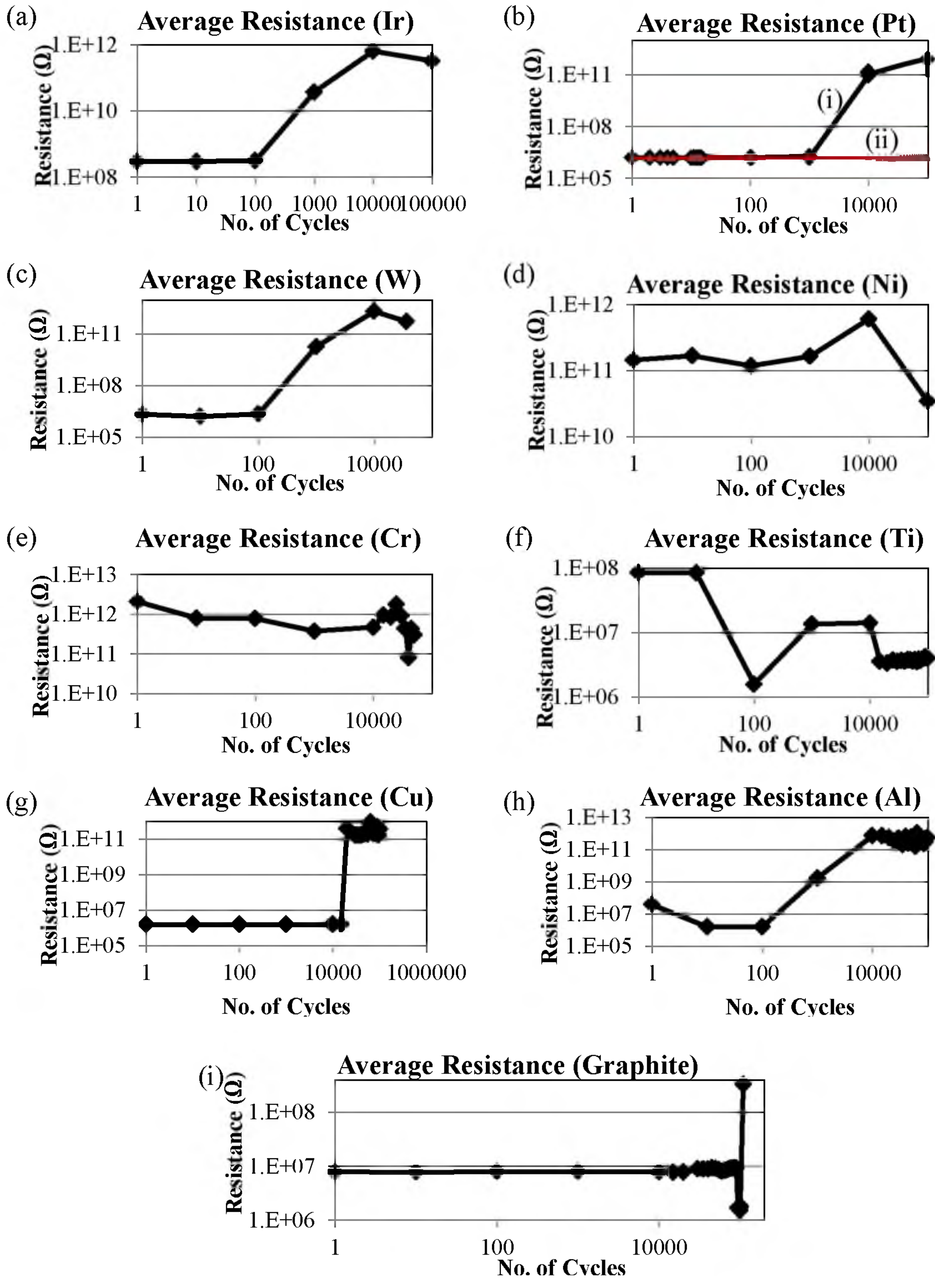


Figure 3.3: Summary of Resistance vs Number of I-V cycles for (a) Iridium, (b) Platinum with (i) thin Cr adhesion layer (8nm) and (ii) with thick Cr adhesion layer (100nm), (c) Nickel, (d) Tungsten, (e) Chromium, (f) Titanium, (g) Copper (h) Aluminum, and (i) Graphite.

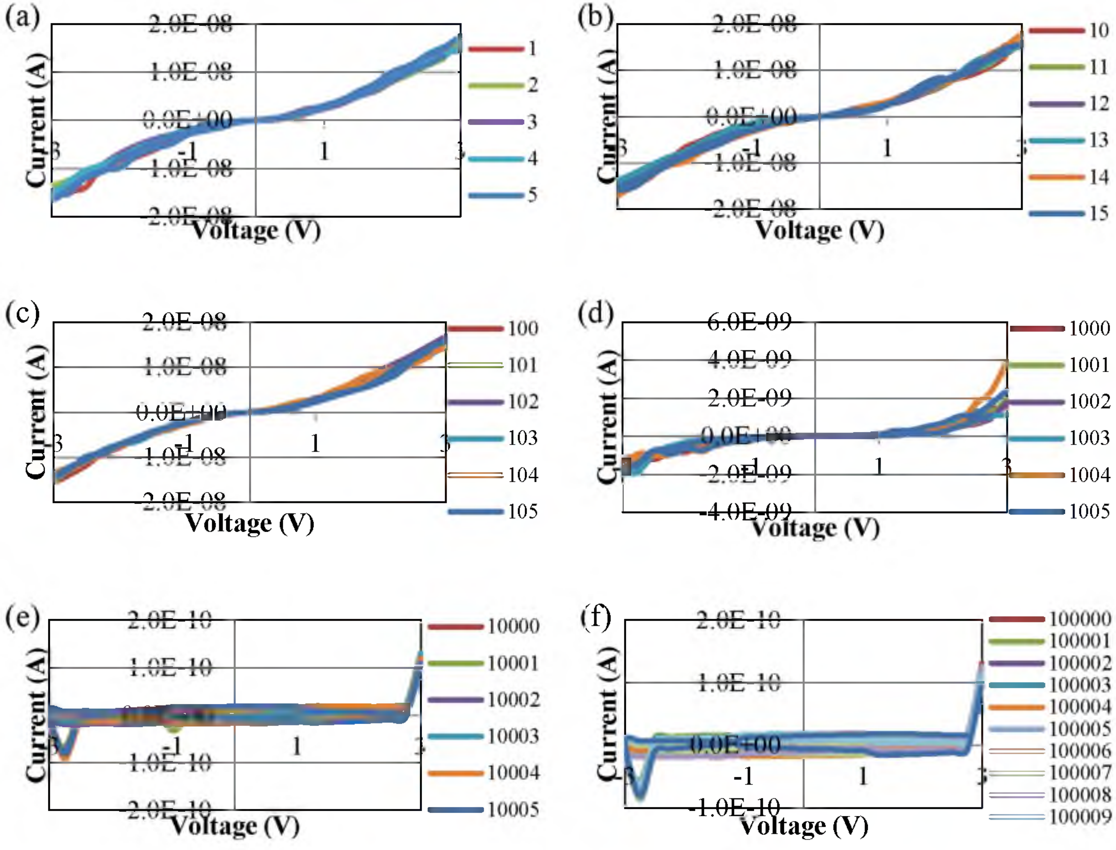


Figure 3.4: Cyclic I-V graphs on Iridium for (a) 1-5 cycles, (b) 10-15 cycles, (c) 100-105 cycles, (d) 1000-1005 cycles, (e) 10,000-10,005 cycles, and (f) 100,000-100,010 cycles

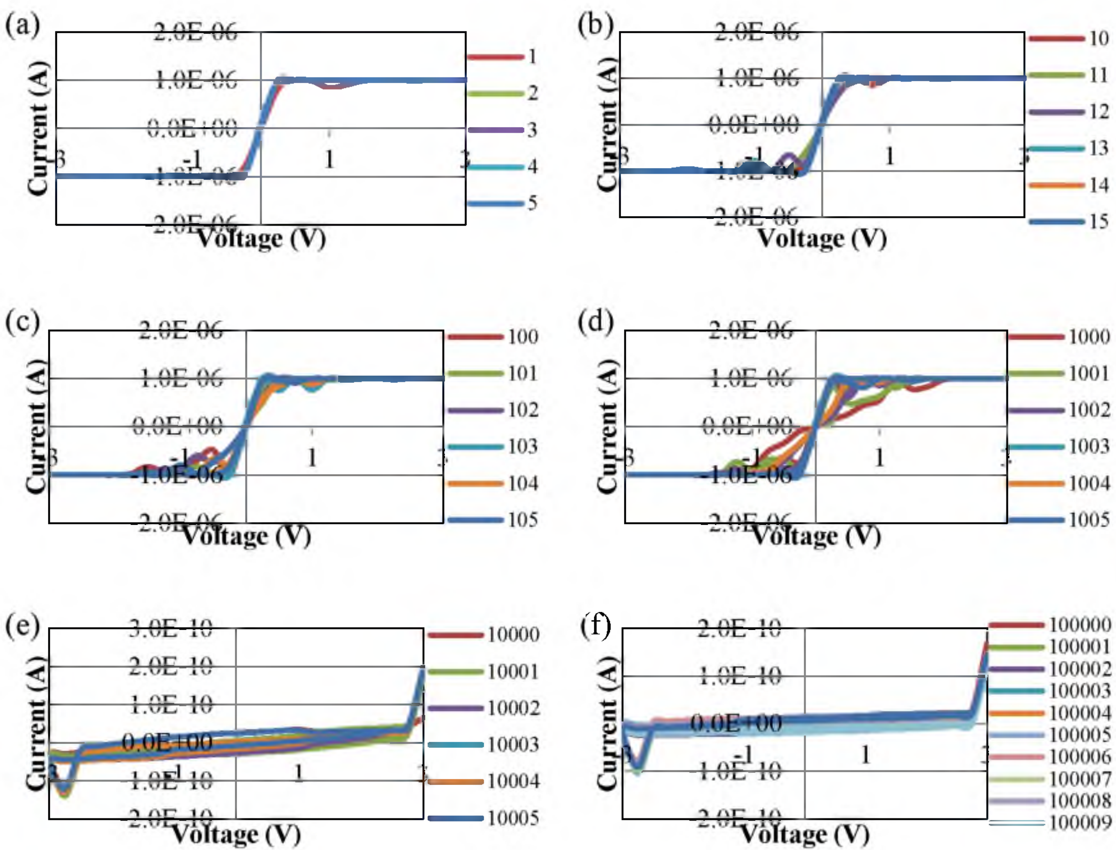


Figure 3.5: Cyclic I-V graphs on Platinum for (a) 1-5 cycles, (b) 10-15 cycles, (c) 100-105 cycles, (d) 1000-1005 cycles, (e) 10,000-10,005 cycles, and (f) 100,000-100,010 cycles

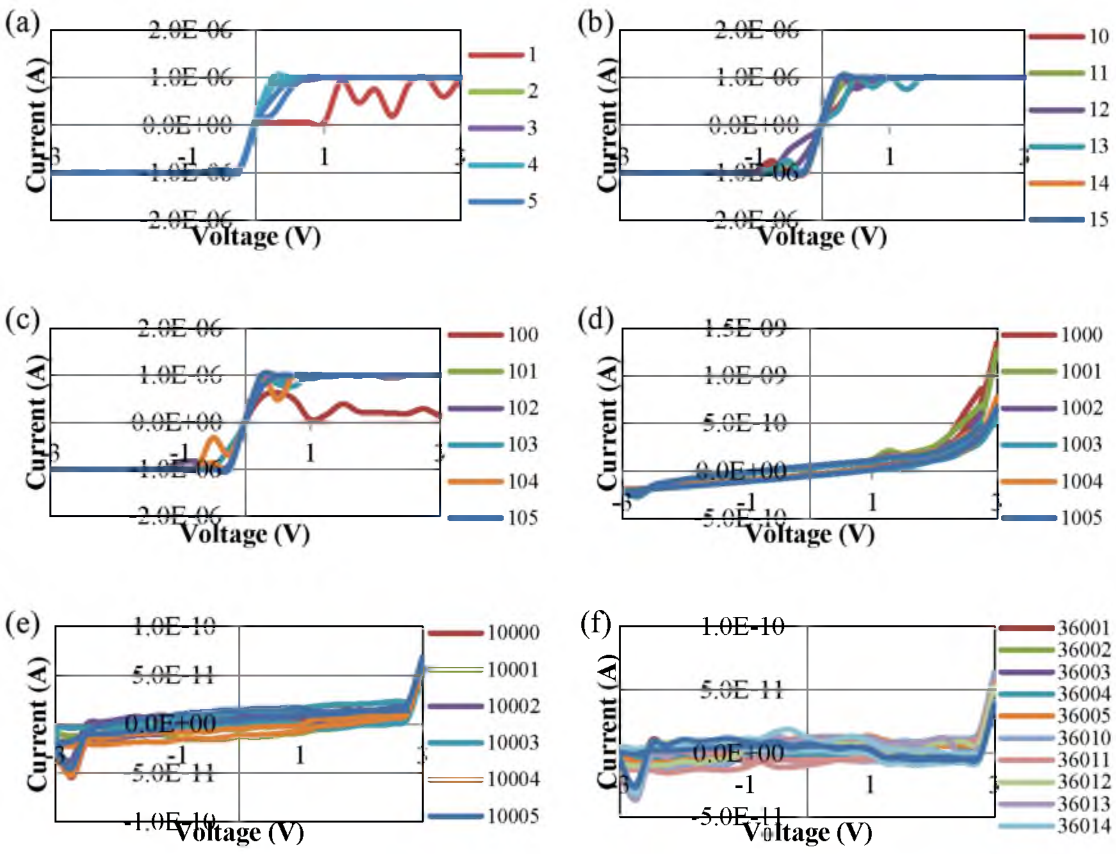


Figure 3.6: Cyclic I-V graphs on Tungsten for (a) 1-5 cycles, (b) 10-15 cycles, (c) 100-105 cycles, (d) 1000-1005 cycles, (e) 10,000-10,005 cycles, and (f) 36000-36015 cycles

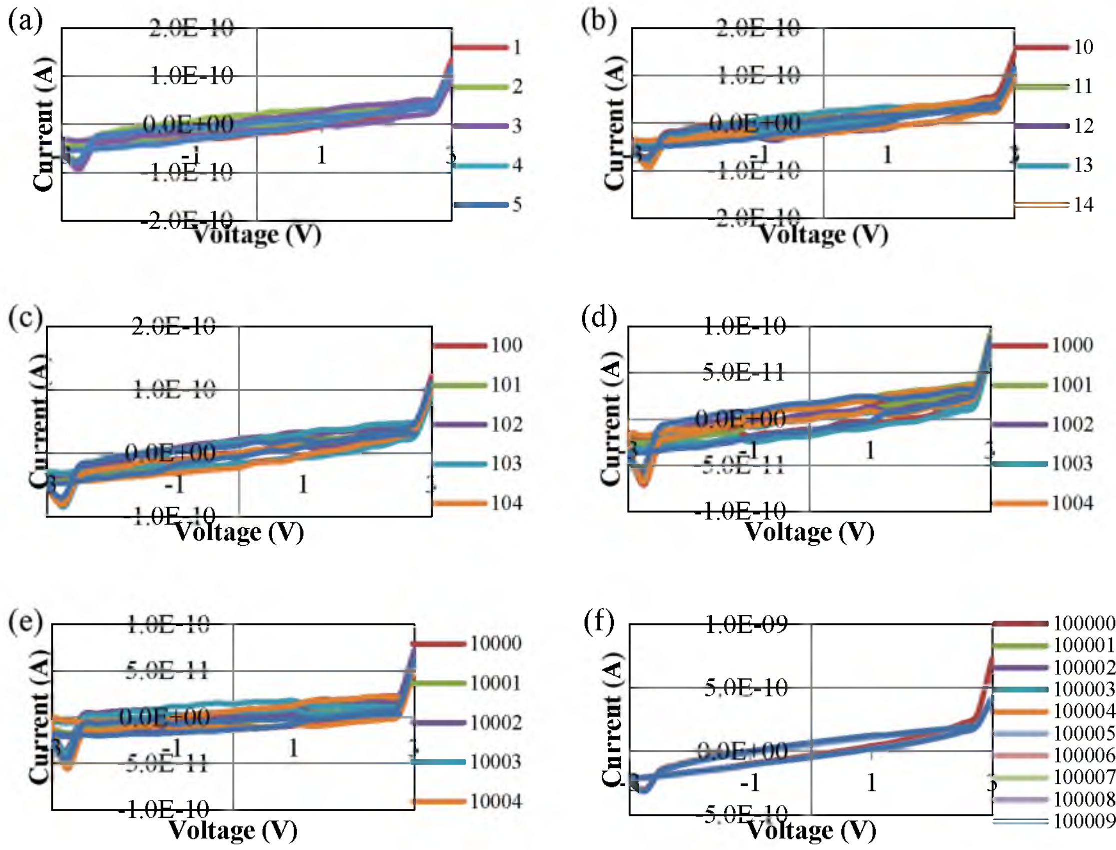


Figure 3.7: Cyclic I-V graphs on Nickel for (a) 1-5 cycles, (b) 10-15 cycles, (c) 100-105 cycles, (d) 1000-1005 cycles, (e) 10,000-10,005 cycles, and (f) 100,000-100,010 cycles

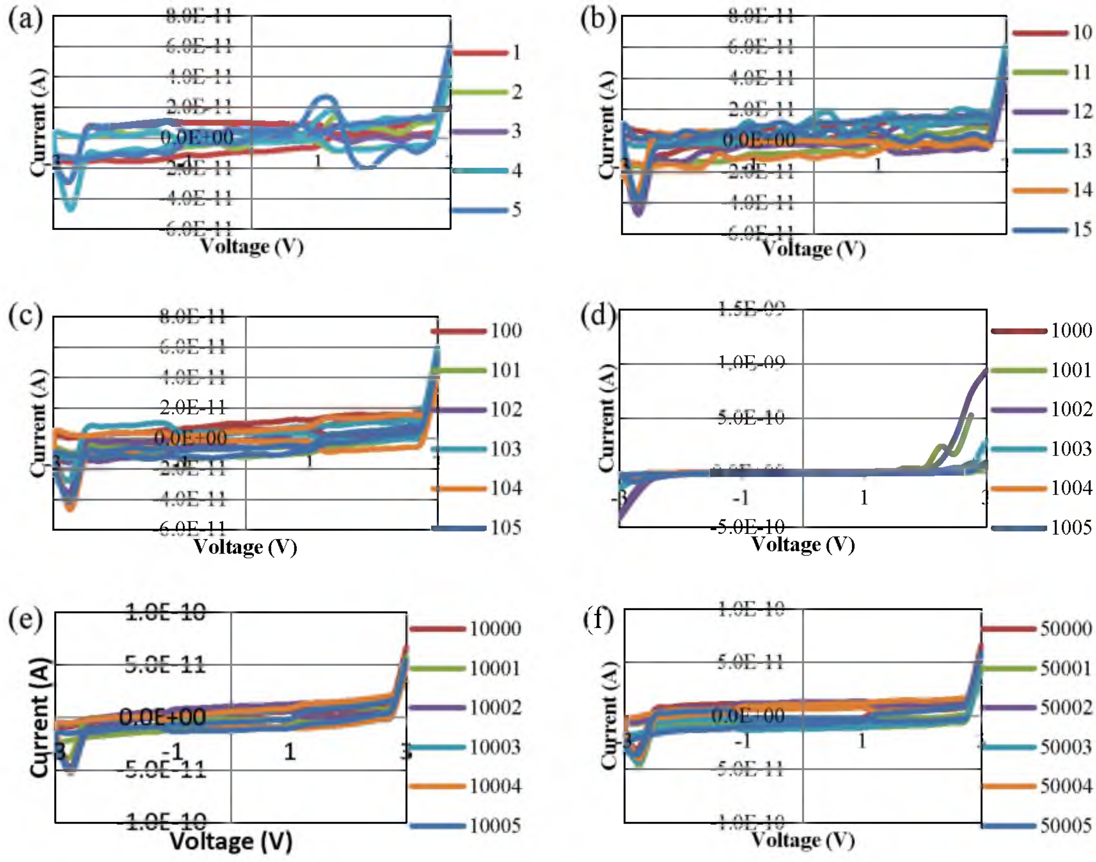


Figure 3.8: Cyclic I-V graphs on Chromium for (a) 1-5 cycles, (b) 10-15 cycles, (c) 100-105 cycles, (d) 1000-1005 cycles, (e) 10,000-10,005 cycles, and (f) 50000-50005 cycles

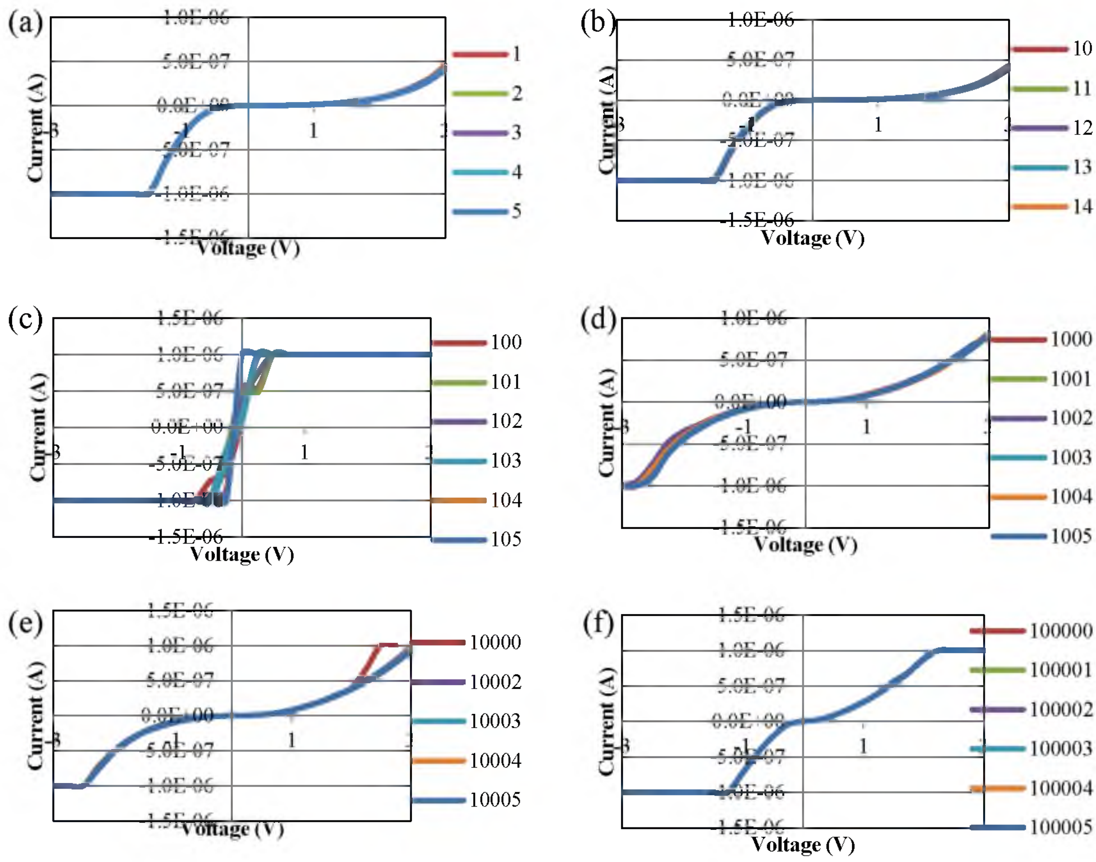


Figure 3.9: Cyclic I-V graphs on Titanium for (a) 1-5 cycles, (b) 10-15 cycles, (c) 100-105 cycles, (d) 1000-1005 cycles, (e) 10,000-10,005 cycles, and (f) 36000-36015 cycles.

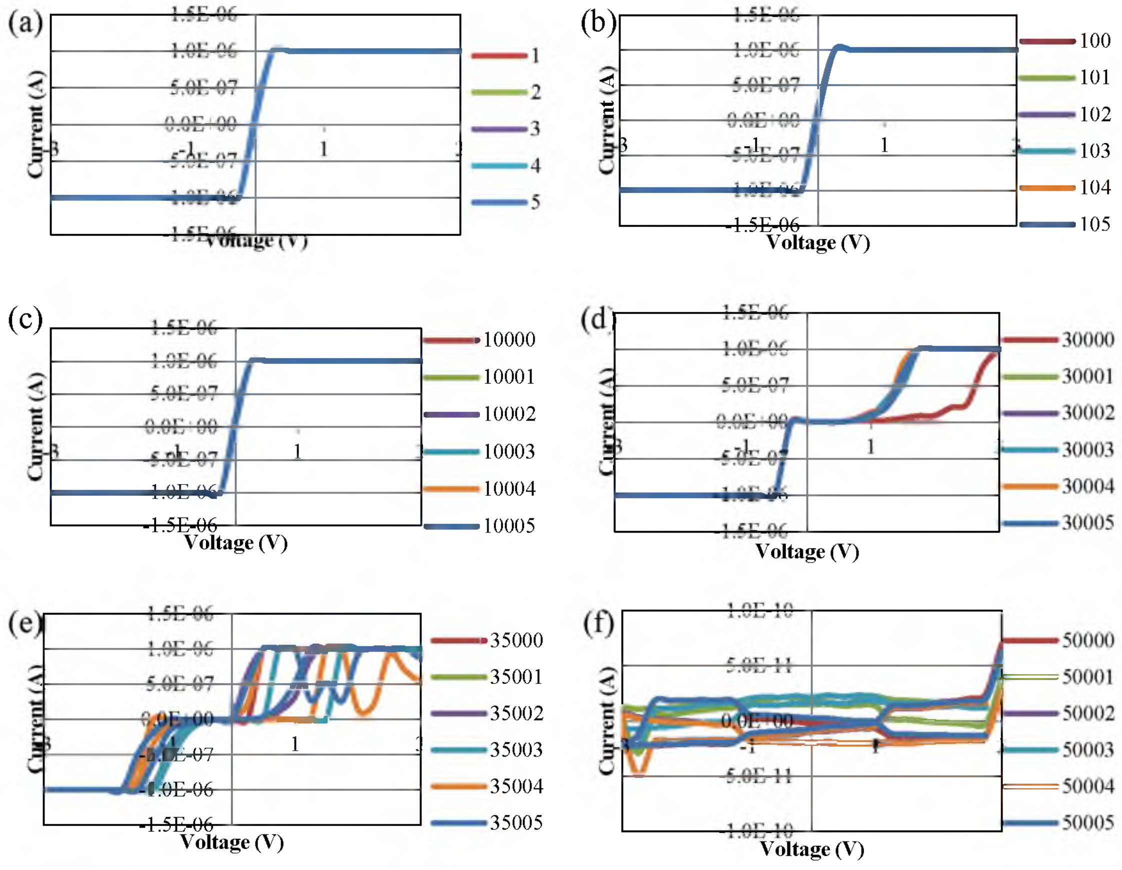


Figure 3.10: Cyclic I-V graphs on Copper for (a) 1-5 cycles, (b) 100-105 cycles, (c) 10000-10005 cycles, (d) 30000-30005 cycles, (e) 35,000-35,005 cycles, and (f) 50000-50005 cycles.

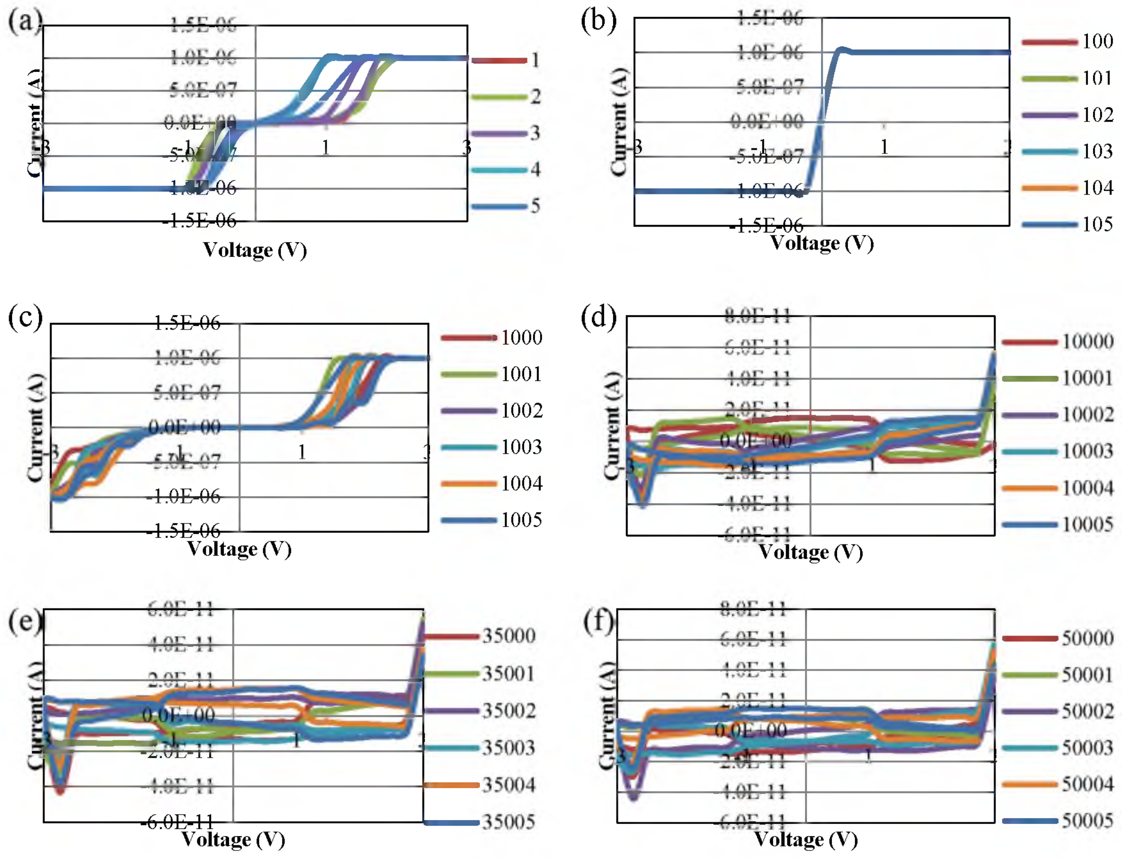


Figure 3.11: Cyclic I-V graphs on Aluminum for (a) 1-5 cycles, (b) 100-105 cycles, (c) 10000-10005 cycles, (d) 30000-30005 cycles, (e) 35,000-35,005 cycles, and (f) 50000-50005 cycles.

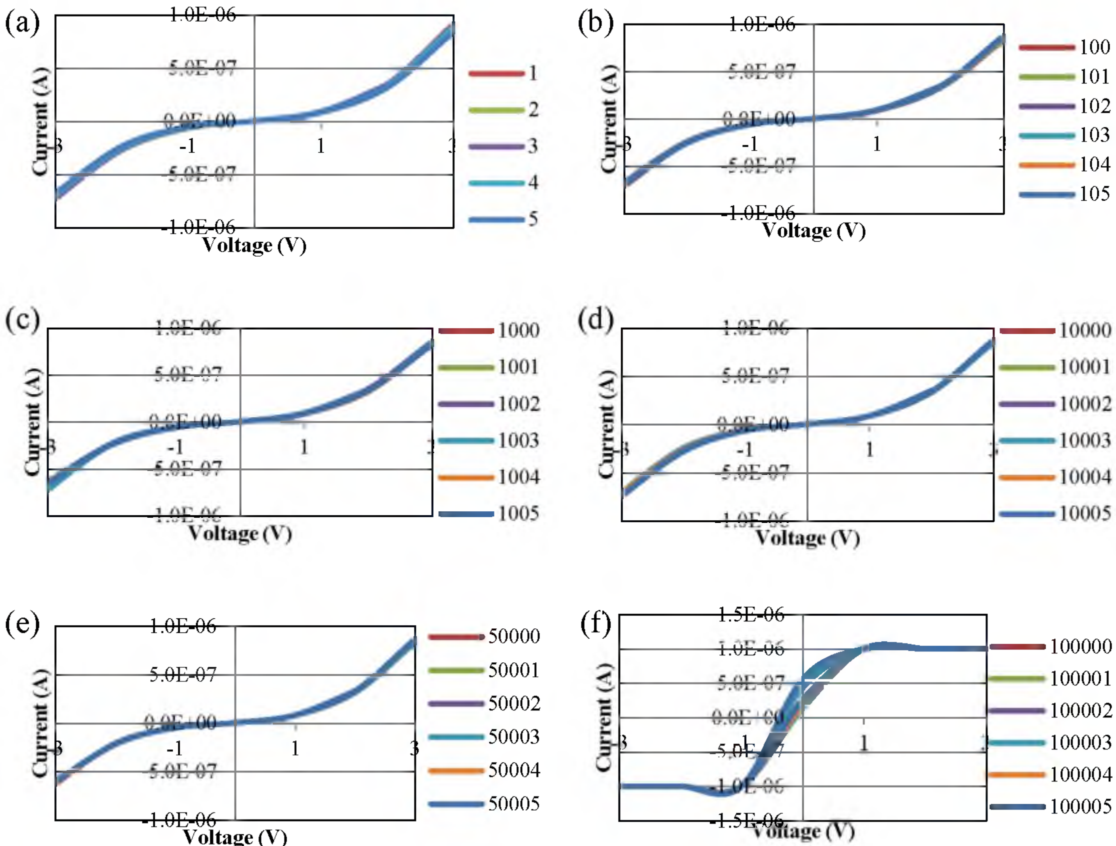


Figure 3.12: Cyclic I-V graphs on graphite for (a) 1-5 cycles, (b) 100-105 cycles, (c) 1000-1005 cycles, (d) 10000-10005 cycles, (e) 50,000-50,005 cycles, and (f) 100000-100005 cycles.

The first metal investigated was Iridium. On the I-V graphs shown in Fig. 3.4, corresponding to Iridium, it is seen that upon commencement of the experiment, the I-V characteristic appears linear – or ohmic. This trend is maintained throughout the first 100 cycles, after which gradual deterioration is observed beyond 1000 cycles and is exacerbated past this point. From Fig. 3.3(a), it is seen that the initial contact resistance is in the ~10^8 Ω to 10^9Ω regime. Beyond 1000 cycles (and up to 100,000 cycles), the trend in change in resistance illustrates approximately 4 orders of magnitude increase in resistance (to ~10^{12}Ω regime), indicating a catastrophic decrease in contact efficiency.

The next metal investigated was Platinum (with thin Cr adhesion layer – 8nm) and its cyclic I-Vs are shown in Fig. 3.5. These illustrate a perfectly ohmic contact during the initial stages (1-1000 cycles), which, as a function of time, also deteriorates in similar fashion as seen previously on Iridium. Pt illustrates a notably small initial contact resistance of ~10^6 Ω. From Fig. 3.3(b)(i), the increase in contact resistance from beginning to end of experimentation was approximately 5 to 6 orders of magnitude.

From the 1000th cycle onward, it is seen that the various effects, such as, surface pitting, fatigue, asperity generation, charge migration, stiction, micro-welding, and other physical damages leading to contact failure may be gradually developing. Towards the final cycles before experimentation was concluded, the area of electrical contact may be considered as entirely depleted via electron migration and therefore, nonconducting. On a separate experiment on Platinum, using a thicker Cr adhesion layer (100nm), it was seen that the average resistance remained at 10^6 Ω during the entire duration of the experiment (Fig. 3.3 (b)(ii)). This confirms the effect of electro-migration of Pt on the previous sample that contributed to its deteriorating contact resistance.

The results from investigating Tungsten are seen in Fig. 3.6. These graphs indicate that the metal performed consistently as an ohmic contact, albeit with a few exceptions until the first couple of 100s of cycles. The initial contact resistance was notably small (~10^6 Ω regime) compared to other metals. Beyond 1000 cycles, deterioration effects began to render the contact nonohmic and the area of contact degraded. The resulting increase in contact resistance at completion was approximately 6 orders of magnitude. The final contact resistance was close to the 10^{13} Ω regime, as seen from Fig. 3.3(c). The trends in changing contact resistance seen in Ir, Pt, and W are similar and can be attributed to one of several factors, including their common high Young's modulus, high melting temperature, and hardness that may be providing hindrance to rapid contact deterioration, such as that seen in Nickel.

Fig. 3.7 illustrates the cyclic I-Vs corresponding to Ni. In spite of carefully stripping the protective PR coating immediately before experimentation, the I-V cycles illustrate that the Ni surface was anything but conducting, compared to other metals investigated previously. A contact resistance of approximately 1×10^{11} Ω as a starting point could only indicate rapid ambient oxidation on the surface of Ni as tested. From Fig. 3.12(d), the overall trend indicates that the contact resistance remained in the high 10^{11}-10^{12} Ω regime, while a conspicuous drop after about 50,000 cycles resulted in a decline in the contact resistance to the 10^{10} Ω - 10^{11} Ω regime. Considering the fact that the contact resistance always remained relatively high, it may be concluded that Ni was poorly conducting throughout the entire experiment.

The graphs in Fig. 3.8 correspond to cyclic I-Vs carried out on Chromium. It appears that Cr was also affected by rapid ambient oxidation, resulting in poor

conductivity, similar to, if not worse than, that seen on Ni. The contact resistance began at around the $5x10^{12}$ Ω regime, and ended in the $5x10^{11}$ Ω regime – a small decrease in contact resistance which may be anomalous. From Fig. 3.3(e), it is seen that there were histrionics along the way as the cycles progressed, but all of these were in the high ohmic resistance (poorly conducting) regime and could all be attributed to many nonlinear effects that correspond to deterioration of contacts, as discussed previously.

The next metal investigated was Titanium and the results are compiled in Fig. 3.9. By far, Ti showed the most interesting results in terms of contact resistance change and also the trend of the change over the number of I-V cycles. It appears that Ti maintained a consistent ohmic contact throughout the testing period, illustrating a contact resistance in the 10^7Ω regime during the entire experimentation period. The change in the contact resistance from the moment that testing began until the very last cycle was approximately 1 order of magnitude. From Fig. 3.3(f), it is seen that this change is negative; indicating that the contact resistance *improved* as a function of time and the regime of operation was in the closed contact zone, entirely unlike that seen in Cr or Ni. This result is very surprising as all other metals have shown catastrophically deteriorating contact resistances as a function of operating cycles. One of the explanations could be favorably directed towards the conductivity properties of TiO_2, and possibly, its differing lattice structure compared to the Cr coating on the AFM tip.

Copper was investigated next and Fig. 3.10 is a compilation of the cyclic I-Vs obtained. It is seen that Cu has a very small initial contact resistance comparable to Pt and W. From the onset of experimentation, Cu has maintained consistent ohmic characteristic for the longest period of time (approximately 30,000 cycles), after which

contact deterioration effects became visible as the contact resistance began to increase. This change was fairly dramatic and abrupt, as seen by the trend on Fig. 3.3(g). The change in resistance was approximately 6 orders of magnitude.

The last metal investigated was Aluminum and the results are compiled in Fig. 3.11. Al showed a trend seen before with metals such as Ir, Pt, and W. This is interesting as the conductivity of Al is known to be high; however, its Young's modulus is far lower compared to the other metals listed. Al maintained consistent ohmic behavior until the first few 1000s of cycles with the initial contact resistance being in the $10^7\Omega$ regime. Interestingly, from Fig. 3.3(h), it is seen that the contact resistance decreased within the first 100s of cycles, indicating clearing of the native Al_2O_3 followed by cyclic deterioration effects, rendering the contact to climb to high contact resistance values, stabilizing at the 10^{12} Ω regime. The overall change in contact resistance from best case to worst case was approximately 6 orders of magnitude.

The final material investigated was layers of graphite, which is a nonmetal known to have a highly planar 2-dimensional structure. The I-Vs on these layers of graphite are illustrated in Fig. 3.12. It is clearly seen from Fig. 3.3(i) that graphite has the most consistent (ohmic) I-V performance compared to all the other metals. Over the duration of its I-V cycling up to 100,000 cycles, the graphs show the shape of the I-Vs were mostly similar throughout, until the final stage. In addition to its being a nonmetal, graphite is known to have a 2-dimensional planar structure and severe resistance to chemical reaction (oxidation, hydration, etc.), as a result of which, graphite is greatly immune to a decline in contact efficiency. From Fig. 3.12(i), it is seen that graphite

maintains contact resistance at $10^7\Omega$ consistently up to 100,000 cycles and this was unique to graphite.

After the electrical measurements on the metals were obtained, contact mode AFM studies and SEM imaging was carried out on each metal sample. The results of these studies are illustrated in Fig. 3.13(a)-(h). It is clear that a period of repeated cycling over a single point exposes the sample to adverse conditions that causes physical restructuring. Some of these are due to surface pitting, fatigue, asperity generation, charge migration, stiction, and micro-welding. Other failure modes include re-arrangements of metal atoms near the surface and possible oxidation in the contact region. Some instances of "clearing" near the contact region from the thin-film metal are also visible.

3.3.2. Adhesion Force Measurement

After carrying out force vs. displacement experiments on the metals, the results of the measurements were compiled into Table 3.1. The table also compiles some relevant material properties of the materials under investigation. Fig. 3.14 compiles data from Table 3.1 into a graphical comparison for convenience.

The following deductions can be made from Fig. 3.14: it appears that Cu clearly shows the highest surface adhesion force (~225nN), while W (~18nN) and Pt (~26nN) are close competitors for the lowest. The following list can summarize the sequence of average adhesion forces (in ascending order): W (18nN), Pt (25nN), Graphite (65nN), Ni (65nN), Cr (62nN), Ti (79nN), Al (100nN), Ir (115nN), and Cu (225nN).

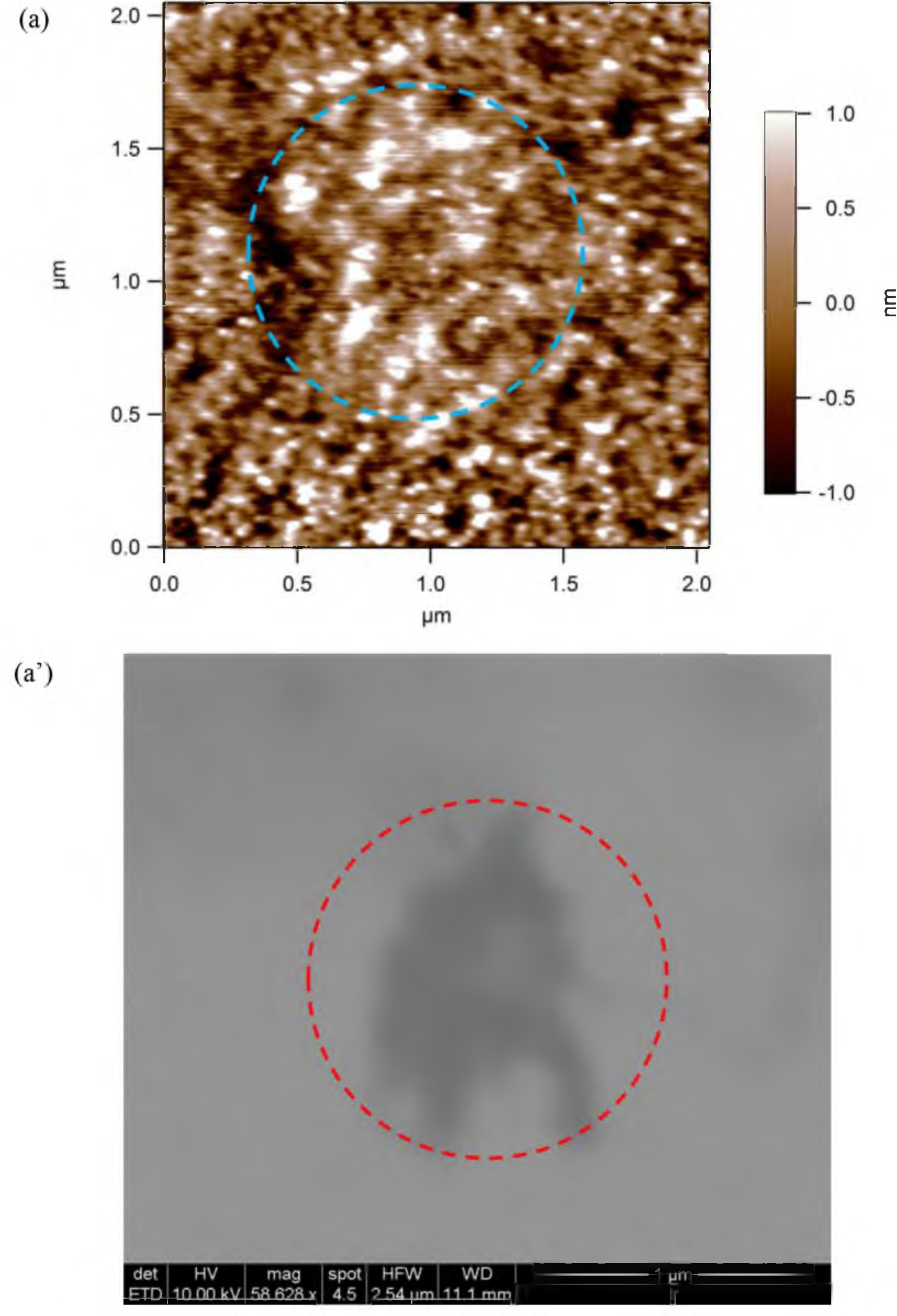
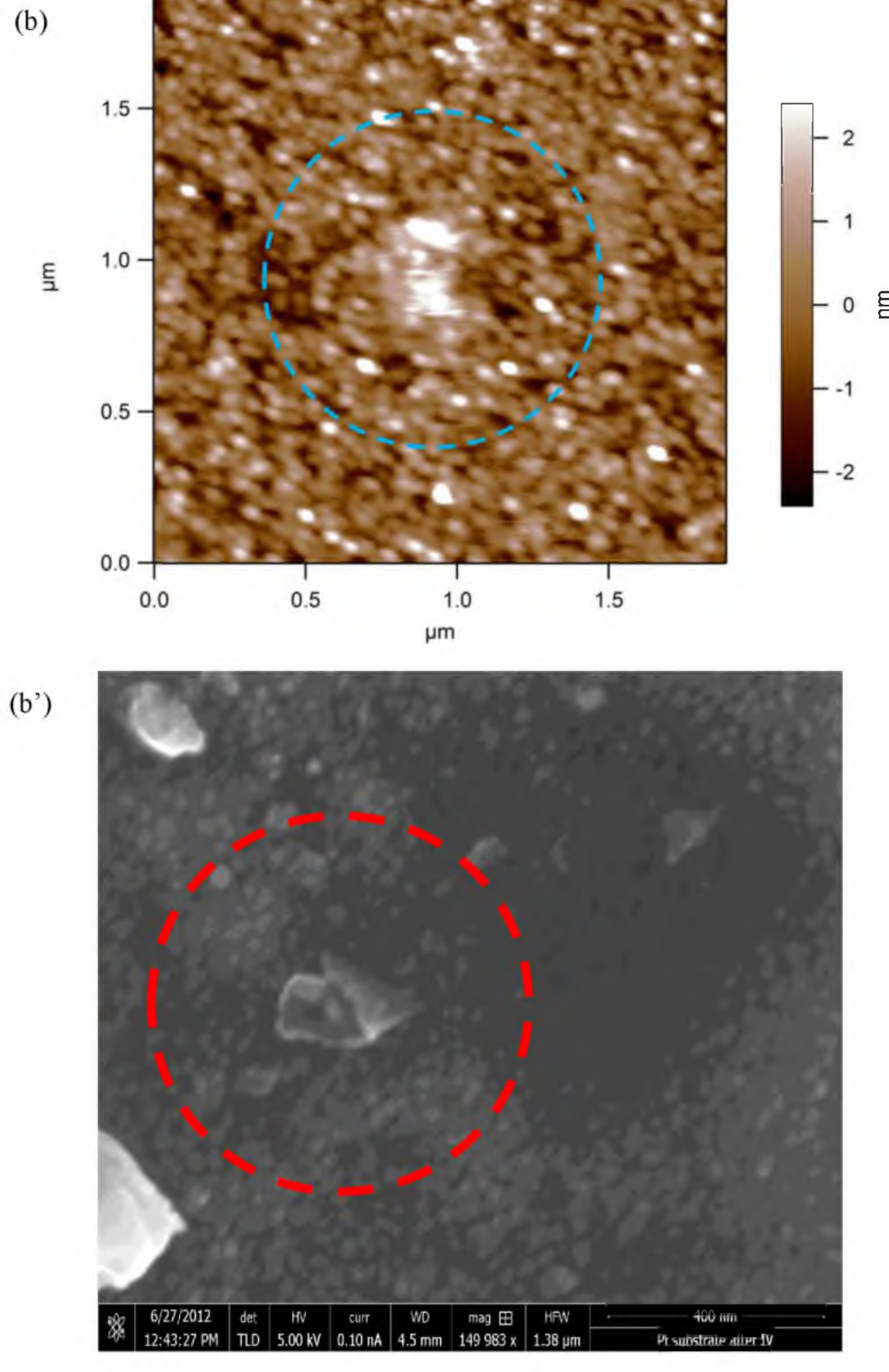


Figure 3.13: AFM surface scans and SEM imaging over region where cyclic I-Vs where carried out for (a) Iridium, (b) Platinum (c) Tungsten, (d) Nickel, (e) Chromium, (f) Titanium, (g) Copper and (h) Aluminum and (i) Graphite (AFM only)



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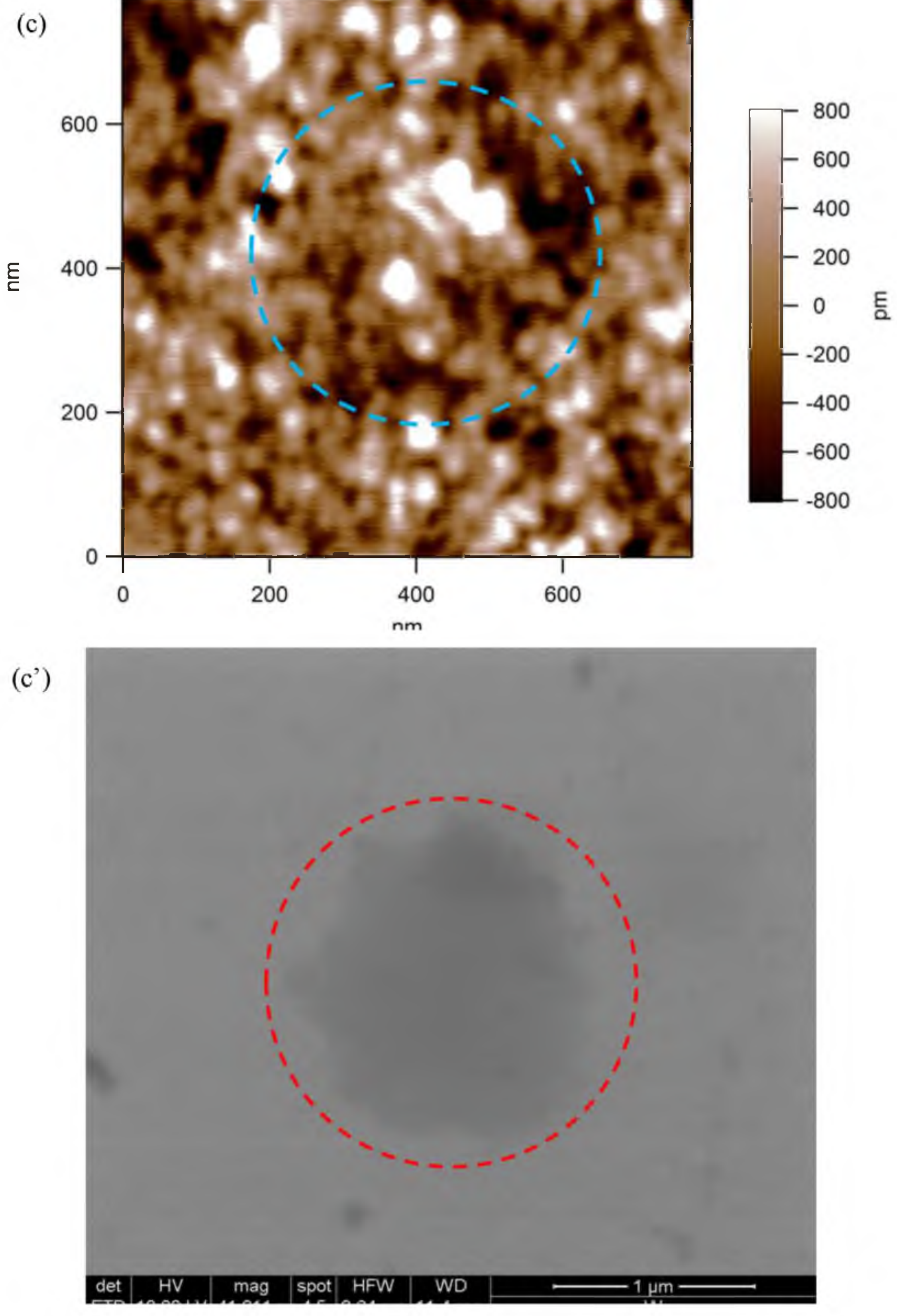

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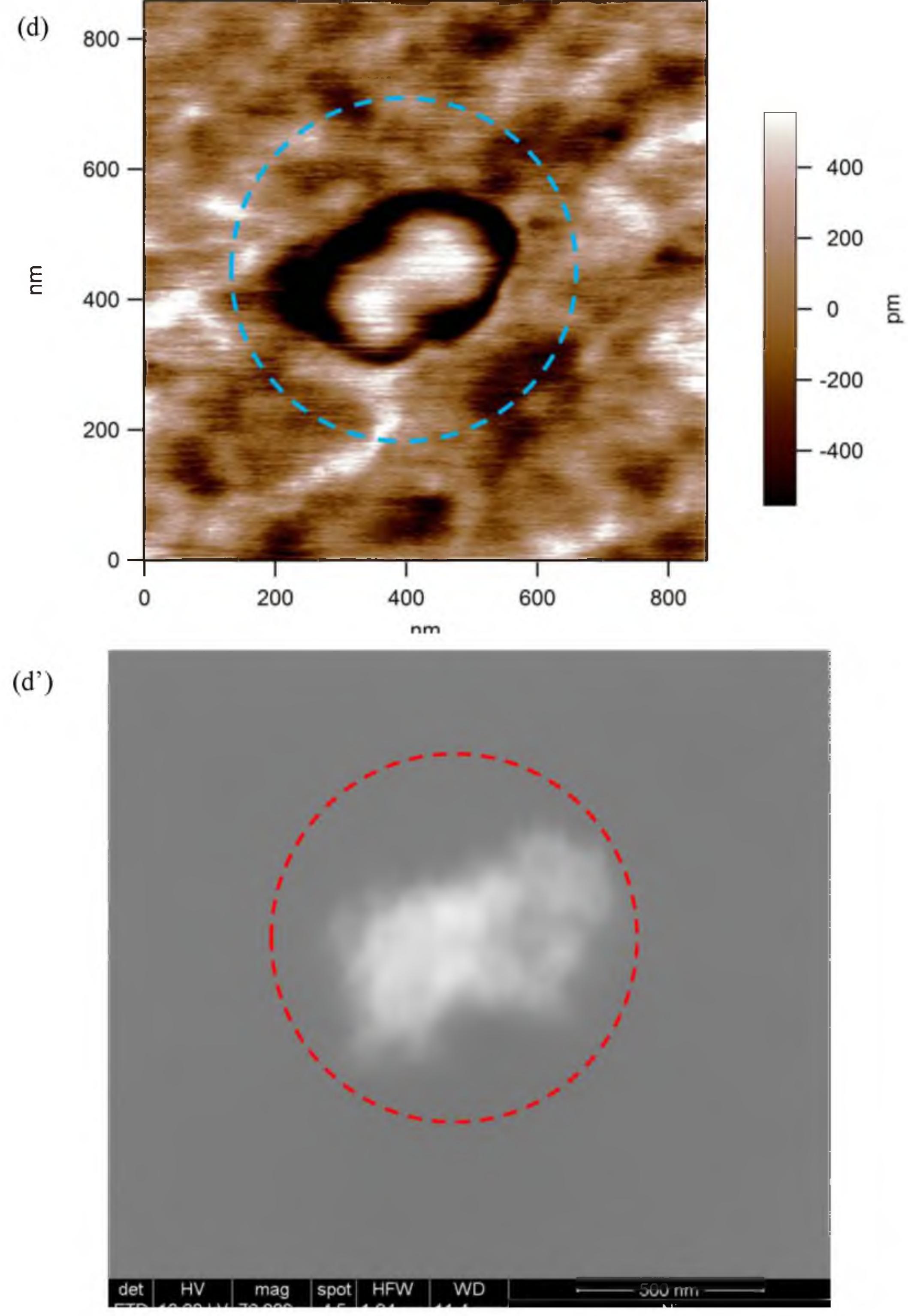

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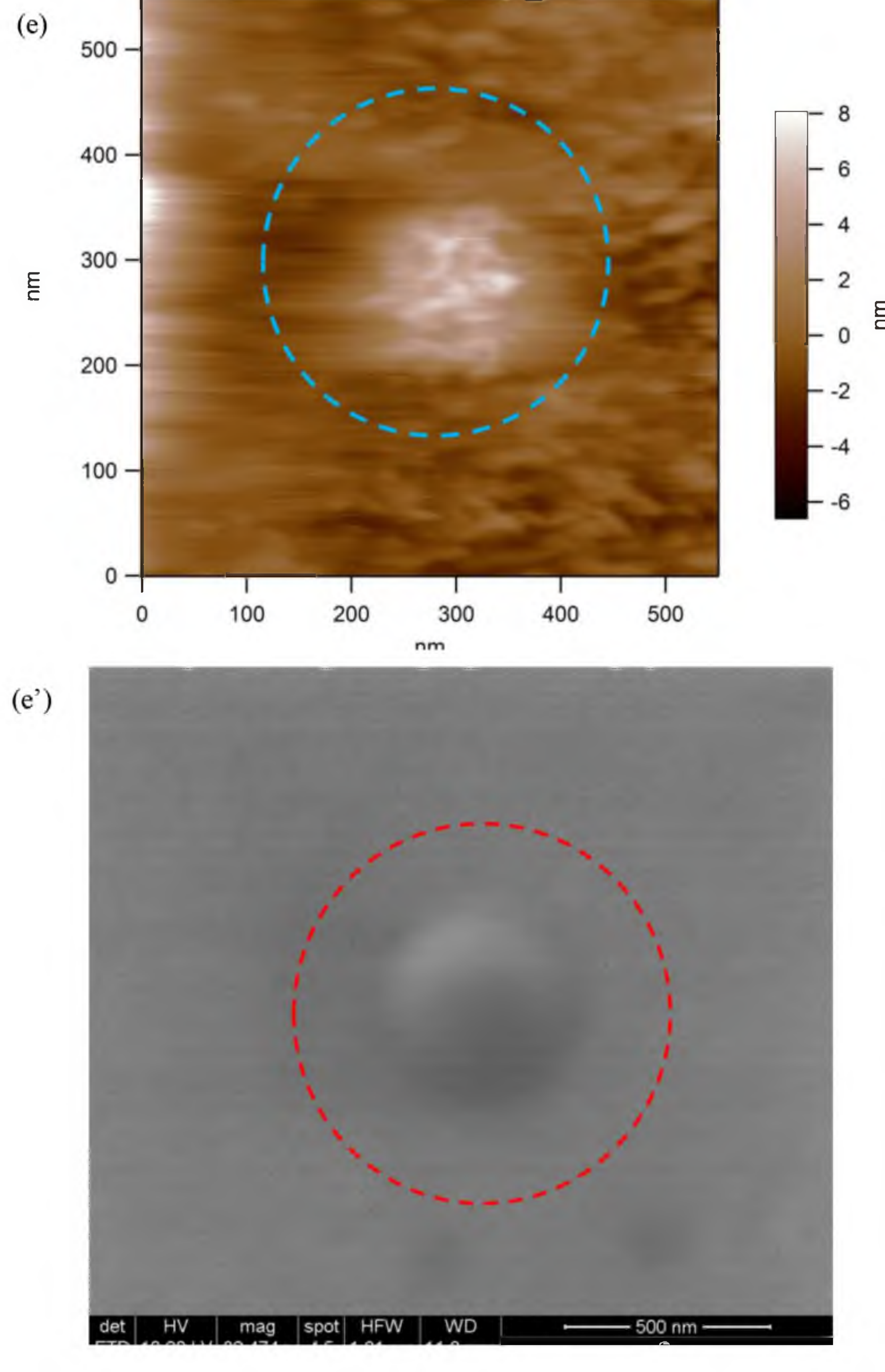

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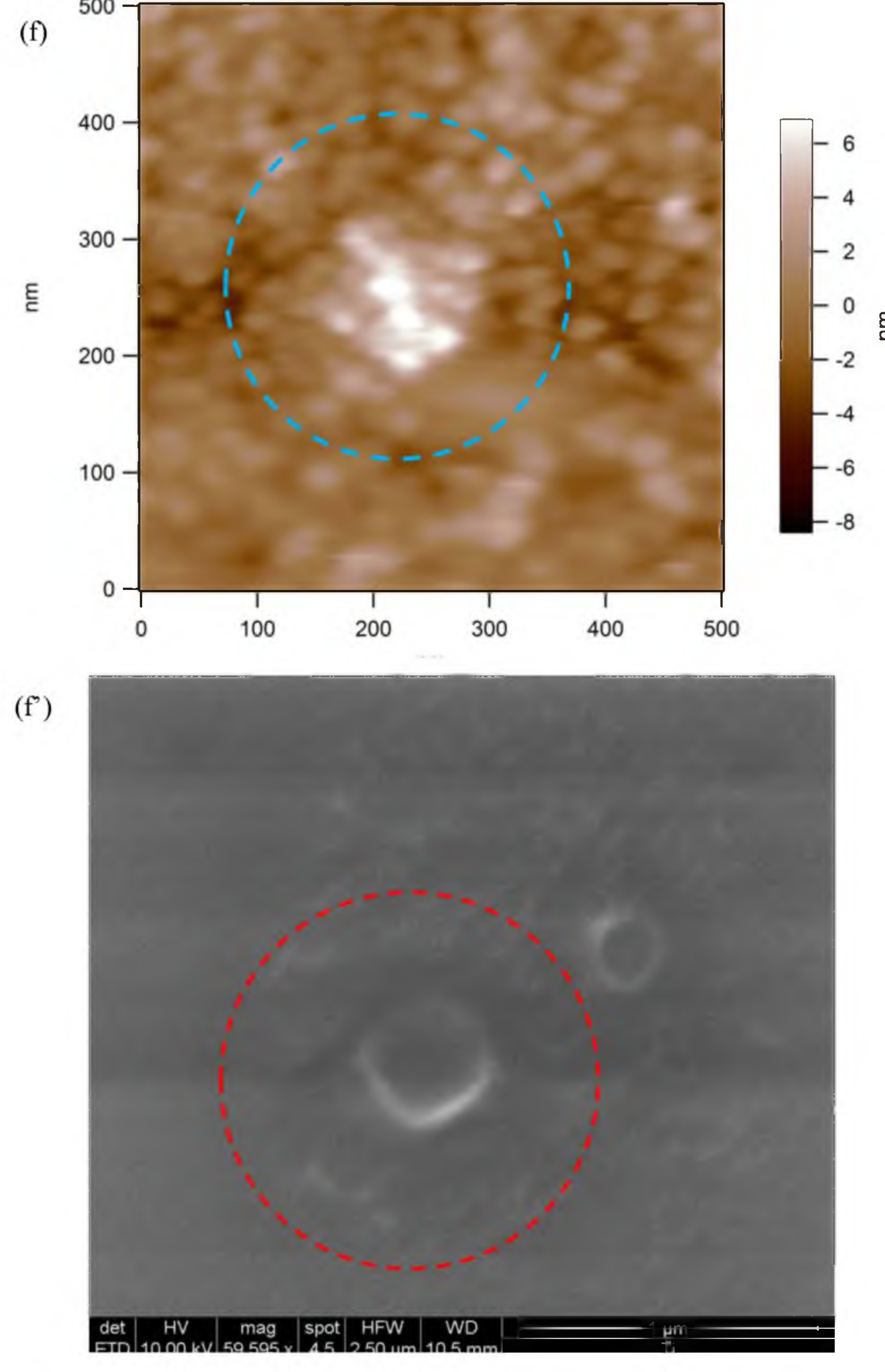

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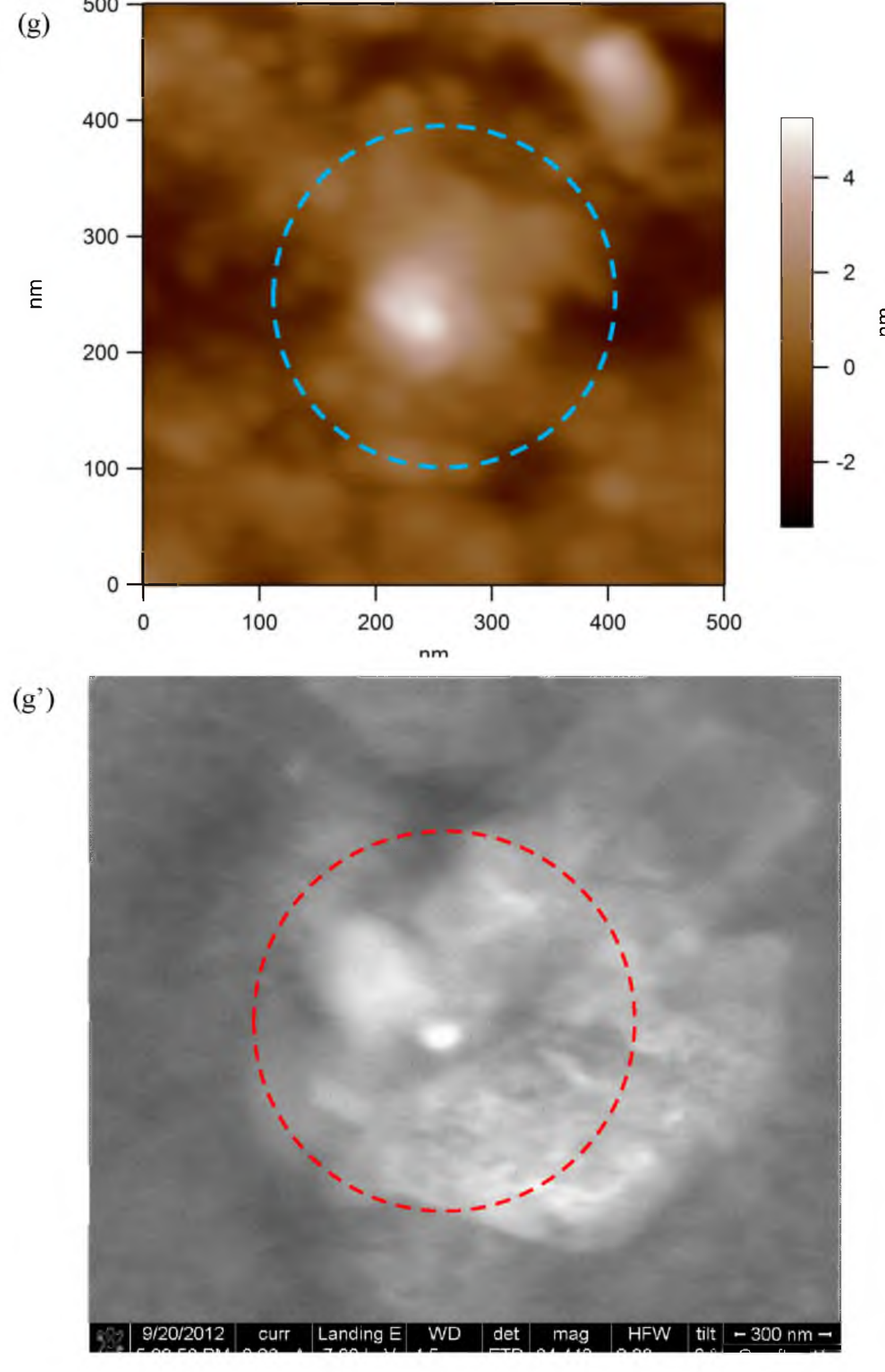

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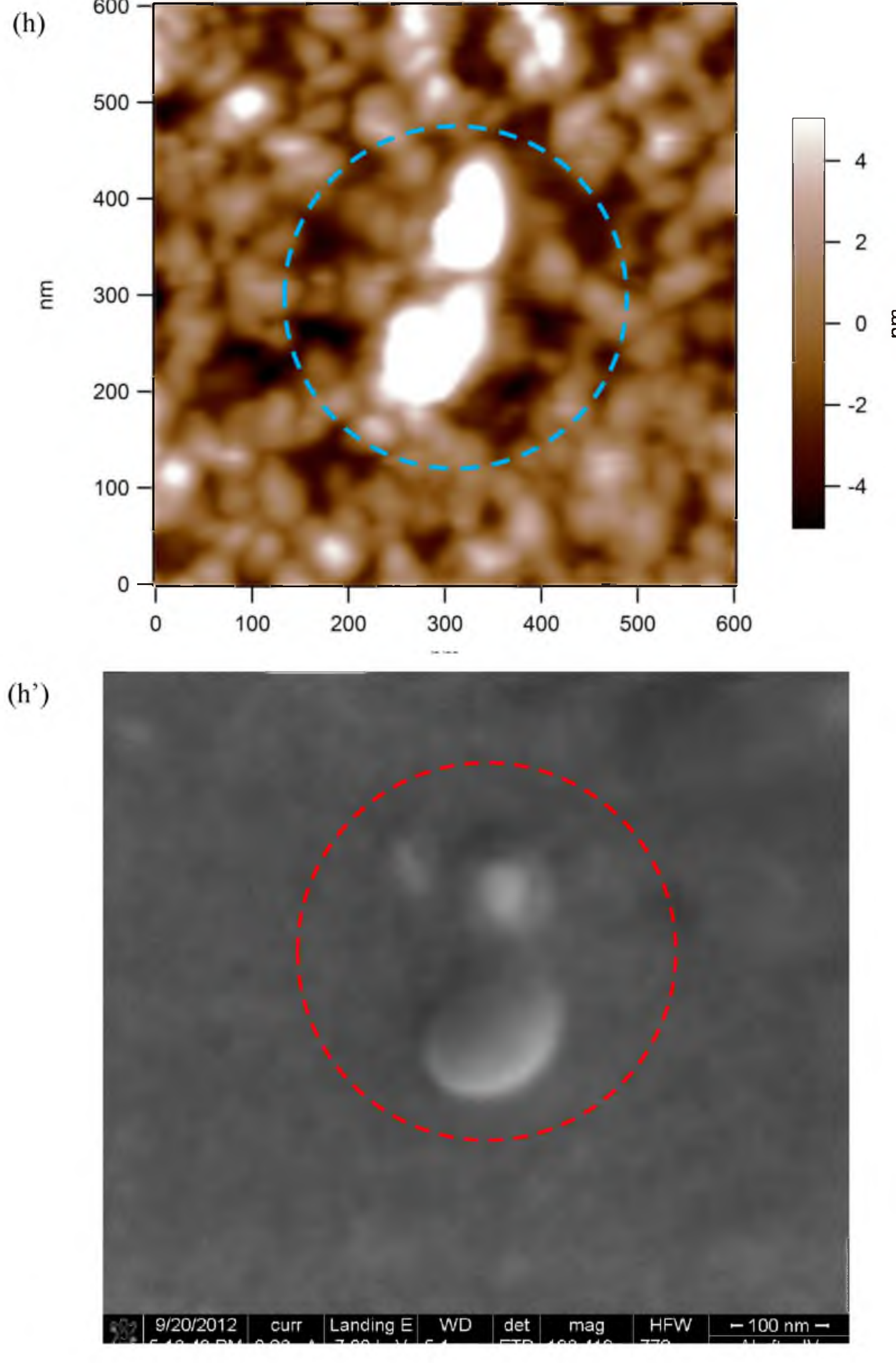

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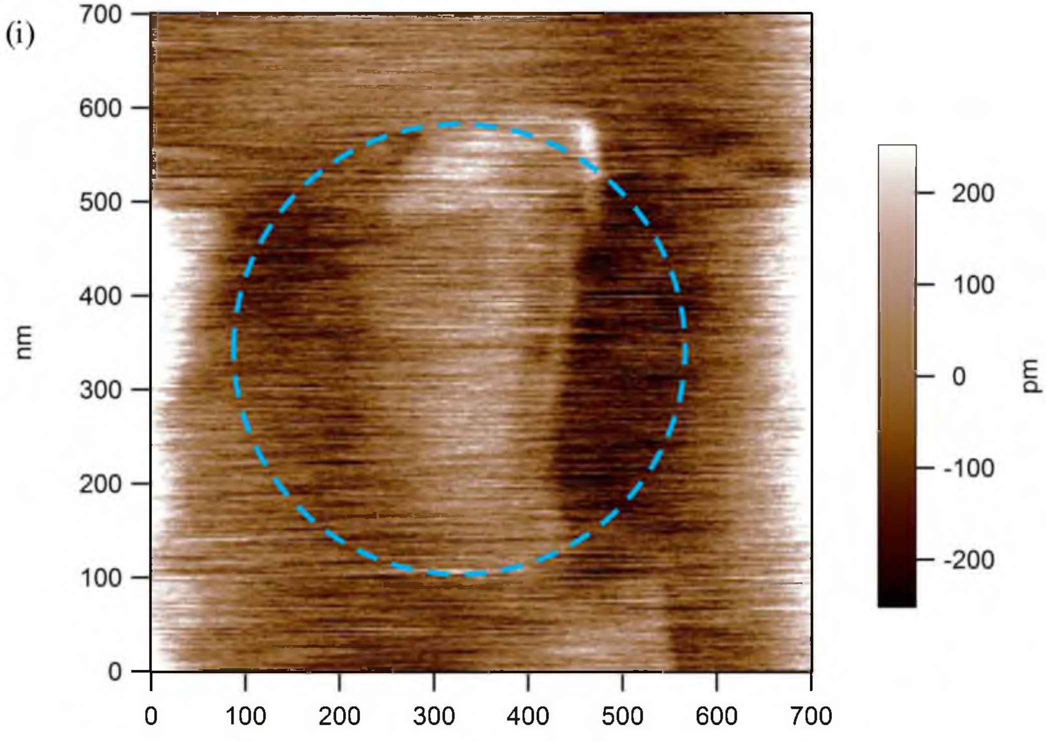

Figure 3.13: Continued

Table 3.1: Material properties of tested substrates

Material	Conductivity % IACS	Young's Modulus Gpa	Density g/cm^3	Melting Temperature °C	Hardness (mohs)	Adhesion force nN	Crystal Structure
Ir	36.6 [21]	516.0 [21]	22.56 [22]	2443[21]	6.5	115	FCC
Pt	16.0 [23]	146.8 [23]	21.45 [23]	1769 [23]	4-4.5	26	FCC
W	30.0 [23]	344.7 [23]	19.30 [23]	3422 [23]	7.5	18	BCC
Ni	25.2 [24]	206.8 [23]	8.90 [23]	1455 [23]	4.0	65	FCC
Cr	13.0 [25]	248.0 [23]	7.19 [23]	1860 [23]	8.5	62	BCC
Ti	13.9 [23]	100-145 [26]	4.51 [27]	1677 [28]	6.0	79	HEX
Cu	103.0 [23]	11.0 [29]	8.90 [29]	1080 [29]	3.0	225	FCC
Al	64.95 [23]	70.0 [29]	2.70 [29]	660 [29]	2.75	100	FCC
Graphite	-	8-15	2.15	3642 (sublimation)	1-2	65	HEX

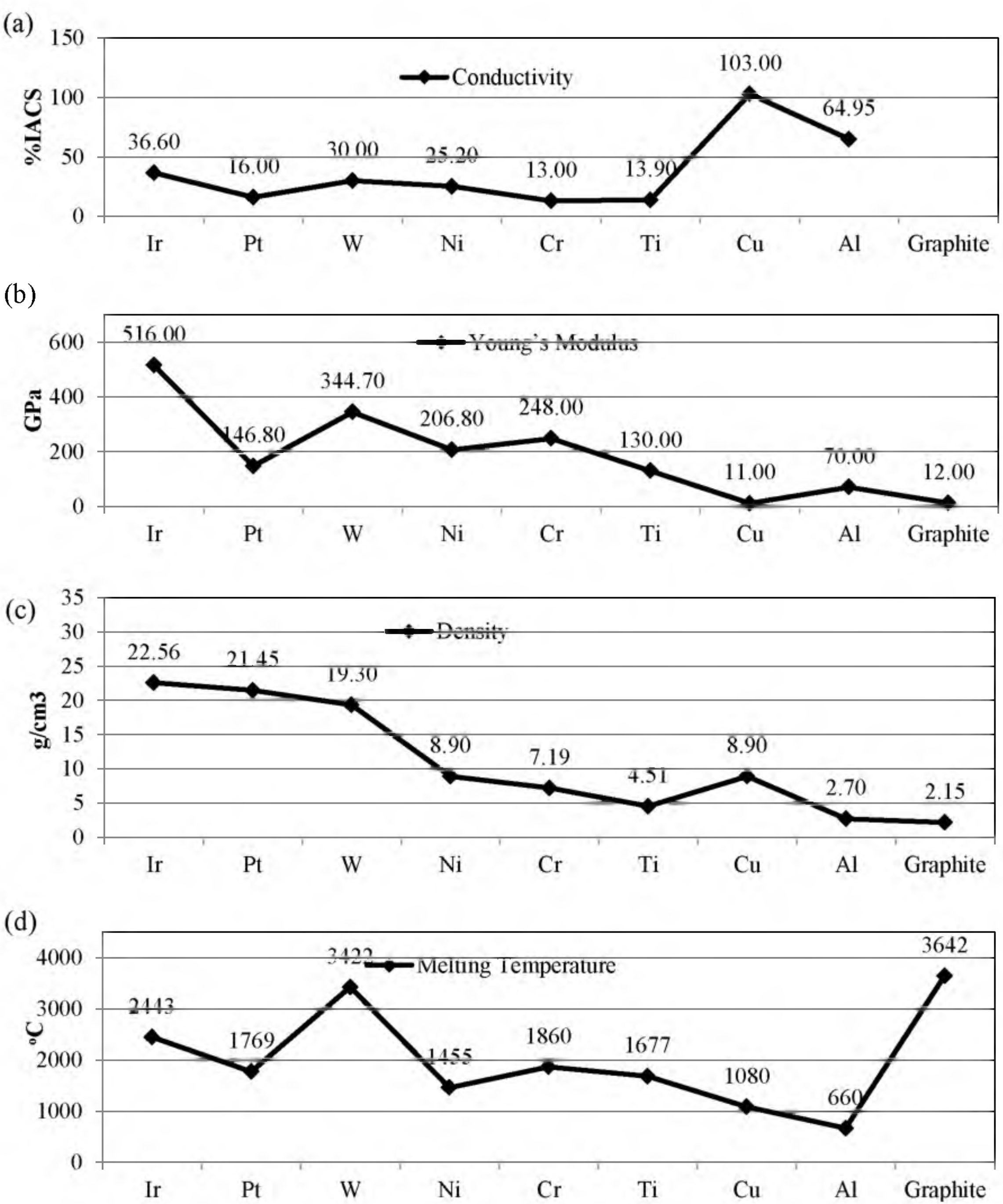

Figure 3.14: Plots comparing material properties data from Table 1. (a) Conductivity, (b) Young's Modulus (c) Density, (d) Melting Temperature (e) Hardness, and (f) Adhesion Force.

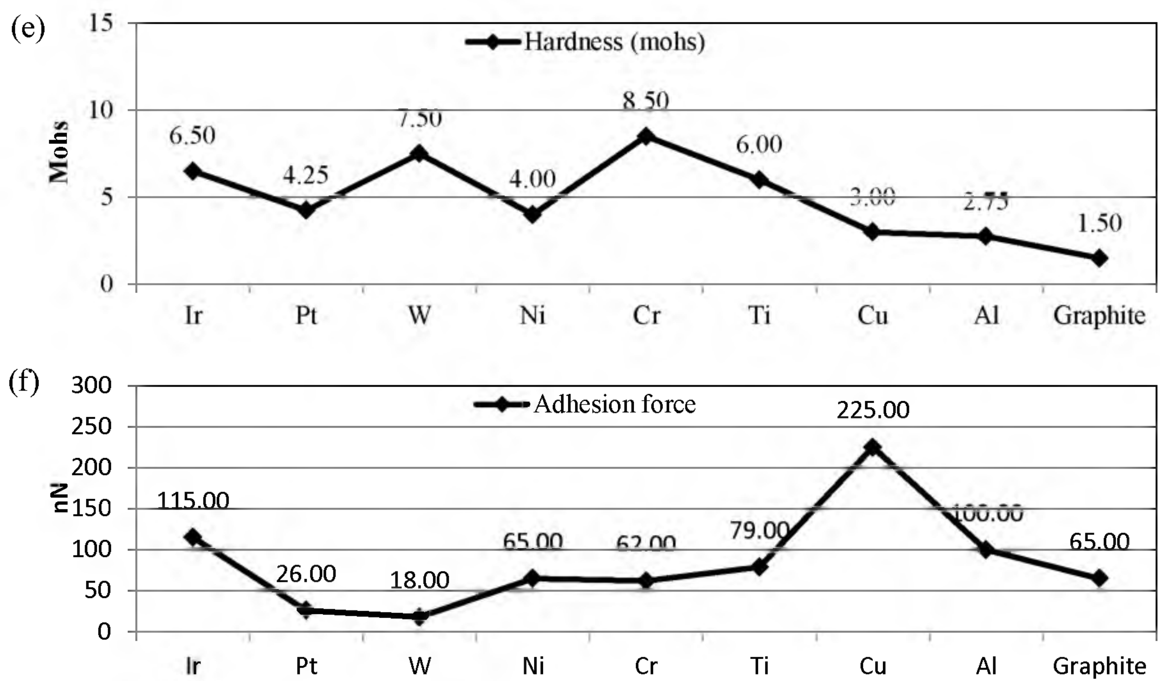

Figure 3.14: Continued.:

Both W and Pt have low adhesion forces while their (initial) contact resistances and overall evolution of contact deterioration were very similar (Fig. 3.3). Although Ir also falls in this category in terms of similarity, it has a much higher adhesion force and this may be attributable to its significantly higher Young's modulus (Table 3.1). One reason that W has the lowest adhesion force may be due to its very high melting point. Interestingly, Ni and Cr show great similarity in adhesion force values as well as in (poor) initial contact resistances. Ti, with its best I-V and contact resistance performance, is midway between the least and most adhesion force measurement value. The same can be said about its other material properties such as Young's modulus and melting temperature. Nevertheless, it does have the second lowest density amongst the eight metals.

3.4. Summary

This chapter discussed the details of an investigation on the evolution of contact resistance (R_c) in eight disparate metals and one nonmetal commonly used as electrode materials in MEMS switches, over 100,000 cycles. A contact-mode atomic force microscope connected to a current versus voltage (I-V) measurement system was used and successive I-V measurements between a Cr-coated AFM conducting tip and Ir, Pt, W, Ni, Cr, Ti, Cu or Al thin-film materials on silicon nitride-coated silicon and graphite in a nitrogen ambient were carried out. The contact regions were subsequently imaged using SEM and contact-mode AFM to correlate changes that occurred in the surface morphology, roughness, and R_c. Adhesion forces between the conducting AFM tip and the thin-film material substrates were also measured.

It appears that high Young's modulus, high melting point, and high hardness metals such as Ir, Pt, W, and Ti illustrate the best cycling I-V characteristics in terms of initial contact resistances while having the lowest adhesion forces. Metals such as Ni and Cr are amongst the worst performers in I-V cycling. Ti has material properties comparable to Ni and Cr, but has a fantastic I-V characteristic that actually maintained a relatively high conductivity throughout cycling and also showed a slight improvement in contact resistance over increasing cycles of operation. This may be attributable to the conducting oxide that forms as the surface is stressed. Cu and Al, both, have very high conductivities; as a result, both had very low initial contact resistances up to a certain point. Beyond that, Cu illustrated abrupt failure, while Al gradually developed a state of nonconductivity (due to formation of its oxide). Graphite was the only nonmetal tested and it illustrated very reliable and efficient contact performance compared to other materials. These were attributable to its highly planar 2D structure along with added resistance to ambient oxidation and furthermore, the significant lattice dissimilarity between the Cr-coated AFM tip and the graphite substrate. This dissimilarity also existed in Ti and may have also contributed to its high contact efficiency.

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CHAPTER 4

FABRICATION PROCESS

Fabrication of the devices shown in Fig 4.1 was carried out at the University of Utah Nanofabrication facility. The facility encompasses a class 100/1000/10,000 cleanroom, packaging, and testing areas. In addition to conventional nanofab tools such as deposition, photolithography (including mask-making), and etch equipment, the Utah Nanofab comprises specialized tools such as ALD, XeF_2 etch, LPCVD (TEOS, LTO, PSG), DRIE, and CMP. The following sections provide an overview of the process flow required to fabricate the MEMS-based XOR and AND gates.

4.1. Fabrication of Single-Device XOR and AND Gates

4.1.1. Overview

The devices, shown in 3D rendering in Fig. 4.1, were fabricated as summarized in the process flow given in Fig. 4.2. A 4" silicon wafer was insulated with 100nm LPCVD stoichiometric silicon nitride deposited at 780°C. Isolated square "wells" were patterned into this insulating nitride layer all the way through to the silicon substrate. The MEMS switches were fabricated around this well. The wells were next filled with thermal SiO_2 at 950°C (by timing the process precisely) up to the brim of the silicon nitride well.

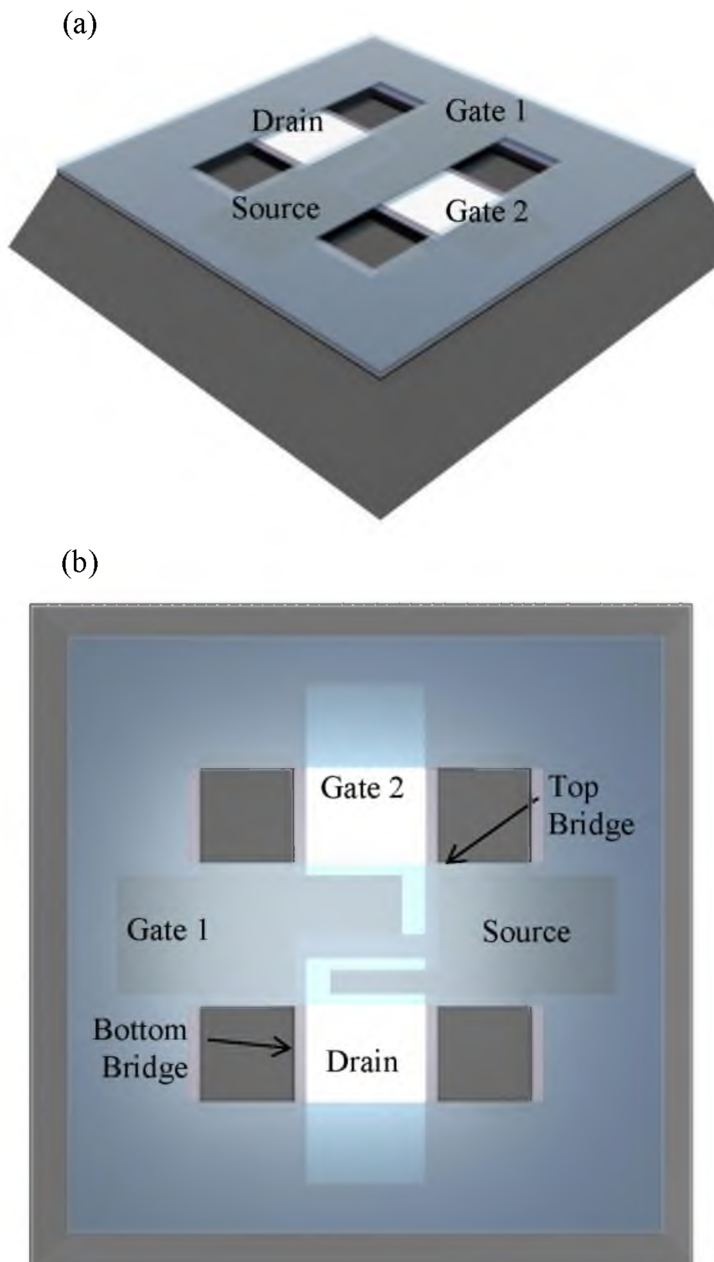


Figure 4.1: Cross-bridge platform for MEMS (XOR) logic (a) 3D isometric render and (b) top view.

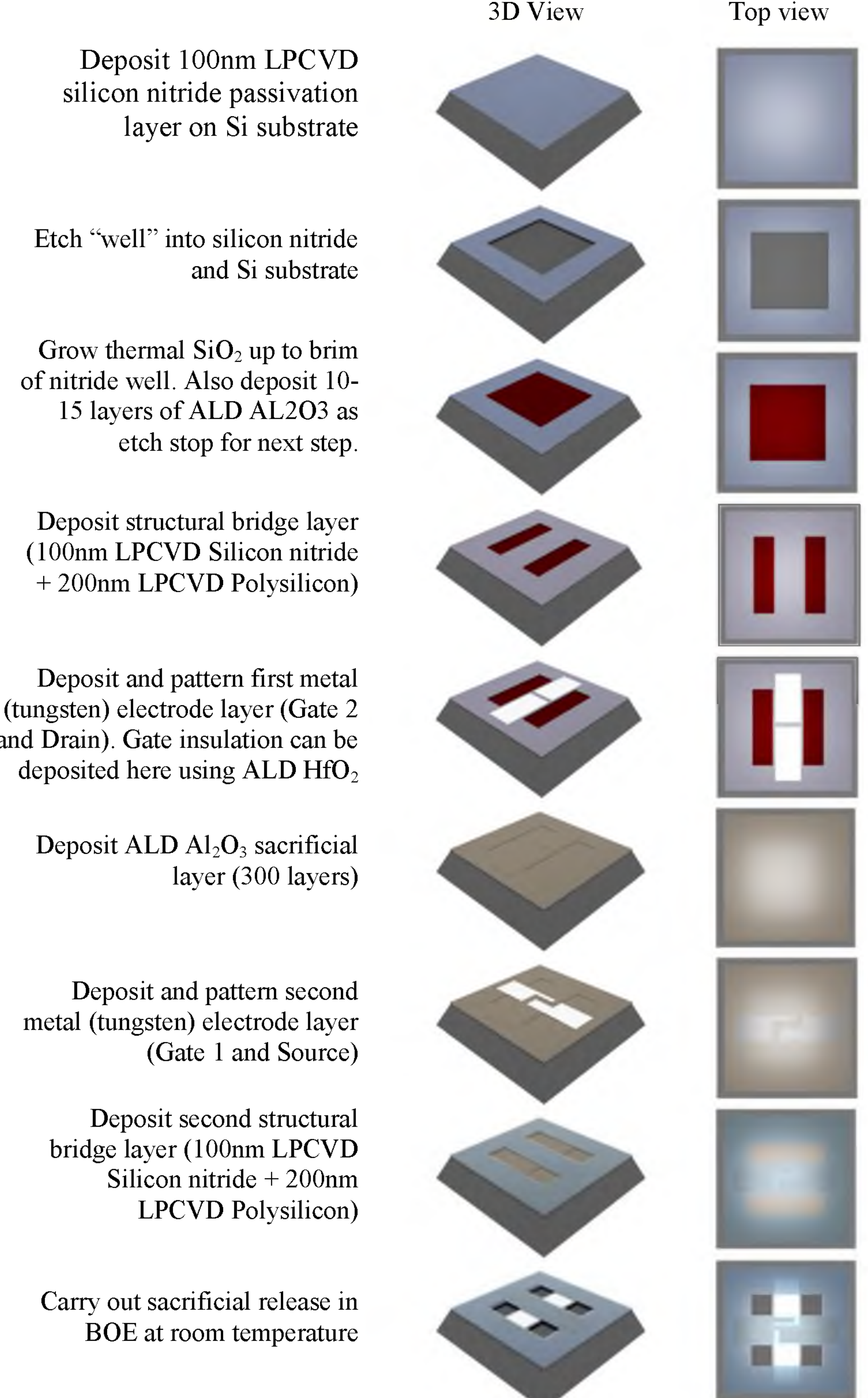
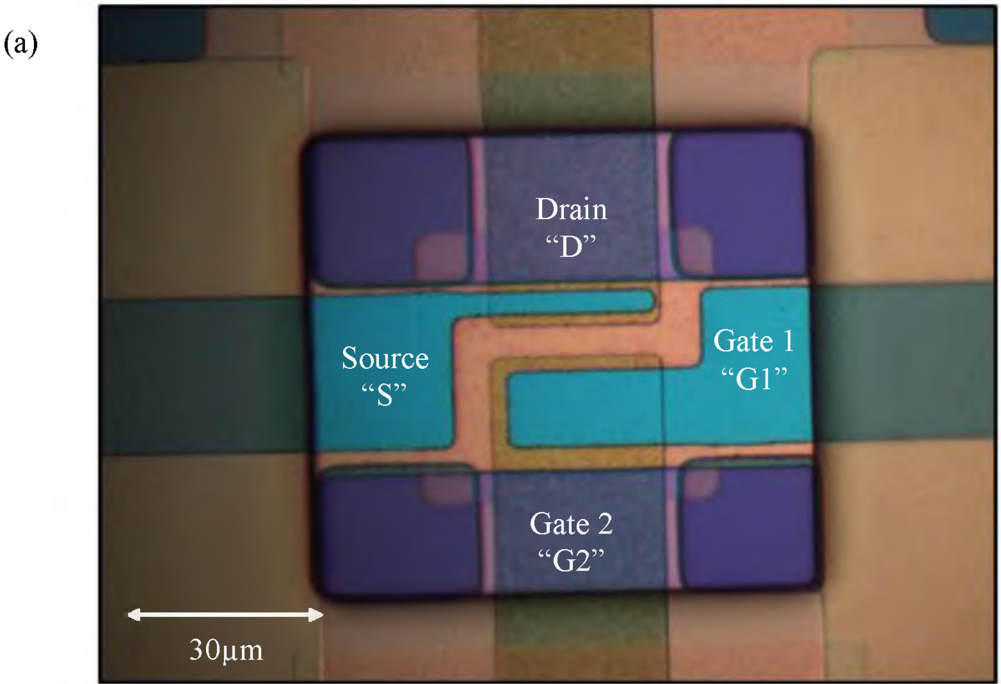


Figure 4.2: Fabrication process flow for XOR and AND gates. The process flow is the same for other gates, such as AND.

Next, the first bridge layer of LPCVD nitride (100nm) and LPCVD polysilicon (200nm) was deposited and patterned to form the first structural bridge. This bridge was designed to support gate 2 and drain electrodes. Following this, tungsten was sputtered and patterned to form the electrodes (gate 2 and drain) on the first nitride bridge. Next, the wafer was capped with 300 layers (~0.1 nm/layer) of thermal Al_2O_3 deposited using a Fiji Atomic Layer Deposition (ALD) system. This also served as the sacrificial gap between bottom and top electrode-bridges. This was followed by the second tungsten metallization (via sputtering), which was patterned to form electrodes (Gate 1 and Source) that reside under the second structural bridge. Thereafter, the second silicon nitride and polysilicon structural bridge was deposited and patterned to define the top bridge. Tungsten was patterned using 30% H_2O_2 at room temperature, silicon nitride and polysilicon was pattered using a dry etch recipe comprised of CF_4/O_2 at 200W, resulting in clean etch of the structural layers.

The ALD Al_2O_3 layers acted as an effective etch stop for this dry etch recipe while patterning the second bridge. Details of these are provided in the following section. At this point, the ALD layers were sacrificially etched in BOE etchant at room temperature to "free" the two bridges from each other and from the substrate. Upon release, the SiO_2-filled well was also etched away, enabling the silicon substrate to be used as a gate in "MOSFET"-like operation of the device as well as to use field effect to separate the two bridges if needed. A variant of this design was to pattern a layer of tungsten electrodes prior to the first silicon nitride bridge. Both variants served the same purpose; however, the latter is not further discussed here. Optical images of the final devices are given in Fig. 4.3.

(a)



(b)

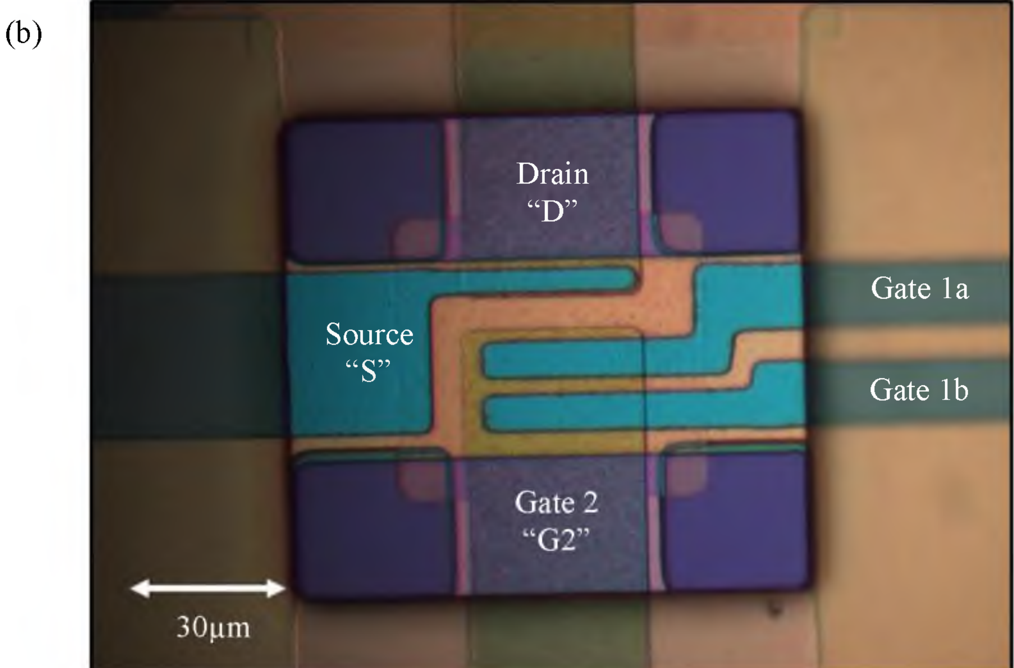


Figure 4.3: Optical images of fabricated a) XOR gate. G1 and G2 are gate electrodes. S and D represent Source/Drain. b) AND gate. S-D will connect only if gate 1a and 1b are high at the same time.

In addition, it must be acknowledged that the need for gate insulators is recognized although absent in this prototype described here. Dielectric materials such as ALD HfO_2 are strongly recommended here as they are excellent insulators and also their uniformity can be reliably controlled when deposited via ALD tools. The following section provides further details on fabrication and elaborates on each step.

4.2. Fabrication Process Details

This section details the device dimensions, process steps, and recipes required to fabricate the MEMS-based XOR and AND logic gates. The section begins with providing the blueprints of electrodes (configuration and dimensions) for each logic gate and follows on with the fabrication process. Each step, such as, Silicon nitride deposition, tungsten sputtering, wet and dry etch, sacrificial release, etc. with their process parameters and documented results is provided. Also included are images of the wafer at each processing step. The Masks were designed using LEdit version 12 and were fabricated using the Electromask MM250 Pattern Generation tool in the University of Utah's Nanofab.

4.2.1. Device Dimensions and Layout/Design

The device footprint was designed to be 30µm x 30µm, as shown in Fig. 4.4. Both XOR and AND gate electrode patterns were conveniently packaged into this platform. Furthermore, the dimensions of each electrode are specified in Figs. 4.5 and 4.6, for XOR and AND gate configurations, respectively.

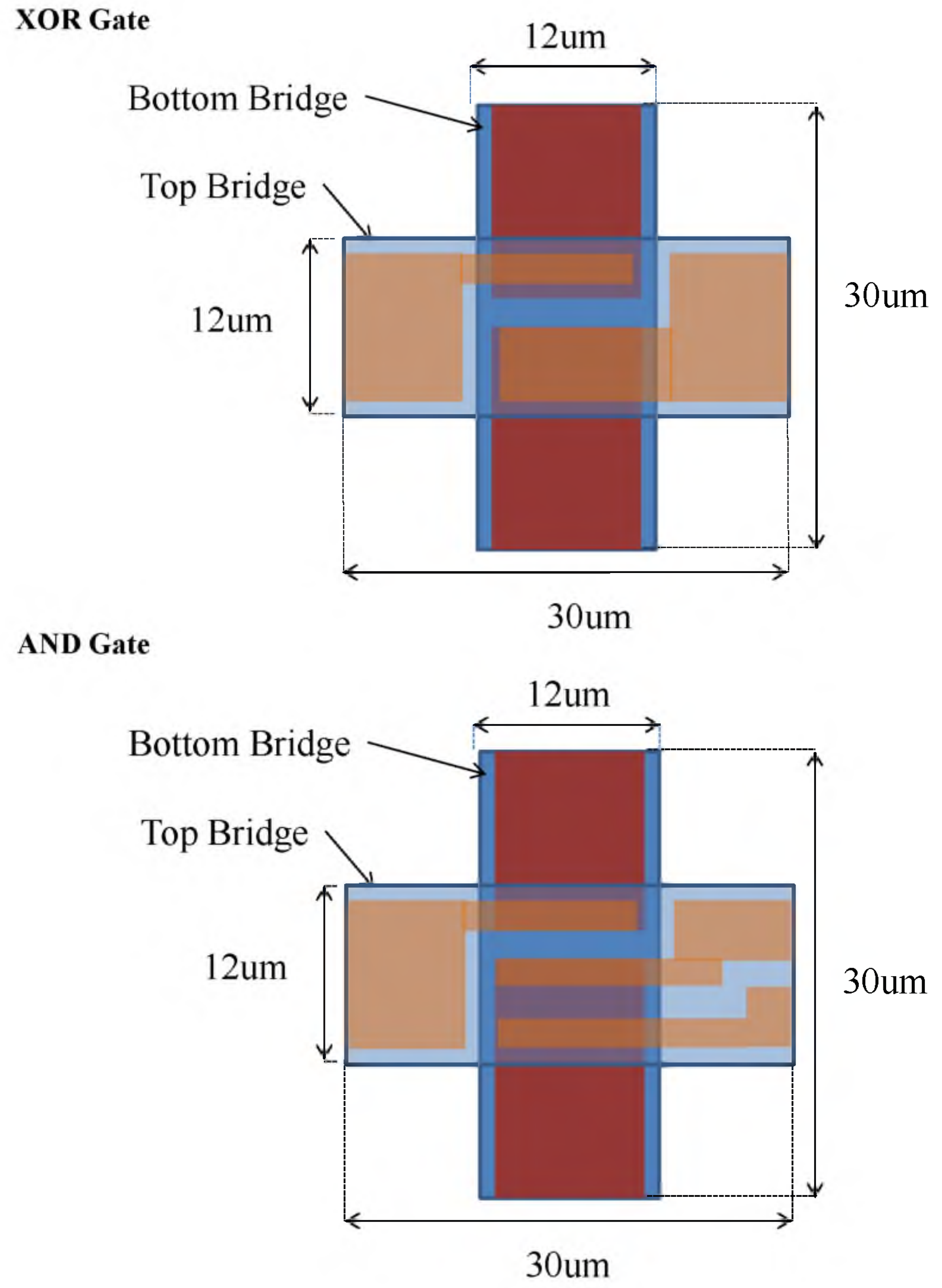


Figure 4.4: Cross-bridge platform dimensions. XOR and AND gate layouts are shown.

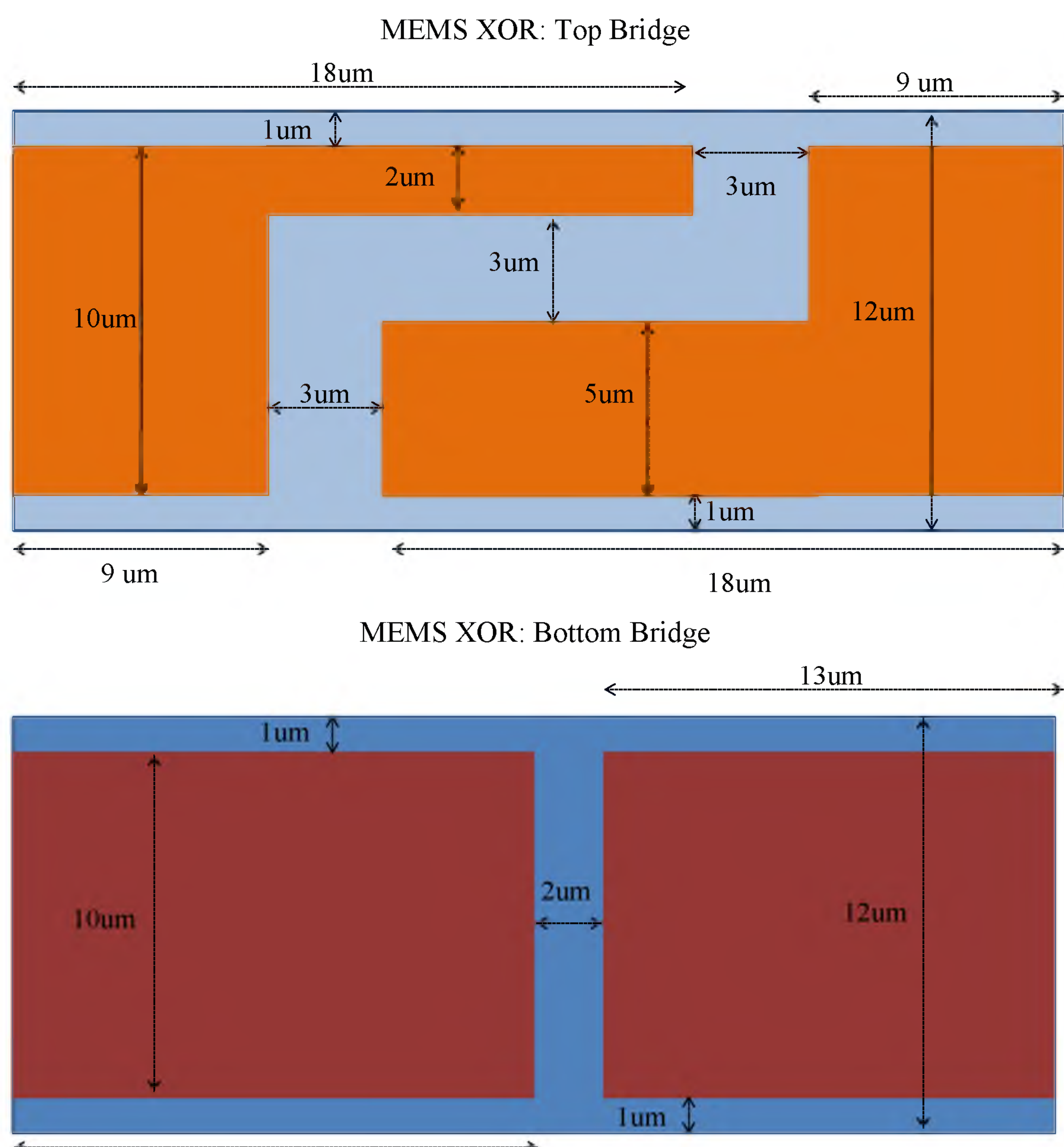


Figure 4.5: MEMS XOR gate Top and Bottom bridge layout and dimensions.

MEMS AND: Top Bridge

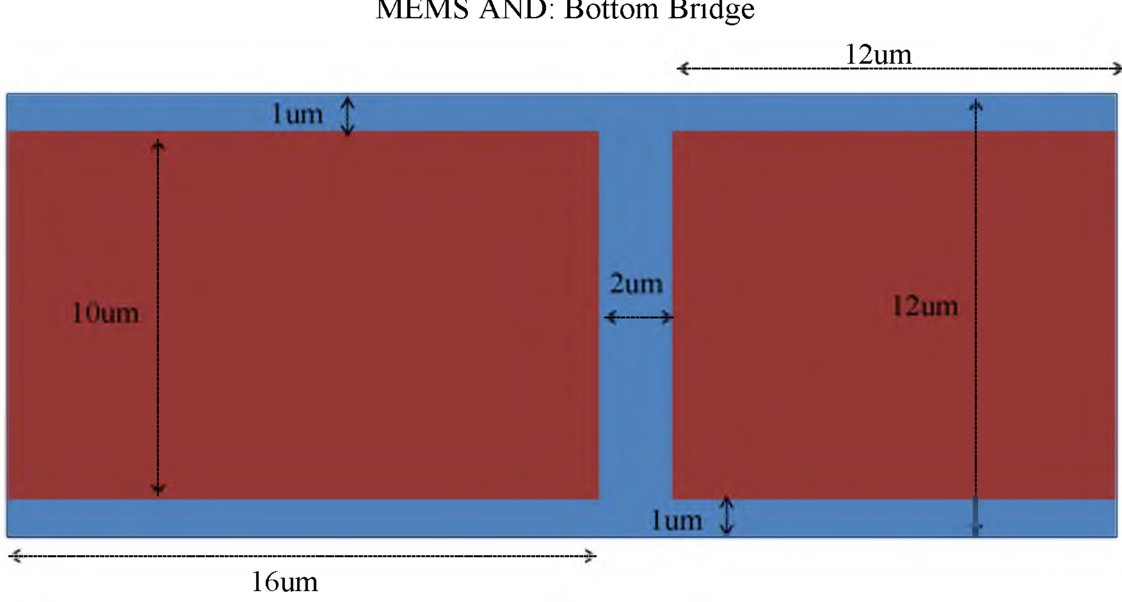


Figure 4.6: MEMS AND gate Top and Bottom bridge layout and dimensions.

4.2.2. Deposition of Silicon Nitride Passivation Layer

A single-side-polished, 4”, conducting (n-type) Si-110 wafer was used as the starting substrate onto which 100nm stoichiometric Silicon Nitride was deposited. This was done using the Canary LPCVD Nitride Furnace inside the Nanofab. The preloaded recipe was timed to run for 25 minutes, which was programmed as shown below. The resulting nitride deposited had reliable uniformity (<5% variation) at ~110nm. Fig. 4.7 shows the wafer boat after deposition of 100nm LPCVD silicon nitride, and Fig. 4.8 illustrates a single wafer from the center of the boat emphasizing the uniformity.

Temperature	:	780 C
Time	:	25min
NH3 flow rate	:	80 sccm
DCS flow rate	:	20 sccm
Controller pressure	:	430-440 mTorr

Figure 4.7: Silicon Nitride wafers on quartz boat.

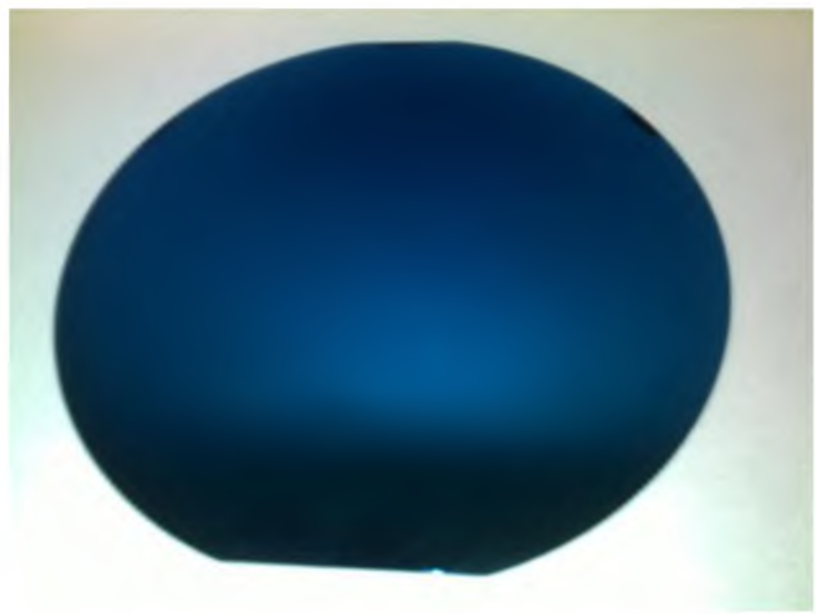


Figure 4.8: 100nm Silicon Nitride wafer surface.

4.2.3. Patterning "Wells" in Silicon Nitride

Photoresist (Shipley 1813) was spun on and photolithography carried out using the first mask. This was used to define 40µm x 40µm 'well'. Using the mask, the underlying silicon nitride later was dry etched (RIE) using a CF_4/O_2 plasma recipe. The tool used for this step was the Oxford 80 Plus RIE. The recipe is given below.

CF_4 flow rate	:	35sccm
O_2 flow rate	:	3.5sccm
Pressure	:	75mTorr
Power	:	200W
Time	:	1min 40s

The Photoresist was next stripped off using Acetone and IPA rinse and further stripped using oxygen plasma using the same RIE tool. The recipe for O_2 plasma is given below:

O_2 flow rate	:	30sccm
Pressure	:	50mTorr
Power	:	200W
Time	:	30s

Fig. 4.9 provides SEM images of the wells that were etched into the silicon nitride all the way through to the silicon substrate.

One of the problems associated with this step was related to nonuniform etching at the edges of the wells. As the RIE etched silicon nitride through the PR "windows", it caused nonuniformity while etching at the edges of the well, as seen in Fig. 4.10. If this problem were allowed to persist, it would translate onto the bridges in the proceeding fabrication steps. In order to avoid it, the RIE etching was extended from 1min 20s to 1min 40s. The results were much better and a more uniform edge was obtained (Fig. 4.11).

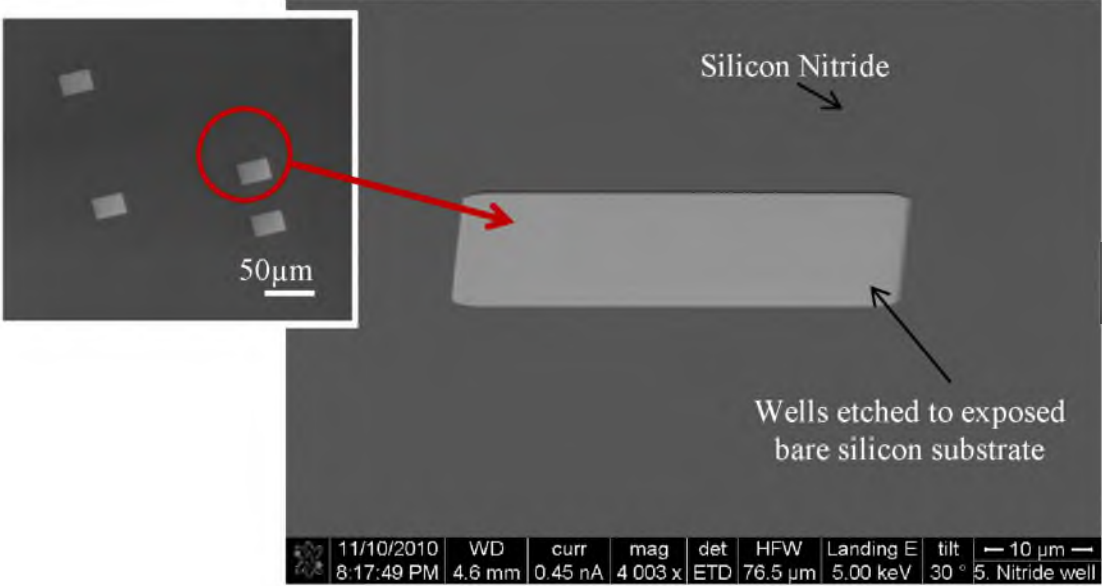


Figure 4.9: SEM of wells etched into first insulating Nitride.

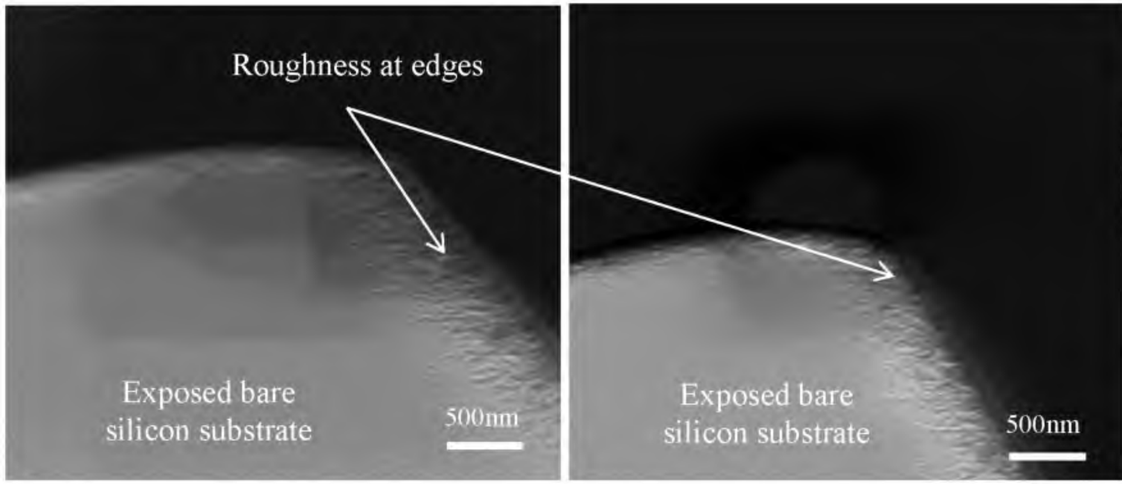


Figure 4.10: SEM of wells' edge shows rough edges on two separate wells. This was corrected for, as seen in fig. 4.11.

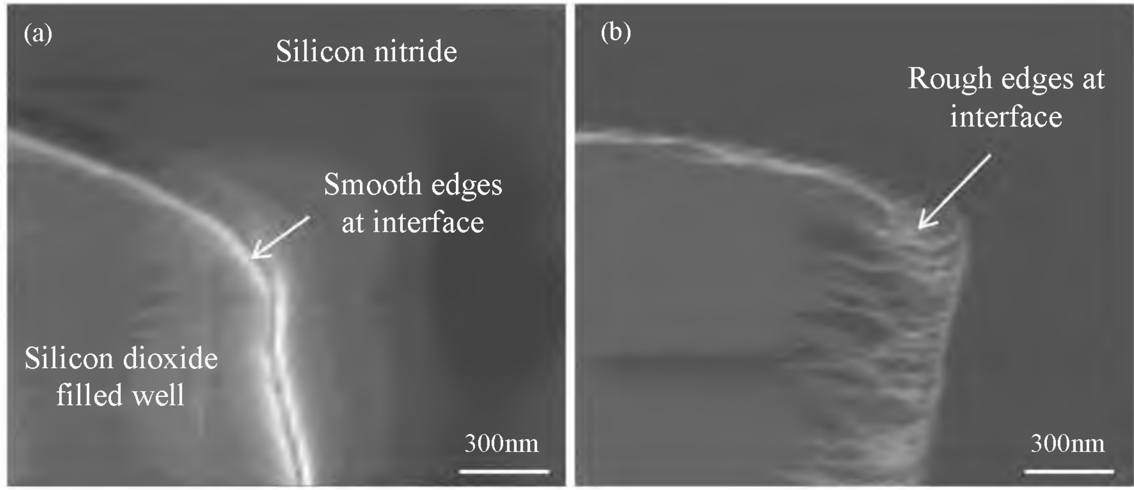


Figure 4.11: SEM of oxide-filled nitride wells. (a) Edges more uniform after over etching nitride wells, (b) Edges non-uniform

4.2.4. Oxide-filled Nitride Wells

The nitride wells were next filled with SiO_2 by timing the wet thermal oxidation step accurately. Wet oxidation was carried at 950°C out in the Canary Oxidation Furnace in the Nanofab. This filled the nitride wells to the brim of the well to act as a support for the proceeding bridge, and later as a sacrificial layer to release the lower bridge. The recipe used is given below:

Temperature	:	950°C
Loop counter	:	70min
N2 flow rate	:	5slpm
O2 flow rate	:	2.25slpm
H2 flow rate	:	4slpm

The thickness of the oxide grown was approximately 260nm using the recipe above. Bearing in mind that 44% silicon is consumed while oxide is grown, the timing was characterized to be just right to grow until the edge of the nitride wells.

The SEM image in Fig. 4.11(a) shows the oxide-filled nitride wells after overcoming the rough edge issue on the nitride wells, while Fig. 4.11(b) shows the rough edges propagating onto the current step if the silicon nitride RIE etch time were not extended as discussed previously. Fig. 4.12 is an optical image of the wafer at this stage, highlighting the uniformity maintained. The golden hue is the silicon dioxide.

4.2.5. Deposition of Silicon Nitride and Polysilicon Layer for First Bridge

The next step was to deposit the first composite bridge layers. Stoichiometric silicon nitride (~100nm) followed by polysilicon (~200nm) was deposited in succession. Both steps were carried out in the respective Canary LPCVD furnaces in the Nanofab.

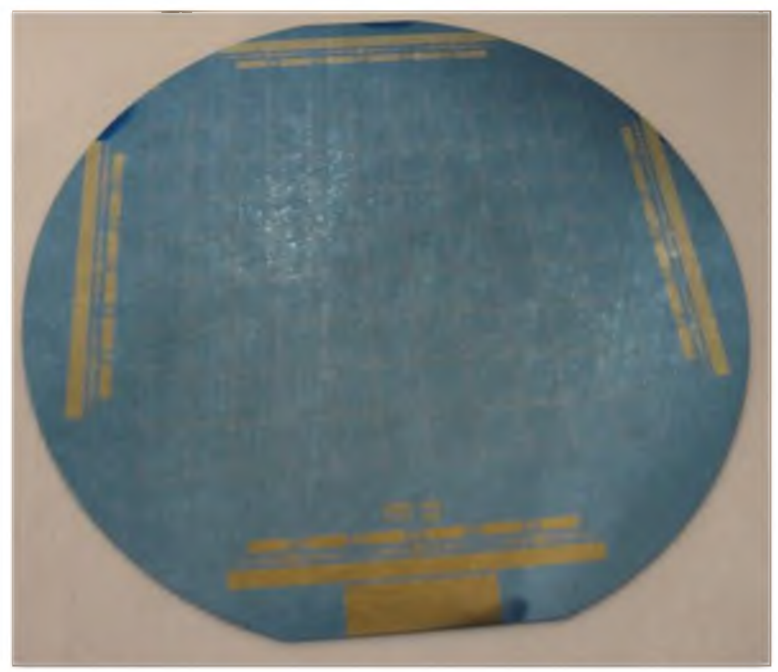


Figure 4.12: Image of wafer after oxide growth in Nitride wells.

The recipes are given below and the optical image of the wafer postdeposition is given in Fig. 4.13:

Process	:	Silicon Nitride Deposition
Temperature	:	780 C
Loop counter	:	25min
NH_3 flow rate	:	80sccm
DCS flow rate	:	20sccm
Controller pressure	:	430-440mTorr
Thickness	:	100nm
Measured stress	:	760MPa (tensile)

Process	:	Polysilicon Deposition
Temperature	:	630 C
Loop counter	:	22min
SiH_4 flow rate	:	55sccm
Controller pressure	:	270-280mTorr
Thickness	:	200nm
Measured stress	:	-50MPa (compressive)

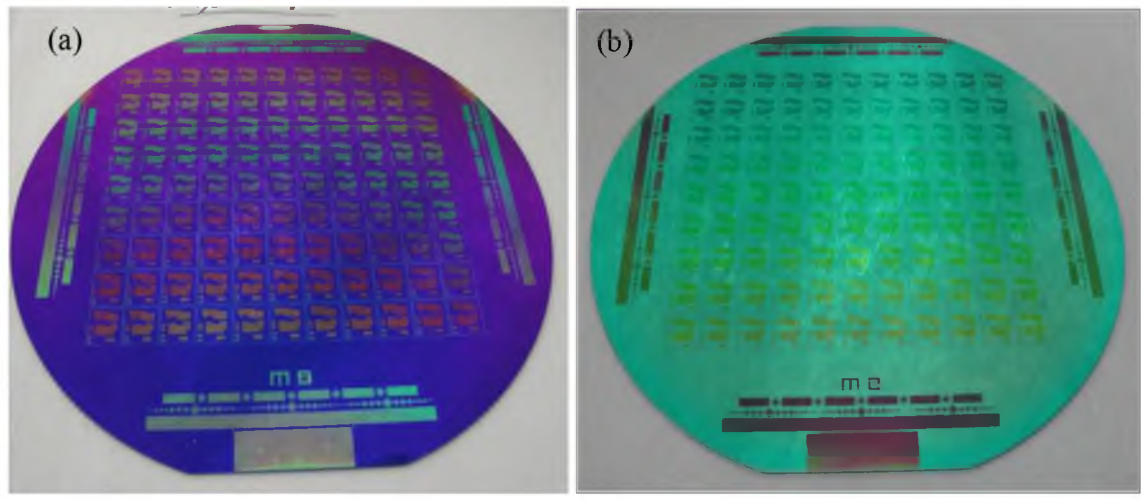


Figure 4.13: Image of wafer after (a) nitride layer deposition over oxide-filled wells (b) polysilicon deposition over nitride layer.

The reason for choosing a composite (layered) bridge structure over a bridge that relied only on one material was that the silicon nitride contributed a tensile stress that would keep the clamped-clamped bridge taut, while the polysilicon layer was compressive. In addition, silicon nitride is prone to being etched (very slowly) in the sacrificial etchant – BOE, while the polysilicon is immune to this attack. As a result, both materials together contributed to having a relatively taut bridge that was compatible with BOE processing.

The wafer is next subjected to annealing in the Canary Oxidation furnace. This enabled the newly deposited polysilicon to relieve its compressive stresses and prevent buckling of bridges postrelease as seen in the SEM images of bridges formed using polysilicon without proper annealing (Fig. 4.14). The recipe used for annealing is given below.

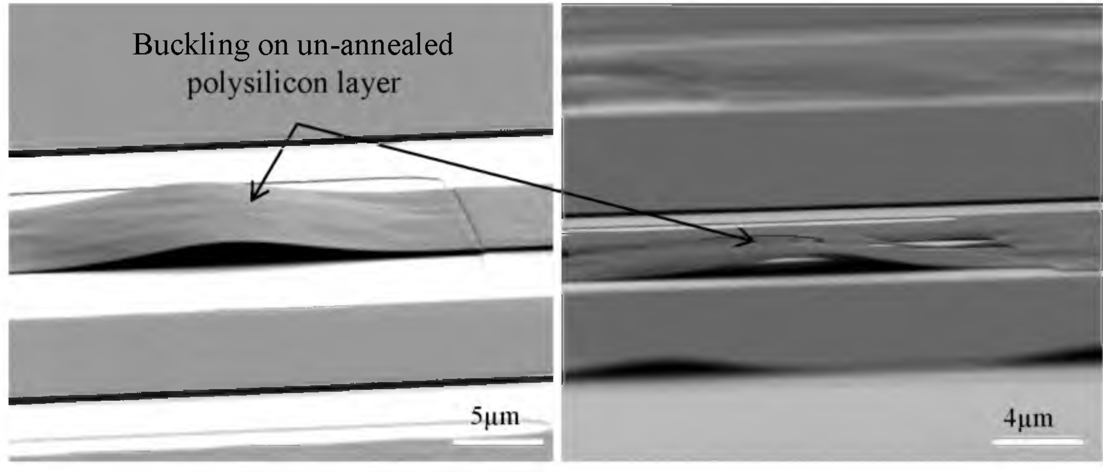


Figure 4.14: Image showing buckled bridges after patterning polysilicon and nitride layers without including an annealing step. Compressive stresses are relieved in polysilicon by annealing.

The program was specially modified to allow growth of an extremely thin layer of SiO_2 over the polysilicon initially and then followed by a pure N_2 flow. This prevented nitridization of the polysilicon at such high temperatures in pure N_2 environment.

Temperature	:	1050°C
Loop counter	:	60min
N2 flow rate	:	5slpm
O2 flow rate	:	2.25slpm
H2 flow rate	:	4slpm
Measured stress	:	545MPa (tensile)

4.2.6. Patterning First Bridge

After annealing, photolithography was carried out to pattern the first bridges. This was then dry etched using the Oxford 80 Plus RIE tool in the Nanofab. The same recipe was applicable to etch both the polysilicon and the silicon nitride layers. The recipe used is given below.

O_2 flow rate	:	3.5 sccm
SF_6 flow rate	:	26 sccm
Pressure	:	75 mTorr
Power	:	100 W
Time	:	4 min

The etching was carried out with observation at intervals of 3min, 30s, and another 30s. The images of the wafer at intermediate stages are given in Fig. 4.15 and the structures formed as a result are given in Fig. 4.16. After patterning, the PR was stripped off in Acetone/IPA rinse and further in O_2 plasma, as was previously done.

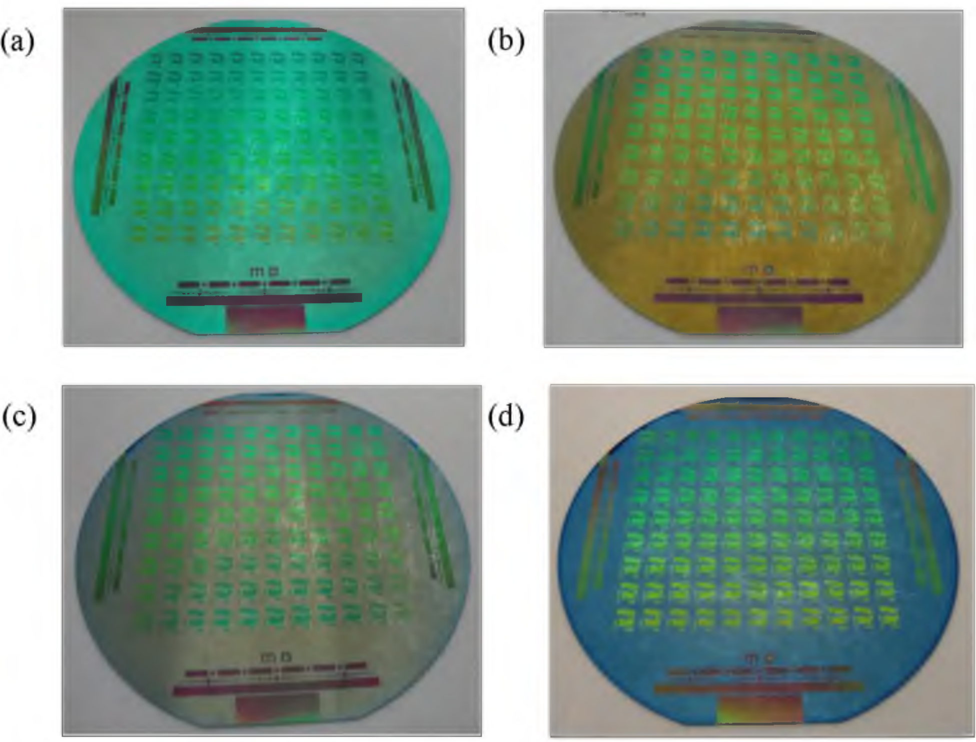


Figure 4.15: Sequence of images showing wafer at intervals of dry etch step for patterning first Polysilicon and Silicon Nitride bridges. a) Before dry etch, b) after 3 min dry etch, c) additional 30s etch, d) additional 30s etch.

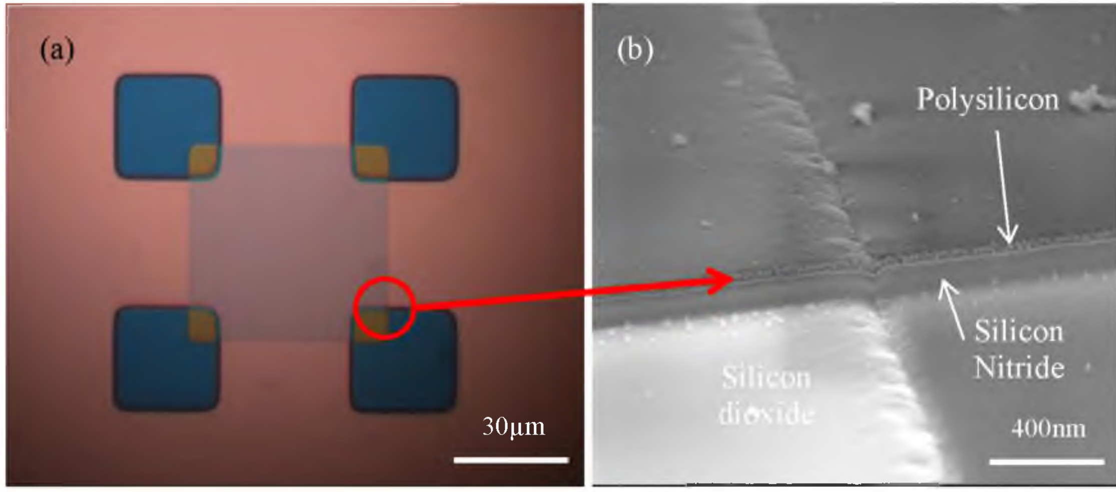


Figure 4.16: Images showing device at stage after composite bridge deposition. (a) Optical image, (b) SEM image of the interface region of the SiO_2 well and composite bridge.

4.2.7. First Metallization

In order to place the first set of electrodes (gate 2 and drain), a 100nm film of Tungsten was DC sputtered using the parameters given below.

Power	: 100 W
Argon flow %	: 25 %
Chamber pressure	: 2mTorr
Time	: 8min 50s
Thickness measured	: 100nm

Photolithography was carried out and this layer of tungsten was patterned using H_2O_2, at room temperature. Wet etching was carried out for ~3-4min. Optical images of the devices after first metallization are shown in Fig. 4.17.

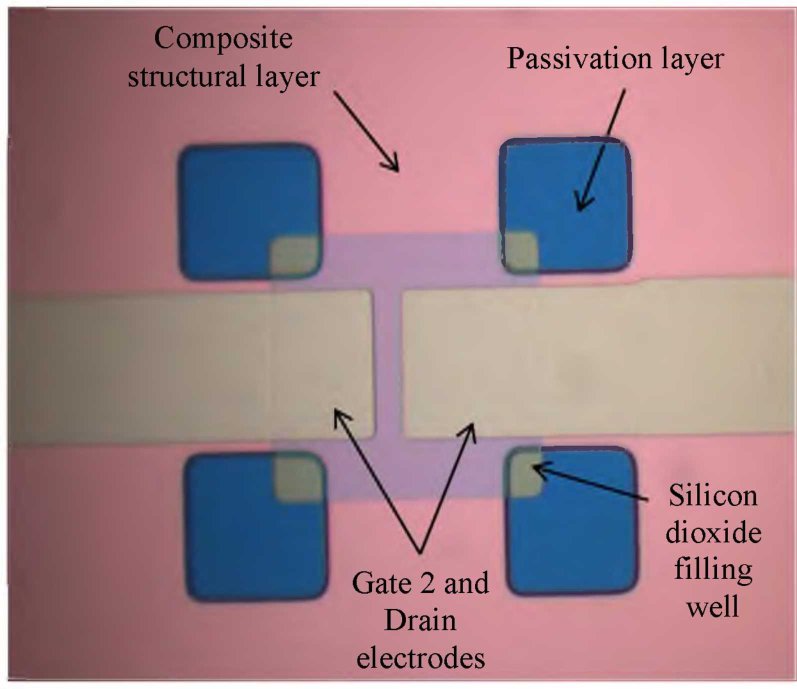


Figure 4.17: Optical image of devices after first metallization.

4.2.8. Gate Dielectric

To prevent conduction between gates 1 and 2 upon snap down, the gate 2 region needs insulation. Although the devices being described here did not have this insulation, a material that would be suitable here is ALD HfO_2 (~10nm). The deposition of such thin materials is very reliable using techniques like ALD and patterning HfO_2 by RIE is now fairly well understood and characterized.

4.2.9. Deposition of Sacrificial Material (Gap Layer)

The gap between the metal contacts was formed by depositing 300 layers (~0.1nm/layer) of ALD Al_2O_3, resulting in a total gap thickness of approximately 30nm. This deposition was carried out in the Cambridge Nanotech ALD tool at 250°C. An optical image of the wafer at this stage is given in Fig. 4.18.

4.2.10. Deposition of Second Metallization

The next step was to deposit the second metallization. As before, tungsten was sputtered using the Denton Discovery 18 sputter tool in the Nanofab. The sputter parameters used are given below.

Power : 100 W
Argon flow % : 25 %
Chamber pressure : 2mTorr
Time : 8min 50s
Thickness measured : ~100nm

This layer of tungsten was patterned using H_2O_2 at room temperature, after photolithography with the appropriate mask. Wet etching was carried out for ~3-4min. Optical Images of the devices after second metallization are shown in Fig. 4.19.

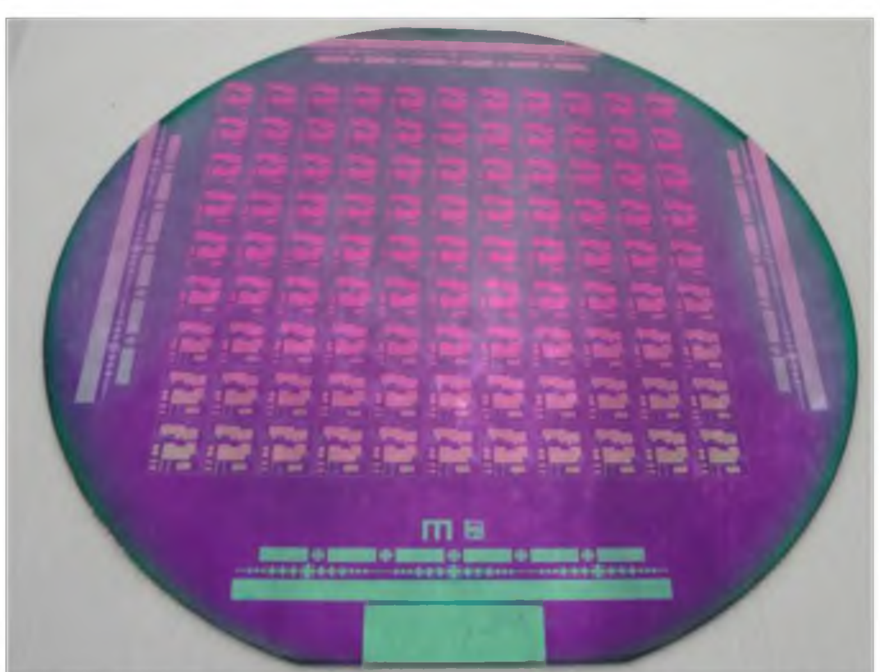
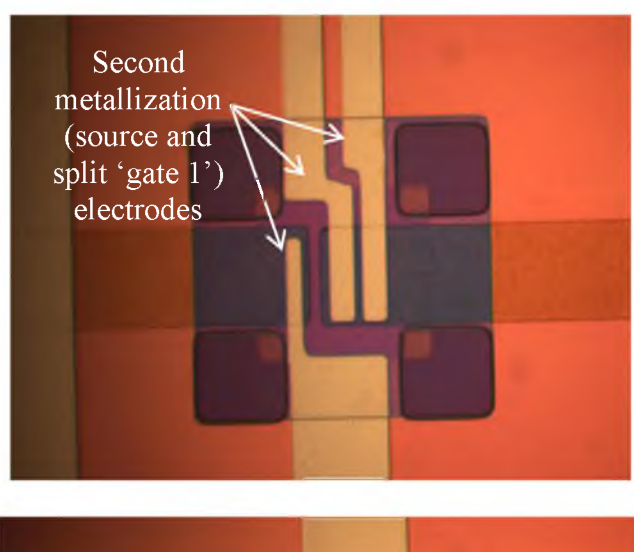


Figure 4.18: Image of wafer after sacrificial layer deposition (300 layers ALD Al_2O_3)



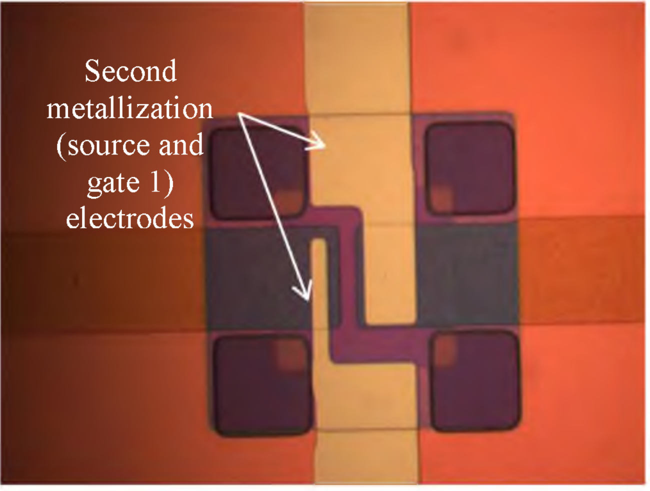


Figure 4.19: Optical images devices after second metallization.

4.2.11. Deposition of Second Structural Bridge

The final structural layers were next deposited using the Canary Furnace stack in the Nanofab. The recipes used for stoichiometric silicon nitride (~100nm) and polysilicon (~200nm) deposition were similar to the first structural bridge. Prior to this step, 3-5 layers of ALD Al_2O_3 at 200°C were deposited as a capping layer before inserting the wafers into the LPCVD furnaces. Furthermore, the deposited polysilicon was then annealed at 1050 °C for 60 min using the oxidation furnace in a nitrogen environment

using the program settings as before. This was necessary to ensure the compressive stresses were relieved from the polysilicon layer. The annealing recipe was modified, as previously, to grow a thin layer of oxide initially to prevent nitridization of the polysilicon in a pure N_2 environment. Following this, the stresses were relaxed and the buckling effects, that would otherwise cause structural failure after sacrificial release, was avoided. Fig. 4.20 provides optical images of the devices at this stage.

4.2.12. Patterning Final Structural Bridge

The final bridges are patterned using photolithography and etched using the Oxford 80 Plus RIE tool in the Nanofab. The recipe used for the dry etch was the same as that detailed previously and required a total period of 4 min of etching. The etch was carried out in intervals to allow for observation before proceeding with further etching. The images of the devices after this step are given in Fig. 4.21.

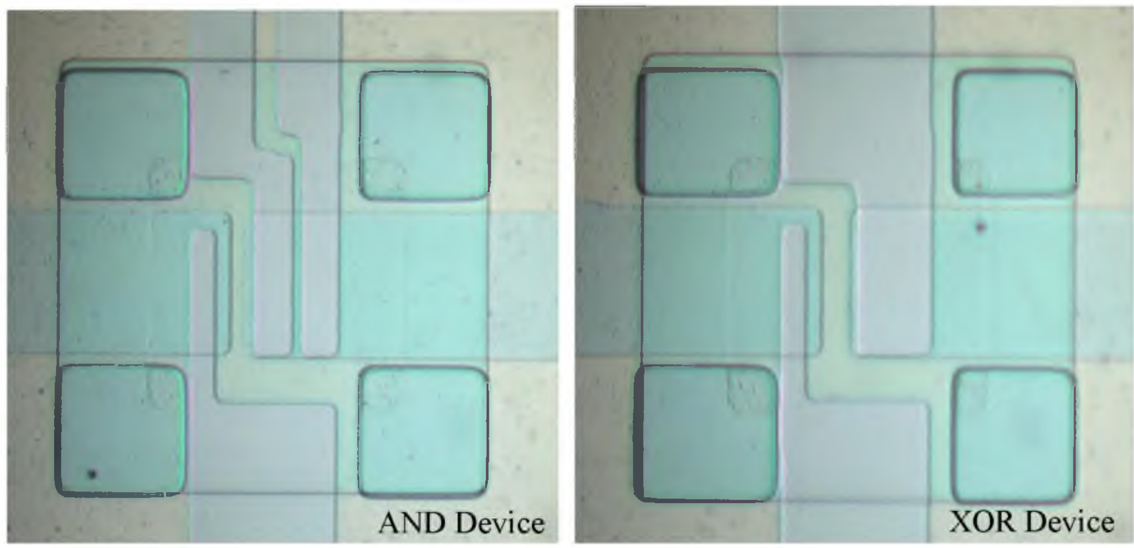
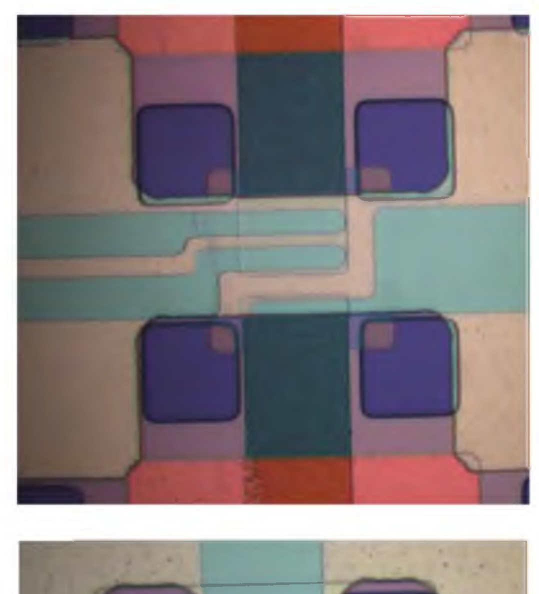


Figure 4.20: Images of devices after deposition of second structural silicon nitride and polysilicon.

AND Device



XOR Device

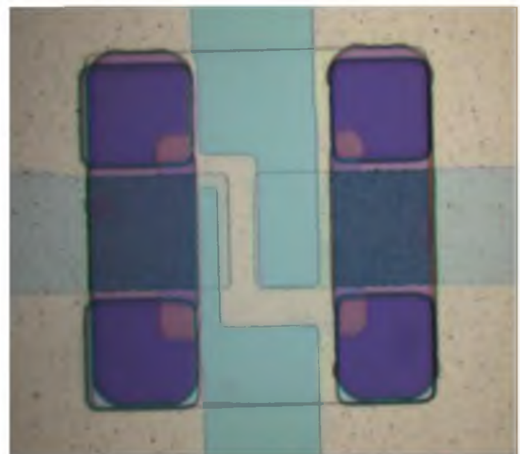


Figure 4.21: Images showing devices after patterning final structural bridge.

4.2.13. Pattern "Windows" for Sacrificial Layer Etch

This step was the last photolithography step for the devices. Photoresist was patterned using a mask such that "windows" were opened just around the switches to enable the release of the sacrificial layer around them. Additionally, there were openings above contact pads to enable probing the various electrodes. The rest of the wafer was protected by photoresist. The optical images in Fig. 4.22 show the photoresist "windows".

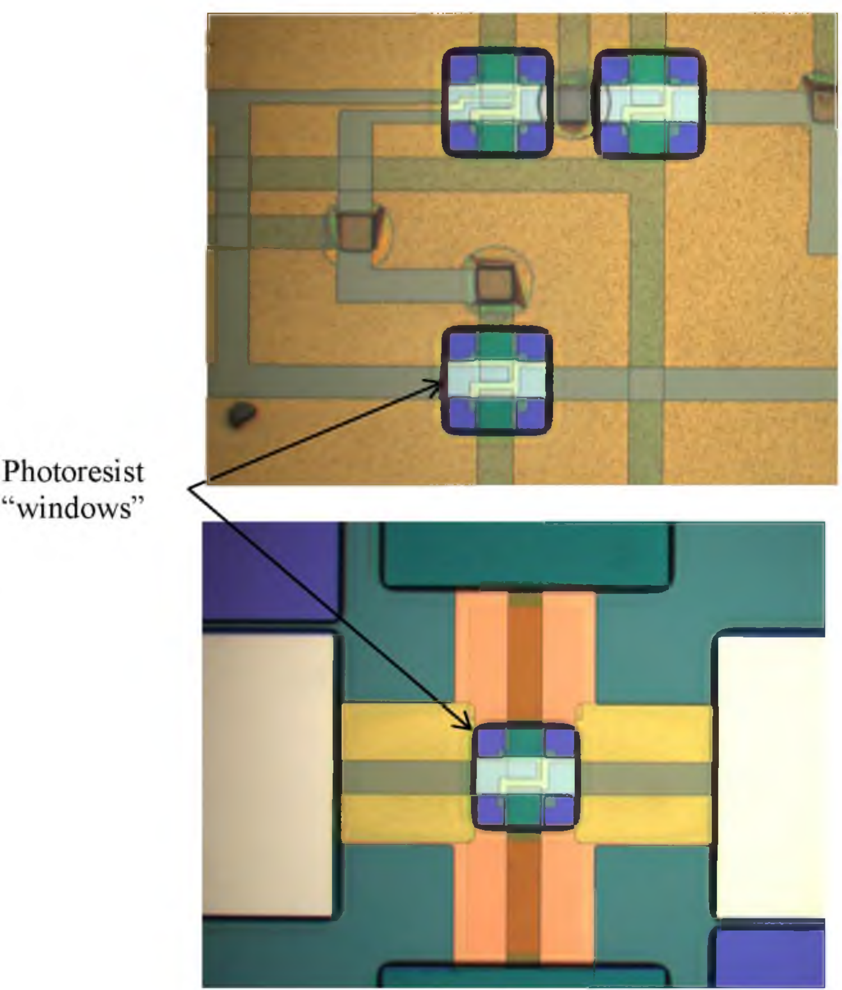


Figure 4.22: Images showing devices with photoresist "windows" patterned.

4.2.14. Sacrificial Layer Etch

Finally, the sacrificial layer (ALD AL_2O_3 and SiO_2) was released by immersing the wafer chips in BOE for anywhere between 5min to 20min. Immediately after BOE etch, the chips were gently flushed in DI water bath followed by a methanol bath. This step was followed by a vacuum dry-step which minimized damage to the released bridges via nitrogen-gun drying. The vacuum step ensured uniform evaporation of the methanol

and also prevented stiction of the fixed-fixed beams. The released devices are shown in Fig. 4.3.

4.3. Summary

This chapter provides details of the process flow used to fabricate the single-device XOR and AND gates. The fabrication was carried out at the University of Utah Nanofabrication facility. Structural materials used to fabricate the device include a composite of LPCVD silicon nitride and LPCVD polysilicon. Electrodes were made of sputtered tungsten and the sacrificial layers were made of thermal Silicon dioxide and ALD aluminum oxide. Images of the wafer at each processing step are also provided.

CHAPTER 5

TESTING AND CHARACTERIZATION

This chapter discusses the electrical characterization of the single-device logic gates that were fabricated, as described in Chapter 4. Testing was carried out in the Advanced Metrology and Nano Device Applications (AMANDA) lab at the University of Utah. The devices were tested to investigate switching voltage, leakage power, longevity, logic gate function, and harsh environment performance (high temperature and high ionizing radiation). The experiments were carefully planned and repeated several times to confirm the results. Compilations of the best and most representative data are provided and discussed in the following sections.

5.1. Characterizing Switching

The micro-fabricated XOR gates were tested to find their switching characteristics and reliability using an Agilent 4156C Precision Semiconductor Analyzer (with compliance set at 1μA) and a probe station, as shown in Fig. 5.1. A switching voltage of approximately Vp ~ 1.5 V was observed over repeated cycling, as can be seen in Fig. 5.2. In this and next tests, the gate 1 was shorted to source and gate 2 was shorted to the drain and the switching voltage was applied between the top and bottom bridges.

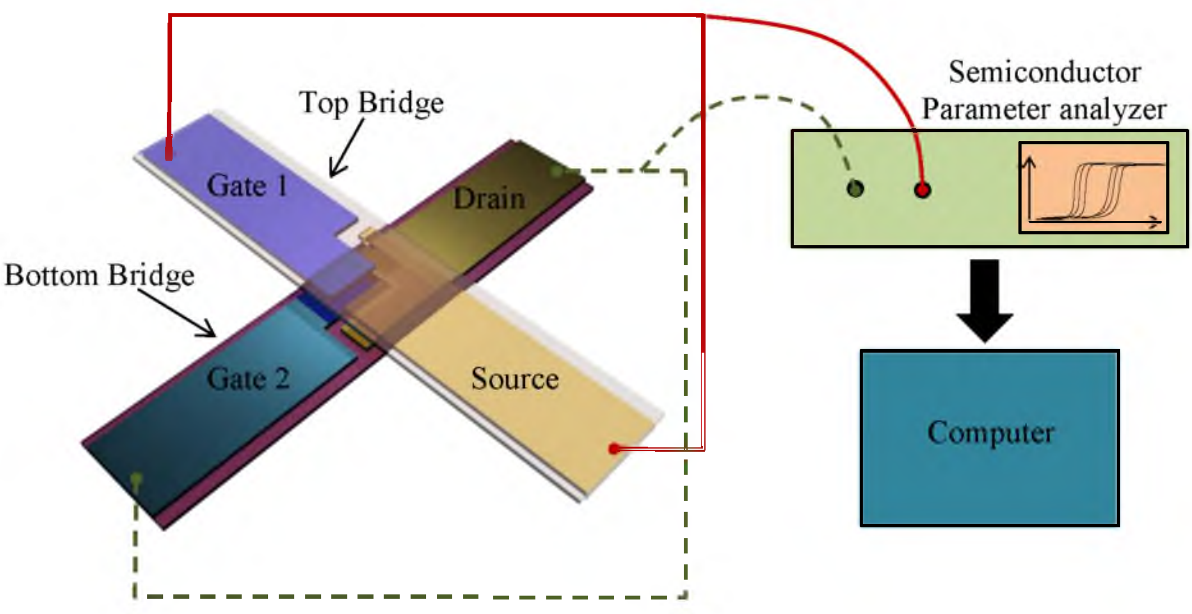


Figure 5.1: Experimental setup to characterize switching performance

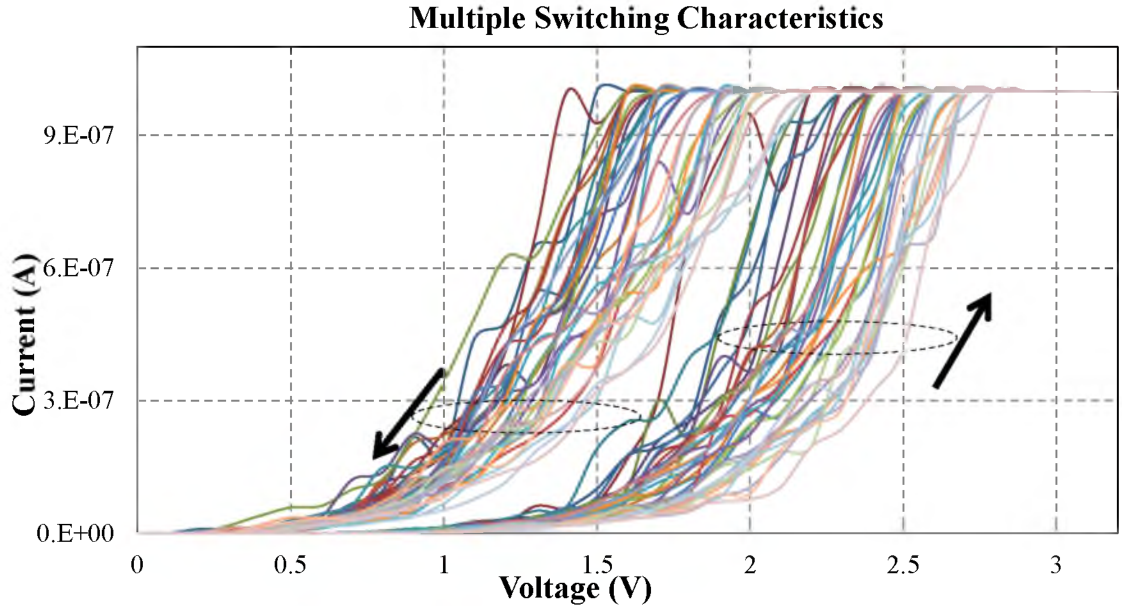


Figure 5.2: I-V characteristics over a portion of a million switching cycles. In this test, the G1 was shorted to S and G2 was shorted to D and the voltage was then applied between the G2-D and G1-S electrodes. The experimental setup is shown in Fig. 5.1. The dashed circles and the associated arrows indicate the I–V branch in the forward direction and reverse direction for the many traces shown here. The hysteresis is due to stiction between the bridges after they touch each other.

The device's drain and source electrodes were situated on separate bridges leading to very small surface leakage current. The electrodes had ~4μm^2 contact area and their leakage current was measured at less than 10^{-9} A at 0.5 V. The leakage power is shown in Fig. 5.3.

Additionally, device lifetime measurement was carried out and its continuous switching characteristic obtained over 10^9 cycles, as shown in Fig. 5.4. The device was intact even after the 10^9 cycles, after which the experiment was arbitrarily halted. The device operated reliably even after 10^9 cycles of accelerated-wear emulation.

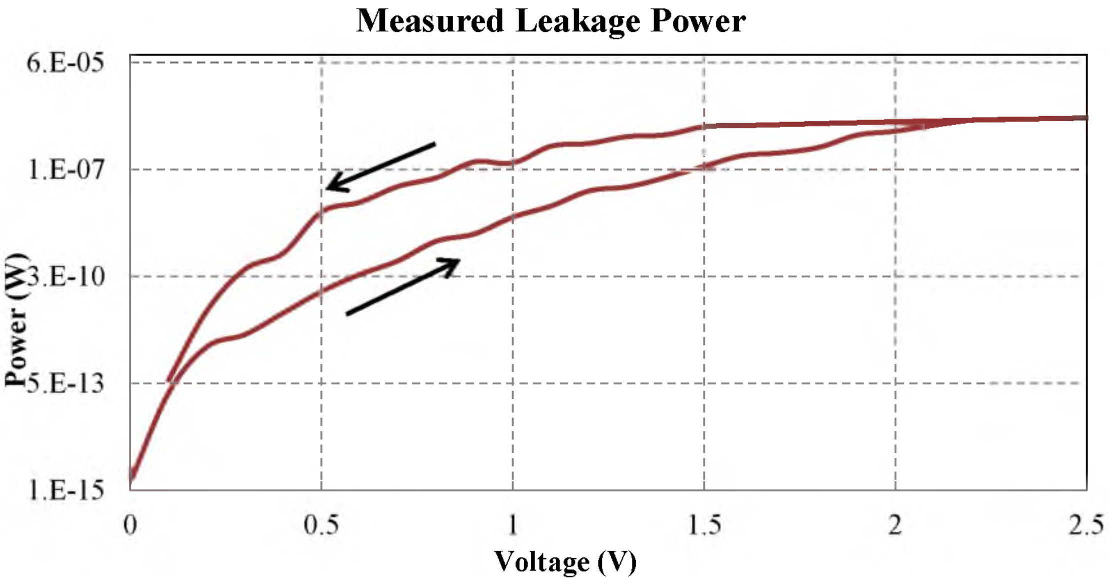


Figure 5.3: Graph showing leakage power characteristic of the fabricated XOR gate (1uW). The arrows show direction of scan. The hysteresis is caused by stiction, as discussed in Fig. 5.2.

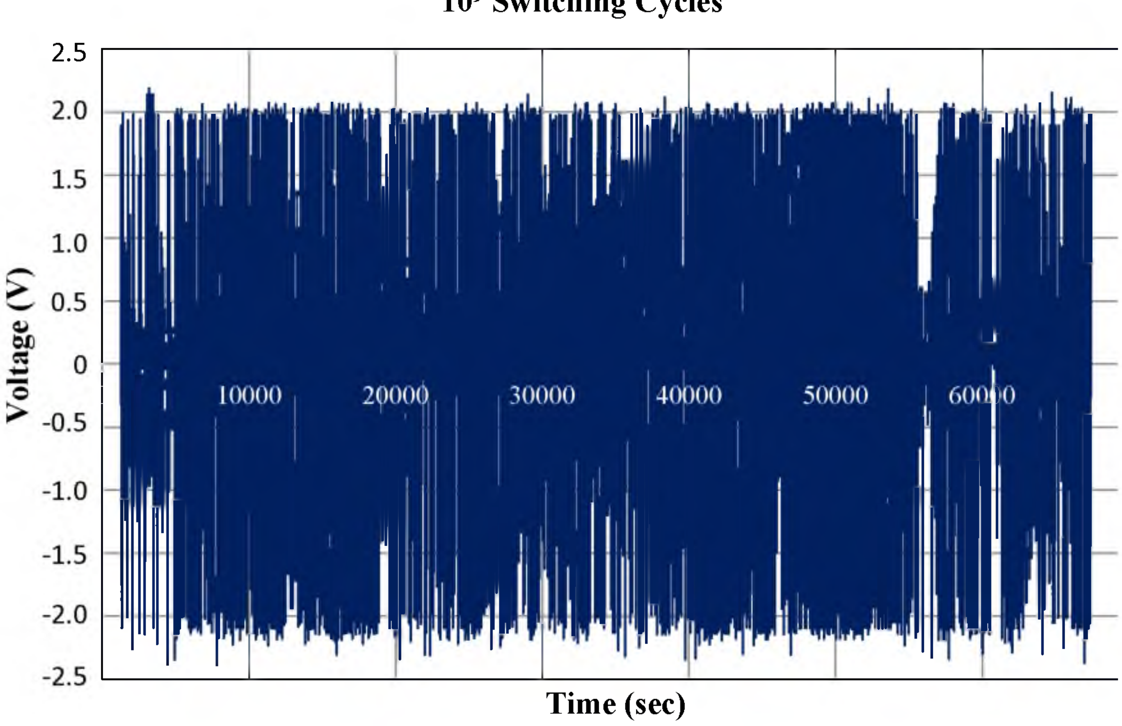


Figure 5.4: Switching characteristics of the XOR gate operated as a switch. The gate switched up to 10^9 cycles and the study was limited by the experiment time.

5.2. Logic Gate Operation

The setup used to test the device's logic functionality is schematically shown in Fig. 5.5. As seen from the switching characteristics, the two gate regions attract each other only when one of them is high. No actuation was observed when either both gates are low or both gates are high. At the ON state (when the bridges contact each other), the drain and source electrodes contact each other and produce the desired output. This simple structure operates as an XOR gate.

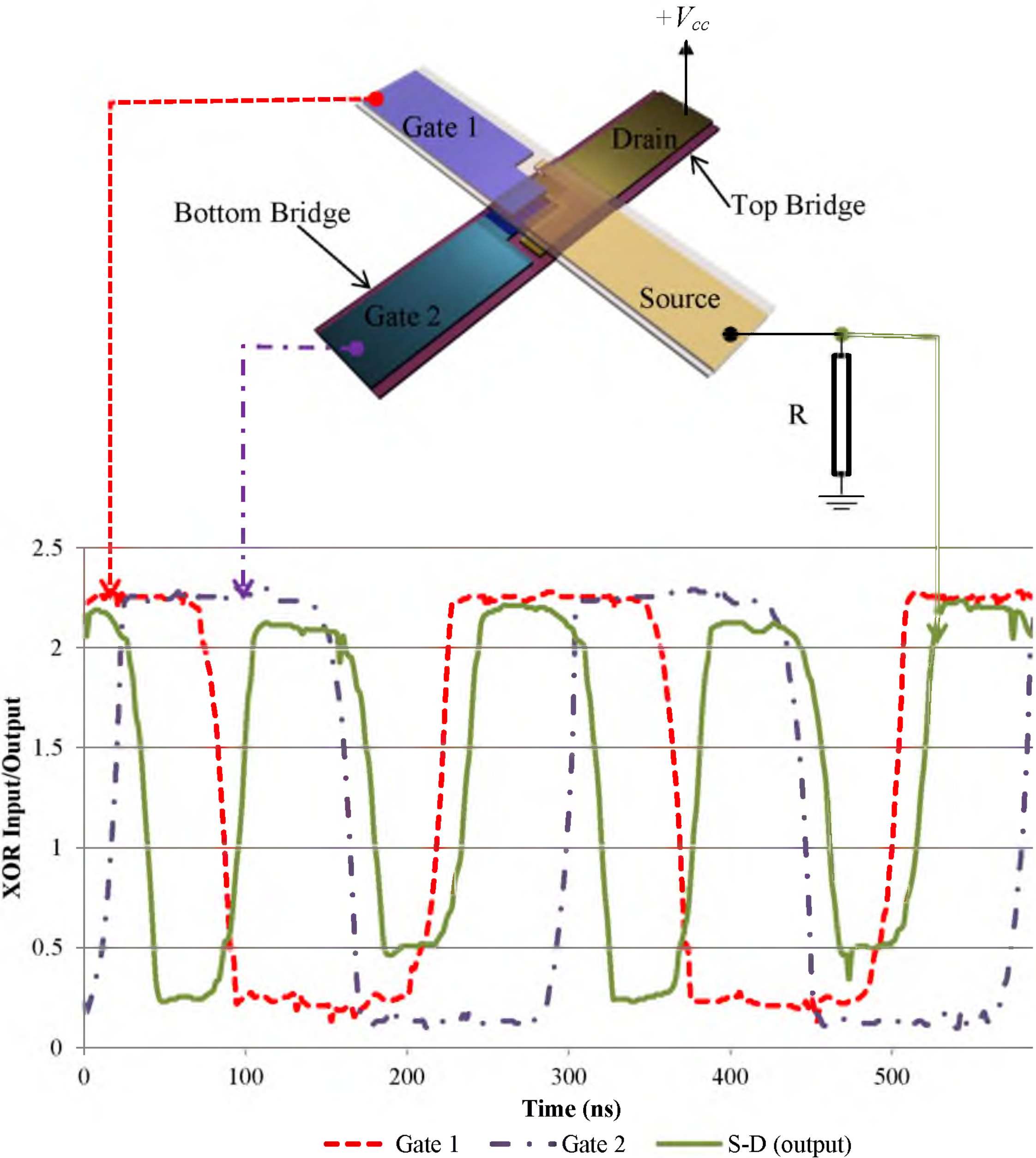


Figure 5.5: Voltage transitions of a single XOR device. S-D transitions to HIGH only when either G1 or G2 are high. When both G1 and G2 are LOW (or HIGH) together, S-D transitions to LOW.

5.3. Harsh Environment Performance

The devices were also tested at elevated temperature inside a vacuum chamber. I–V characteristics of the switch at 298 K and 409 K are shown in Fig. 5.6. The switching characteristics did not change considerably at elevated temperatures, albeit shifted by ~0.5 V. The shift in the voltage at elevated temperatures can be caused by the temperature dependence of material parameters (i.e., Young's Modulus) and by the temperature dependence of the electrical properties of the different parts of the switch. The temperature dependence of the contact region may dominate in most cases since it is the most active part of the switch.

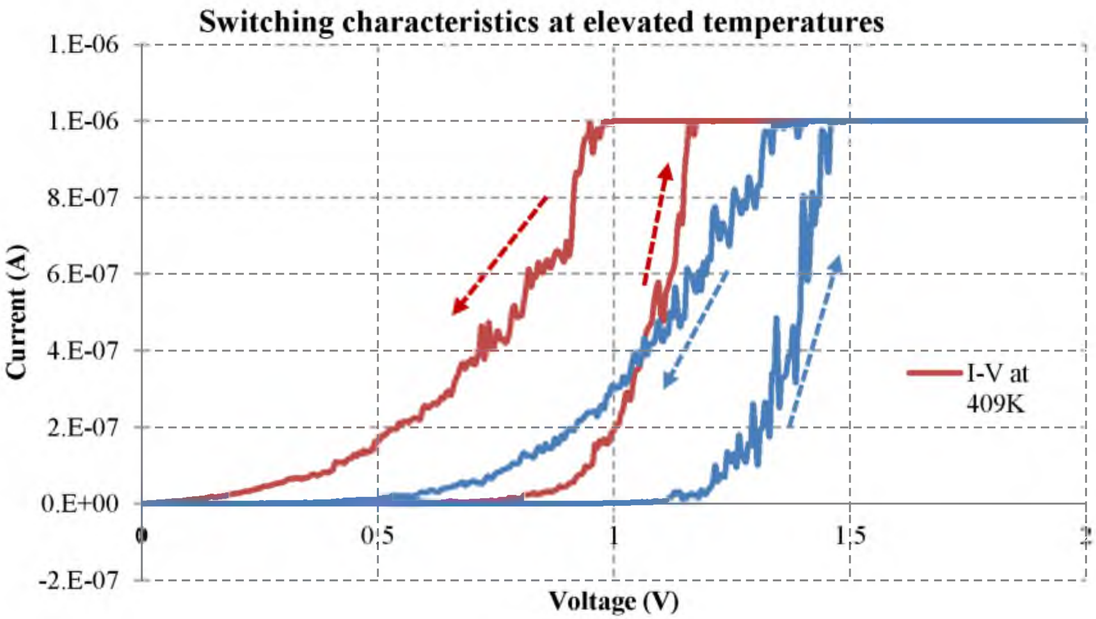
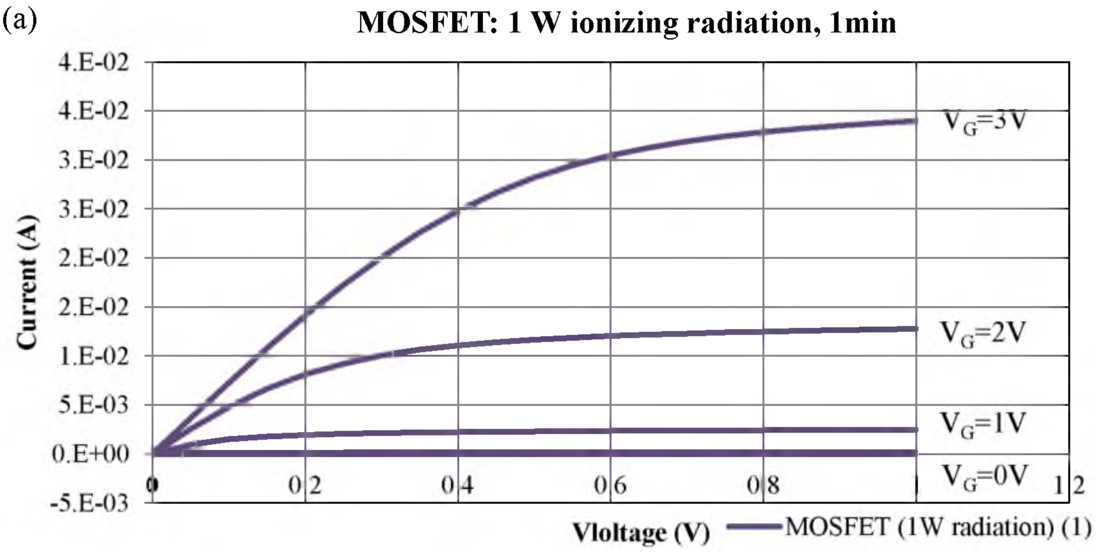


Figure 5.6: Switching characteristics at elevated temperatures. These tests were performed using the same electrode arrangements used in Fig. 5.5.

In order to investigate the performance of these devices in high radiation environments, the TRIGA reactor at University of Utah was engaged to bombard the fabricated devices with high ionizing radiation. According to reactor specifications, at 90 kW, typical neutron flux is $\sim 3\times 10^{12}$ neutrons/cm^2-s. The energy of the neutrons varies from 0.025 eV to 10 MeV, but most have energies less than 1 MeV. In general, alpha particles do not exist in the reactor core except for inside the fuel element, which has an average energy of 6 MeV. It is known that gamma rays exist ubiquitously in the reactor core. Approximate gamma flux is on the order of 10^{13} gamma/cm^2-s (or higher). Gamma particles' energy ranges from approximately several keV to 3 MeV. Beta particles' flux at 90 kW is approximately 10^{13} beta/cm^2-s and typical energy of a beta particle is between 100–1500 keV.

Figs. 5.7-5.8 show the I–V characteristics of a MOSFET and an XOR gate connected as a switch (i.e., Gate 1 shorted to source and Gate 2 shorted to the drain) inside the TRIGA nuclear reactor at 90 kW, respectively. After a few minutes of exposure, the MOSFET's I_{DS} increased by an order of magnitude and its channel became permanently conducting (Fig. 5.7). At this point, the MOSFET gate voltage could no longer control the channel current. In the case of the XOR gate, the I–Vs were not affected appreciably by the radiation even after 120 min (Fig. 5.8). The switching voltage changed somewhat, but the device continued to operate with clear "ON" and "OFF" states. Many factors may contribute to the changes in the switching parameters of MEMS and NEMS exposed to intense ionizing radiation. Material embrittlement following large densities of defect generations, the resulting resistance changes, and heating are just to name a few.

(a)



(b)

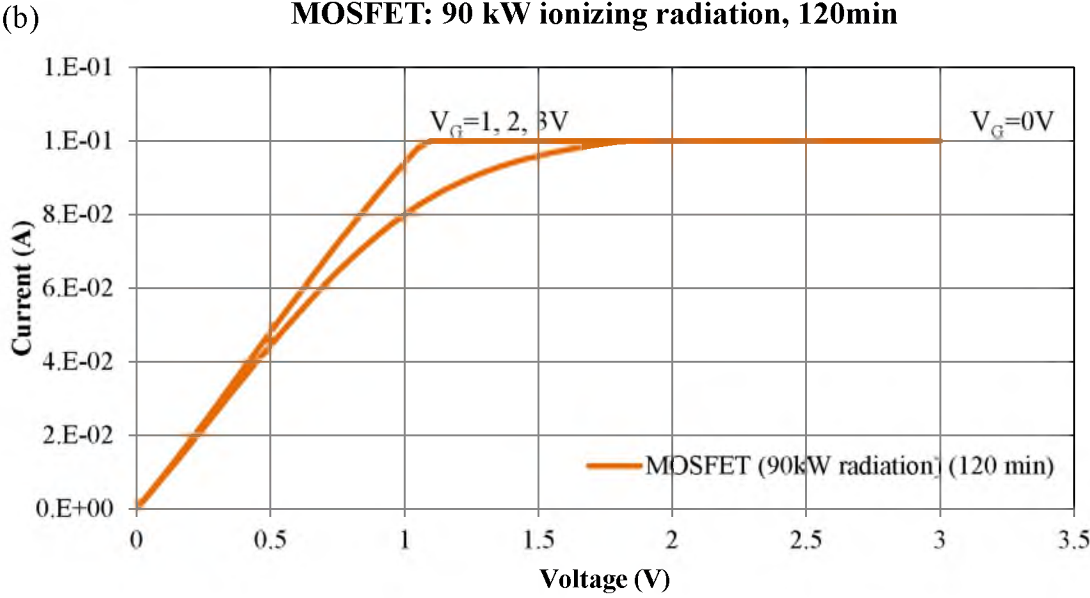


Figure 5.7: MOSFET I_{ds}–V_{ds} at (a) 1 W ionizing radiation, 1 min. (b) 90 kW ionizing radiation for 120 min. After 120 min, even after increasing V_{ds} up to 3 V, there is no change in I_{ds}.

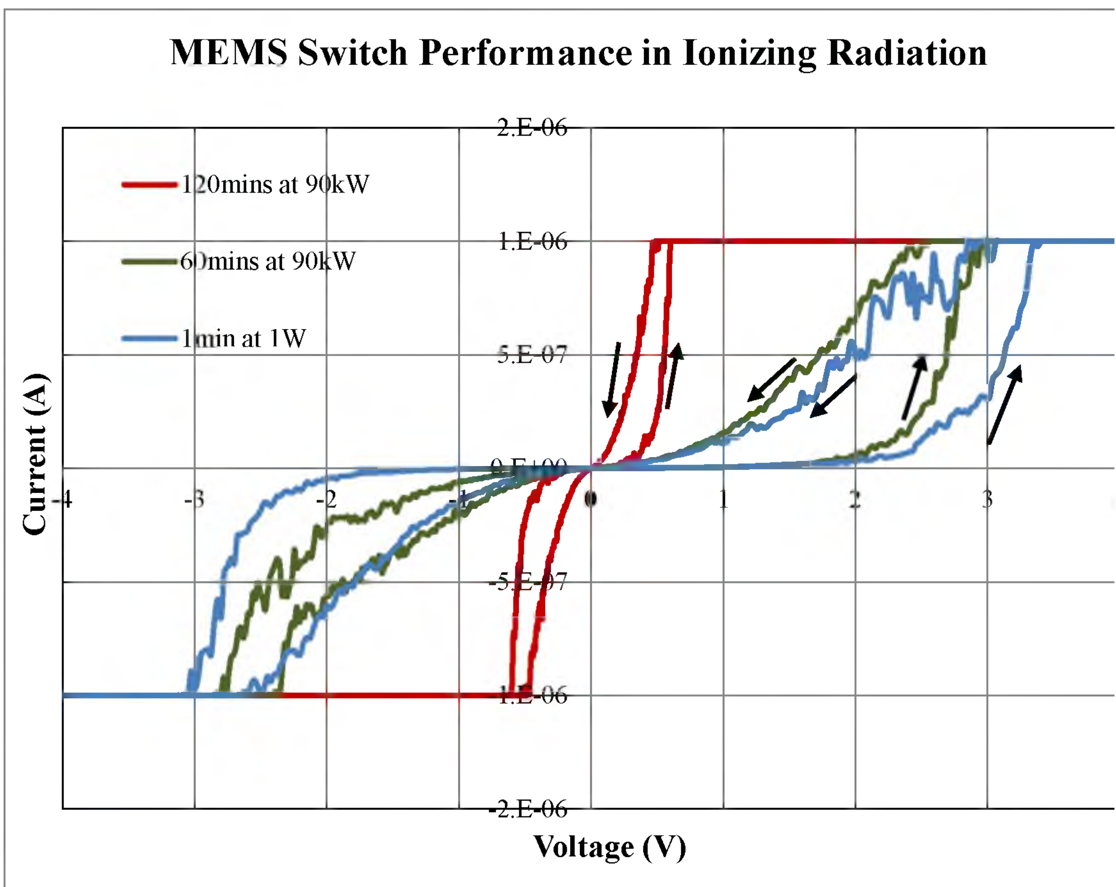


Figure 5.8: MEMS switch I–V characteristics at 1 W-1 min, 90 kW-60 min and 90 kW-120 min ionizing radiation. Clear “on” and “off” states are still discernible even after prolonged exposure to I–R. The arrows show scan directions.

5.4. Validation

A comparison between the calculated, simulated, and measured performance metrics of the switch are summarized in Table 5.1. It can be seen that the disagreement between most calculated and measured values are quite large. This is mainly due to the simple nature of the equations used. Essentially, factors such as fringing fields, viscous damping, squeeze film damping, torsional hinge effects, inertia, etc. were neglected during preliminary calculation. These, however, were taken into consideration to a larger extent in the FEA simulation and as a result, the agreement is much better with measured results.

Table 5.1: Comparison of calculated, simulated, and measured performance metrics.

Metric	Calculated	Simulated	Measured
Pull-in voltage	1.6V	2V	1.5V
Switching time	45ns	30ns	30ns
Resonant frequency	8MHz	10MHz	5Mhz
Leakage current	-	10^{-40}A	$<10^{-9}$A
Spring constant / *w*	~ 24 N/m/µm	32.5 N/m/µm	10.1 N/m/µm

5.5. Summary

This chapter discusses the characterization techniques used to test the devices and results obtained. The devices were characterized for their switching and revealed a pull-in voltage of approximately 1.5V, a lifetime exceeding 10^9 switching cycles, and successful operation as a logic gate (XOR). Additionally, the devices were interrogated in harsh environments where at elevated temperature (409K), the devices remained operational, albeit with a 0.5V shift in pull-in voltage attributable to material property changes corresponding to temperature elevation. When exposed to high ionizing radiation, the MEMS devices outperformed solid-state transistors by illustrating clear ON and OFF states even after prolonged exposure to high I-R doses (120min at 90kW), while the solid state devices were unresponsive within minutes of exposure to I-R.

CHAPTER 6

ADDITIONAL WORK

This chapter discusses additional work that was done to complement the single-device-logic gate devices. First, scaled MEMS switches that rely on ALD SiO_2-Al_2O_3 electrets [1] that enable both attractive and repulsive field effects are discussed. As a result, the devices present field-assisted pull-in/pull-out voltage modulation. This technology renders the MEMS switches highly desirable in harsh environments such as high temperature and high ionizing radiations – where pull-in voltage variation is seen [2] – for *in-situ* voltage compensation/correction. Second, MEMS switches to efficiently manage power in scaled CMOS that can be integrated with Back-End-of-The-Line (BEOL) VLSI processes are discussed. And third, the design of simple, functional circuits making way for more complex systems using such circuits – probably even electro-mechanical microprocessors – is discussed.

6.1. Additional Work

6.1.1. Charged-Electret Scaled MEMS Switches and Logic Gates

A considerable dependence of pull-in voltage change of MEMS switches on the environmental conditions in harsh environments has been seen [2]. To address this, charged SiO_2-Al_2O_3 electrets are incorporated into the single-device MEMS logic gate

structure, illustrated in Fig. 6.1. These electrets were fabricated using a new technique based on ALD Al_2O_3-SiO_2 stack deposition.

Charged electrets possess a net electric charge and can respond to applied external electric fields, resulting in a displacement in response to the applied E-field. The converse phenomenon may also occur where a displacement of an electret in an E-field can result in a current flow. As a result, such electrets have been widely used in transducers such as microphones, electric-field, pressure, temperature, and radiation sensors [3, 4]. However, with the increased popularity of MEMS, the use of electrets has seen new opportunities that take advantage of the massive reduction in actuation voltages for a given displacement [5-7]. Materials generally used to create these electrets include teflon, parylene, PVDF, PDMS, and frequently, SiO_2. The stored charges can be both surface and/or bulk in nature. Interface trapped charges also contribute to the overall charge in a multilayered stack. In porous materials, electrets are created by charges trapped in the porous cavities. Due to the unipolar nature of these electrets, both attractive and repulsive forces can be obtained, as opposed to purely electrostatic that is only attractive.

Generally, electrets are produced by corona discharge or electron beam scanning, both based on a very high electric potential. In the devices discussed here, the electrets are formed by a combination of thermal ALD Al_2O_3 and plasma-enhanced ALD SiO_2 deposition technique that inherently results in electret formation within the bilayer stack and eliminates the need for further steps for electret charging [1]. The fabrication flow is outlined in Fig. 6.1.

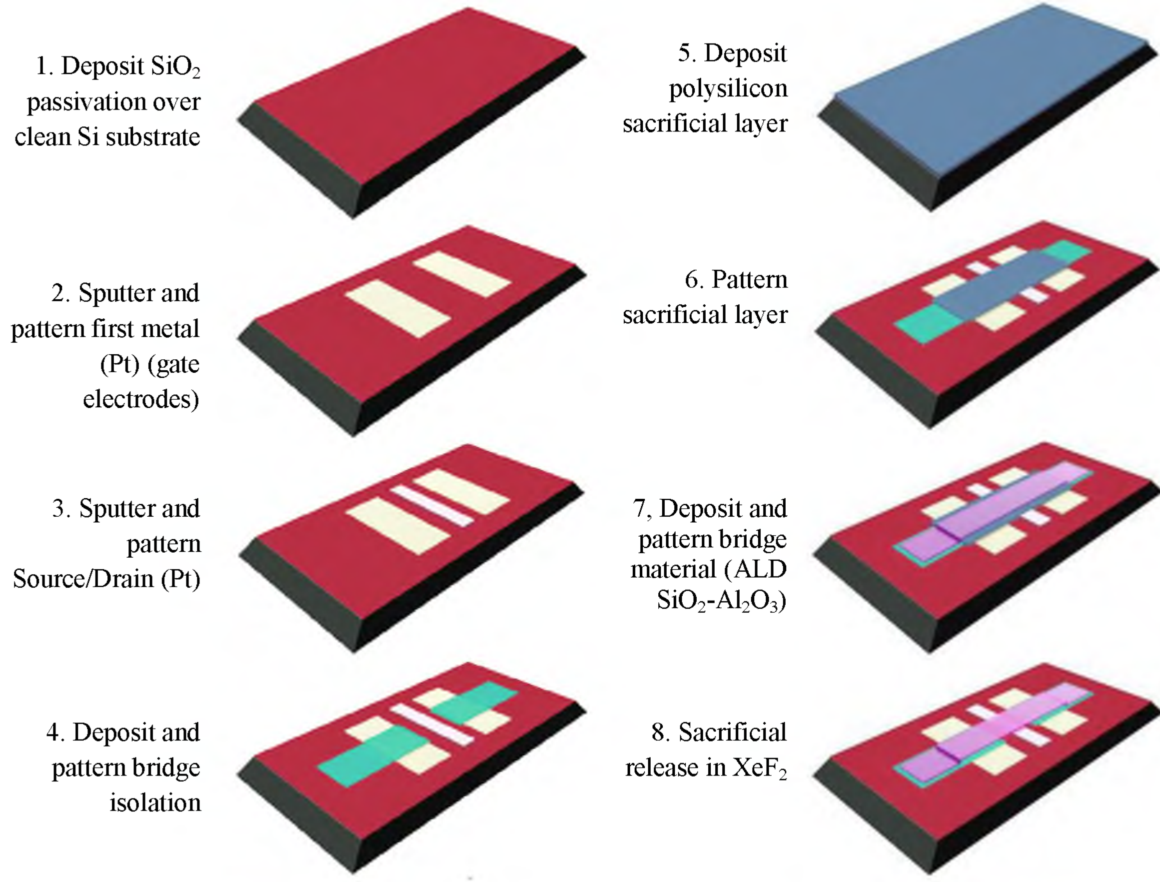
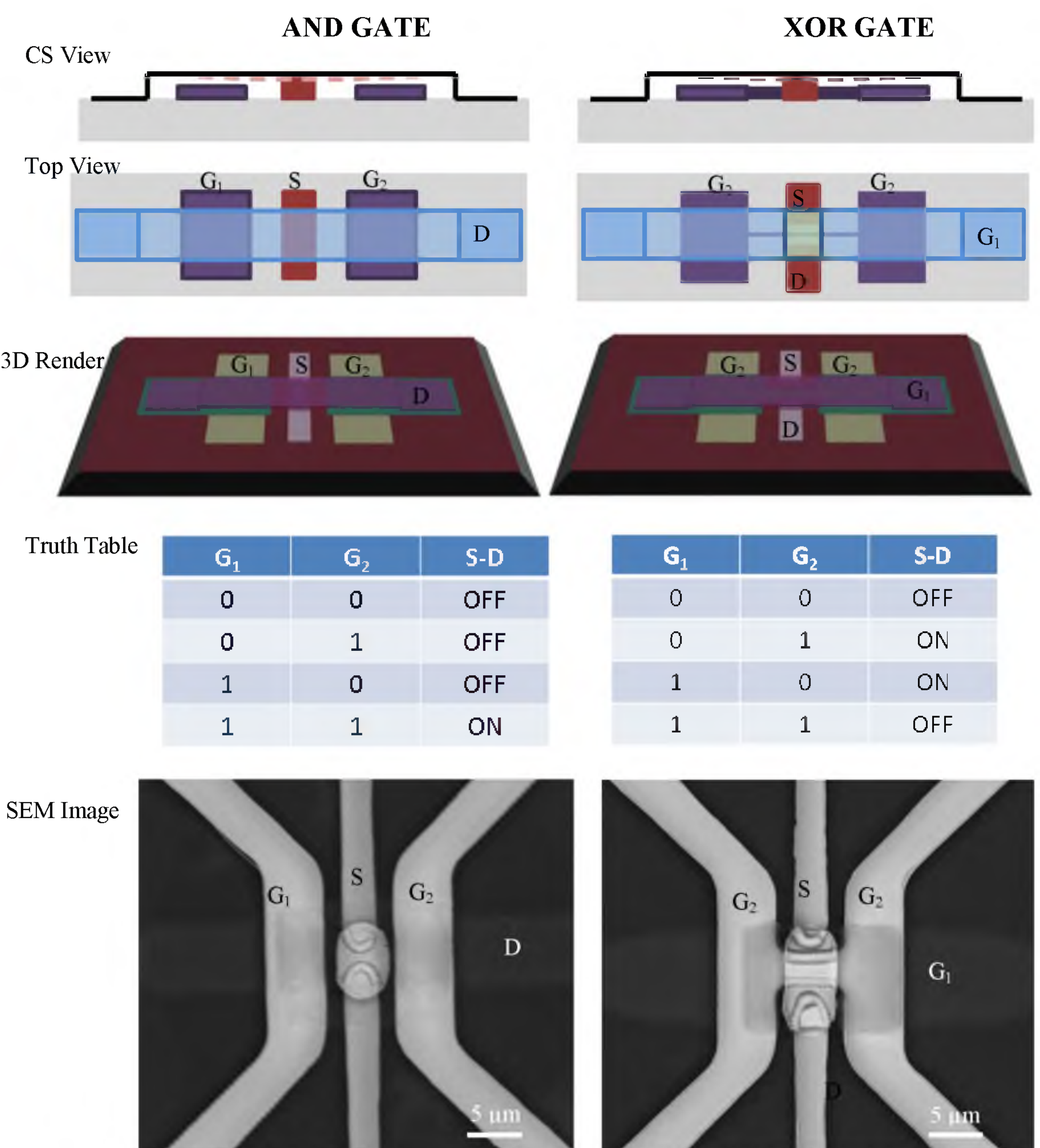


Figure 6.1: Fabrication flow of twin gate MEMS-AND gate. The XOR fabrication follows a similar flow, with a slight modification for patterning the first and second metallization and for including electrode under the bridge.

SEM images of the fabricated devices, 3D render, and schematic of its G1, G2, S, and D terminals are illustrated in Fig. 6.2. The AND device consists of a clamped dielectric bridge (ALD SiO_2-Al_2O_3) spanning across two gate electrodes and supports a Pt electrical contact underneath it. This contact terminal is attracted towards the gate regions only when both of them are high (“G_1, G_2”=“1, 1”). When both are low or the combination of either "0,1" or "1,0", there is no (or insufficient) electrostatic attraction to cause drain-source contact if the electrets are discharged. In the case of electrets being present, we observe field-assisted pull-in voltage control.

In the XOR device, G_1 is the insulating bridge, with a metal contact underneath. G_2 is shorted between the adjacent electrode pads by a small interconnect. Only when G_1 and G_2 are "1,0" or "0,1" is there sufficient electrostatic force to cause the bridge to collapse, making a connection between Source and Drain..

The field effect modulation of pull-in voltage is illustrated in Fig. 6.3. With the application of V_g=-5V, the pull-in voltage is driven to 15 V, with gradual increase in gate voltage to V_g=-2.5V, V_{PI}=10V, and finally at V_g=0V, V_{PI}=3V. We can conclude that the electrets were negatively charged, owing to the trend seen when negative gate voltages were applied, and confirmed by measurement as explained in [1]. The density of the infused negative charges was measured at ~ 12pC/cm^2. Fig. 6.4 graphically summarizes the switching voltage (V_{on} and V_{off} as a function of gate voltage V_G). It is seen that V_{on} increases nearly linearly with an increase in negative gate voltage (V_G). V_{off} remains fairly constant and can be attributed to the fact that the surface energy between the contacts does not change as a function of applied gate voltage. As a result, the trend seen in the curve of V_{on}-V_{off} is similar to that of V_{on}, alone.



AND GATE

G_1	G_2	S-D
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

XOR GATE

G_1	G_2	S-D
0	0	OFF
0	1	ON
1	0	ON
1	1	OFF

Figure 6.2: Next Generation (twin-gate) XOR and AND gate layout, 3D render, truth tables, and SEM Images.

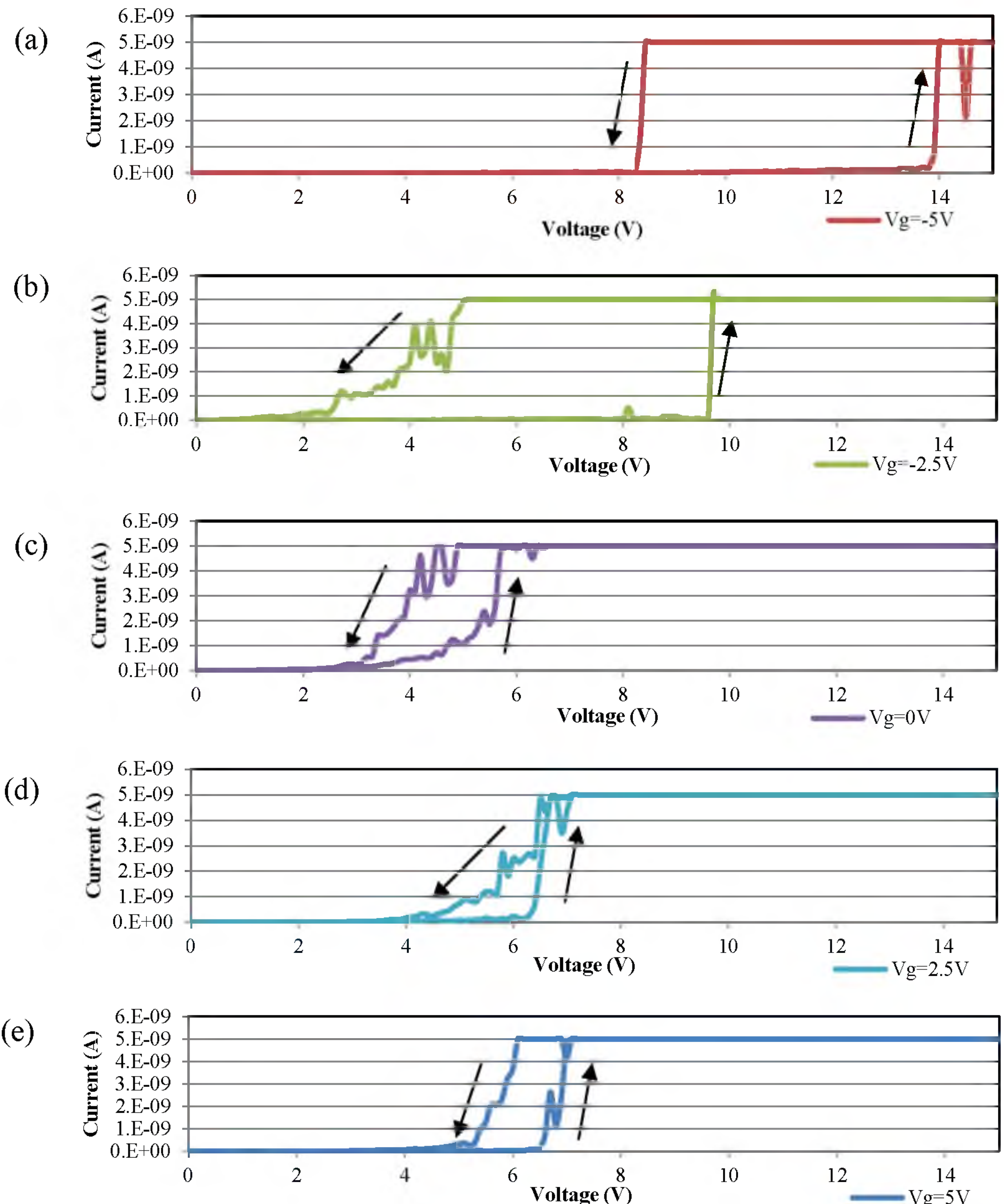


Figure 6.3: I_{DS}-V_{DS} characteristics of the MEM Logic gate shown in Fig. 6.2 with V_g=-5V, -2.5V, 0V, 2.5V, and 5V. Field-assisted pull-in voltage variation seen as a function of applied gate voltage. At (a) V_g=-5V, V_{PI}=14V; (b) V_g=-2.5V, V_{PI}=10V; (c) V_g=0V, V_{PI}=3V, (d) V_g=2.5V, V_{PI}=6.1V (e) V_g=5V, V_{PI}=6.2V.

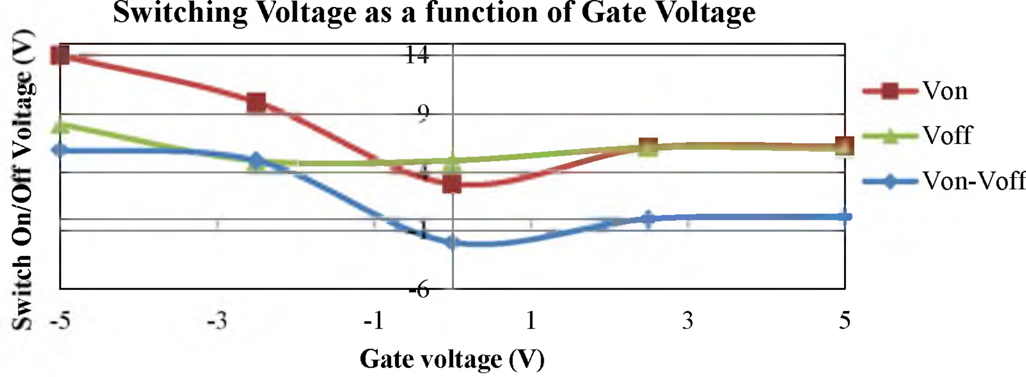


Figure 6.4: Graph illustrating switching voltage a function of gate voltage

6.1.2. MEMS Switches for Efficient Power Management in Scaled CMOS

Since 2003, the industry's approach has addressed device power efficiency improvements on the circuit level such that significant circuit modification and performance overhead for leakage reduction was introduced [8]. Apart from using ultra-low leakage switches, as described in this thesis, there is a strong need today for ultra-low-leakage power management technology on scaled VLSI devices.

Here, a simple cross-bar geometry is discussed, as shown in Fig. 6.5(a), that can be easily fabricated at low temperature (<30°C) at the interconnect levels of a typical VLSI processes.

These devices were fabricated using a simple 2-mask process using sputtered platinum at 50W at <2µtorr pressures. The final released devices are illustrated in Fig. 6.5(b) and (c), emphasizing the ON and OFF states that are clearly visible via change in transmission when observed through a microscope-mounted camera. The fabrication process is outlined in Fig. 6.6.

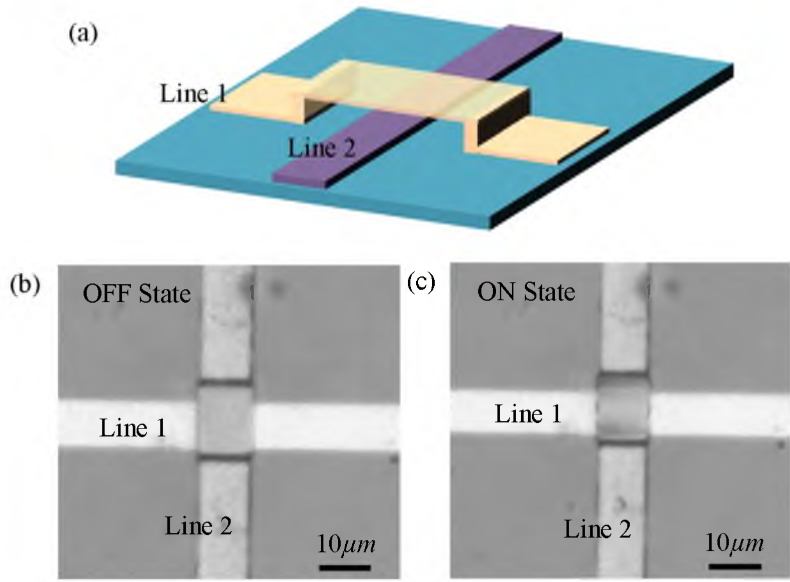


Figure 6.5: BEOL process compatible cross-bar Pt switches shown in (a) 3D rendering; optical image of (b) OFF, state and (c) ON (pulled-in) state.

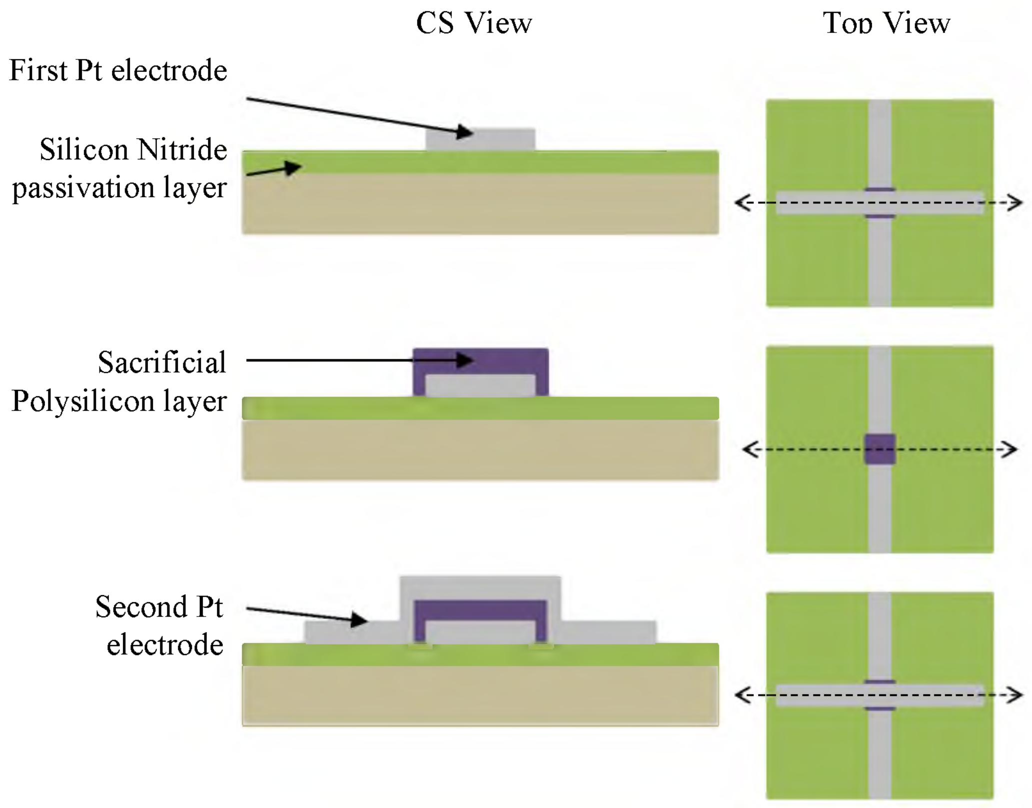


Figure 6.6: Fabrication process outline

Calculations on design were based on ANSYS simulation results and revealed the trend illustrated in Fig. 6.7 for pull-in voltage vs. gap height. From measurement on actual devices, it was seen that devices with 100 nm gaps were found to switch at just under 2 V, as seen in Fig 6.8. Other devices with larger gaps (500 nm) were tested for reliability and illustrated >1270 cycles of operation in ambient lab environment (Fig. 6.9). Under more stringent/controlled environments, such as vacuum back-filled with N_2, the 'catalytic' effects of Pt combined with O_2 can be minimized to enhance reliability. The measured contact resistance in the ON state was on the order of 10's mΩ. The design of these simple switches for use as interconnects for FPGAs are also illustrated here in Fig. 6.10.

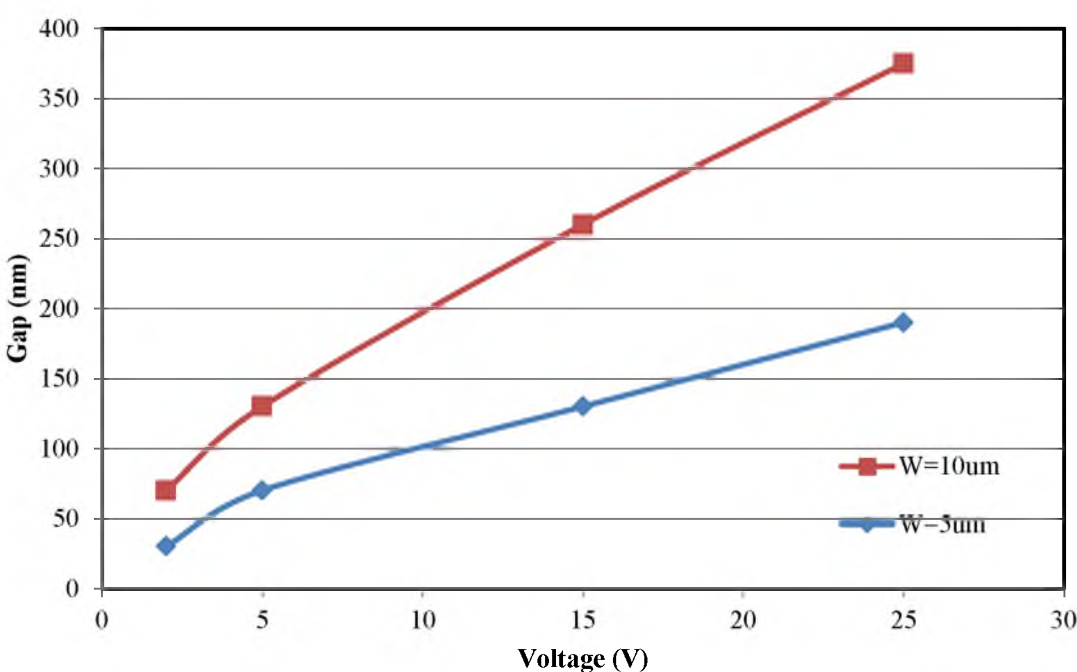


Figure 6.7: Design calculations on pull down voltage and gap height based on ANSYS simulations on beams having active switching areas of 10µm x 10µm and 5µm x 5µm.

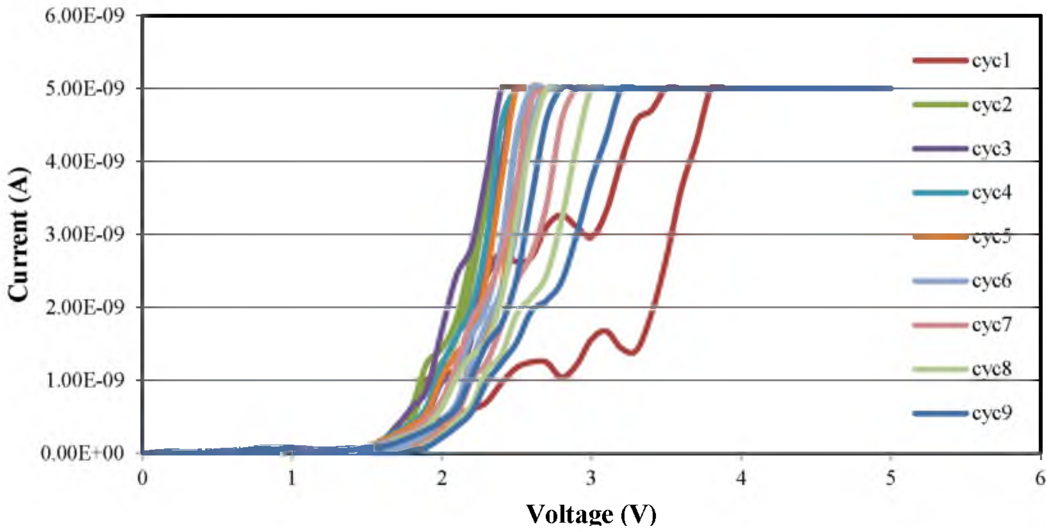


Figure 6.8: I-V Cycling measurements on 100nm gap devices. V_{PI}~2V.

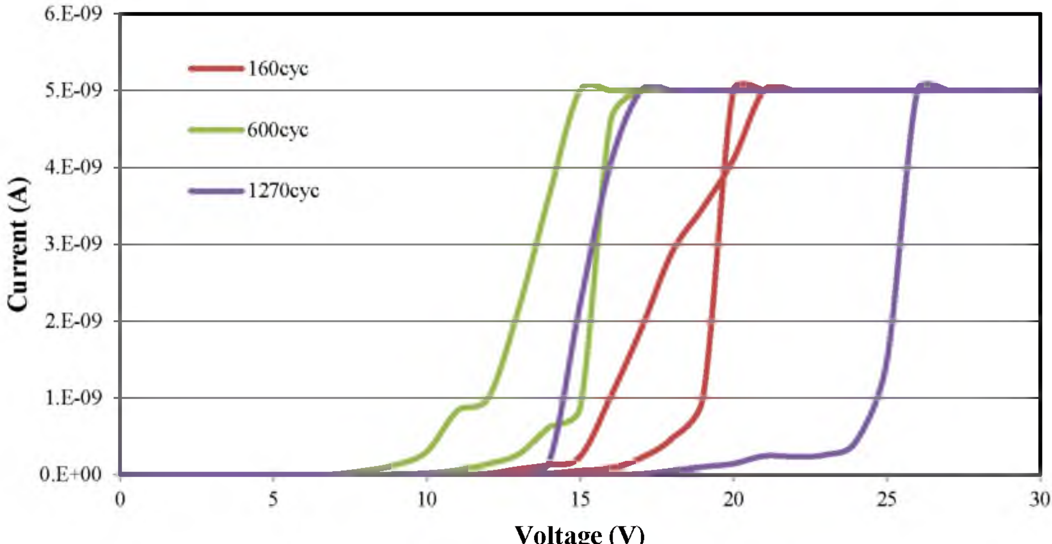


Figure 6.9: Prolonged I-V measurements on 500nm gap Pt switches. Switches worked >1270 cycles. Steady VPI~15V.

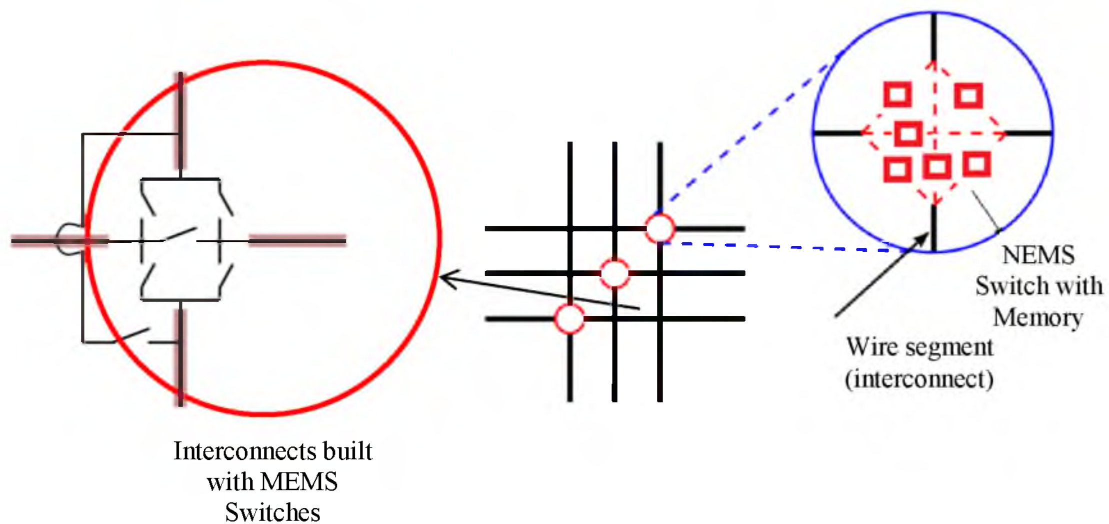


Figure 6.10: Schematic illustrating interconnect setup for FPGAs using MEMS cross-bar structures.

6.1.3. MEMS Circuit Design

Simple electro-mechanical circuits were designed and fabricated using a fabrication flow that was slightly modified to incorporate boron-doped polysilicon resistors to enable functional circuits. Some examples of these are given in Fig. 6.11, which shows optical images of a 1-bit multiplexer chip built utilizing 4 AND gates, a 1-bit adder chip built using 3 XOR and 2 AND gates, and a multiplier circuit utilizing 6 XOR and 4 AND gates. These represent the first steps towards developing more complex circuits, microcontrollers, and eventually mini-computers capable of ultra-low power computation in the age of the "Internet of Things" enabling the More than Moore's law era.

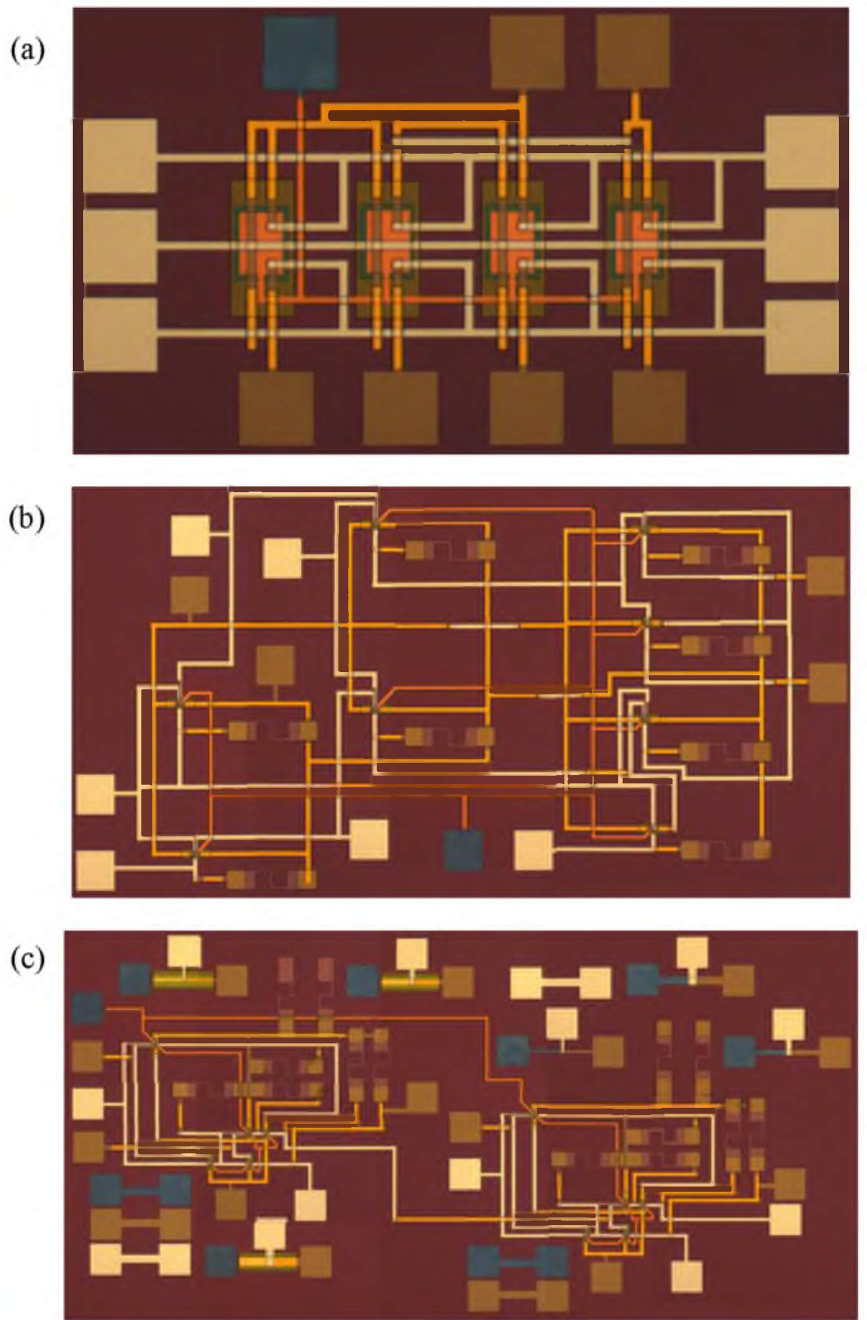


Figure 6.11: MEMS circuits fabricated using single-device XOR and AND gates. a) 2-bit multiplexer, b) 1-bit full adder, and c) multiplier circuit.

6.2. Summary

This chapter presented the development of next-generation field-assisted MEMS logic gates for *in-situ* pull-in voltage compensation/control usually applicable in harsh environments using a unique method of introducing electrets using ALD SiO_2-Al_2O_3 deposition. Also discussed here are MEMS switches for efficient power management that can be integrated easily at low temperature with BEOL VLSI processes, and development of simple functional circuits designed and fabricated using single-device MEMS logic gates (XOR and AND).

6.3. References

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CHAPTER 7

CONCLUSIONS

This thesis discusses novel single-device MEMS-based logic gates, such as XOR and AND, for ultra-low leakage computation and for harsh environment usage such as those in high ionizing radiation and high temperatures.

The functional MEMS/NEMS structures operate as logic gates in a single device instead of using individual switches commonly employed in CMOS. Given that 6–14 CMOS switches are typically needed in logic gates, the functional structures reduce the device count leading to better reliability, yield, speed, and overall better characteristics (subthreshold characteristics, smaller turn-on/off voltage variations, etc.). The theoretical considerations, design, fabrication, and characterization and analysis of XOR and AND gates as specific examples of single-device logic functions were discussed. The results showed a ~1–2 V pull-down voltage, less than 1μW leakage power consumption, and reliable switching lifetime greater than 10^9 cycles.

An intensive study on the evolution of contact resistance of nine disparate, yet commonly used, contact electrode materials (Ir, Pt, W, Ni, Cr, Ti, Cu, Al, and graphite) were investigated on a cycle-by-cycle basis using a special AFM setup, up to 100,000 cycles. The investigation revealed that the initial contact resistance (R_c) of Ir, W, Pt, Cu, Al, Ti, and graphite was low (10^6-10^7 Ω) compared to other metals (Ni~10^{11}Ω and

Cr~$10^{12}\Omega$), which evolved to much higher values (>$10^{11}\Omega$) over the course of 100,000 cycles of operation, in nearly all cases. However, an anomaly was seen in the case of Ti, which remained fairly conductive throughout (~$10^{7}\Omega$). This was attributed to its conducting TiO_2 formation. The only nonmetal experimented with was graphite and it yielded the most reliable electrical performance by revealing the least deterioration over the testing period. Additionally, by using a separate adhesion-force measurement AFM setup, a relationship between contact resistance evolution and measured adhesion forces was seen where materials with high Young's modulus, high melting temperatures, and high hardness indicated low adhesion forces (such as Ir, Pt, and W). The study concludes that the best electrode materials (in terms of minimally deteriorating contact resistances) to choose from are generally W, Pt, Ir, Ti, and graphite; however, the ultimate choice is usually influenced by other device requirements and compatibility issues.

Furthermore, the fabricated single-device logic gates were interrogated for harsh environment operation at elevated temperatures (409 K) and high ionizing radiation environment (90 kW for 120min in a nuclear reactor). Both experiments showed successful and reliable operation of these MEMS devices compared to silicon MOSFETs.

Finally, additional work on charged-electret based scaled MEMS switches were presented that relied on a unique ALD SiO_2-Al_2O_3 deposition technique that enabled field-assisted *in-situ* pull-in voltage compensation for MEMS in harsh environments. Also, a simple Pt-based cross-bar structure that can be used for efficient power management integrated with BEOL VLSI processes at low temperatures was discussed. Finally, micro-fabricated circuits, such as, multiplexers, 1-bit full adder, and a 2-bit full adder that employ the XOR and AND gates were also discussed.