Quantifying Device Degradation in Live Power Converters Using SSTDR Assisted Impedance Matrix

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***Abstract*—A noninterfering measurement technique designed around spread spectrum time domain reflectometry (SSTDR) has been proposed in this paper to identify the level of aging associated with power semiconductor switches inside a live converter circuit. Power MOSFETs are one of the most age-sensitive components in power converter circuits, and this paper demonstrates how SSTDR can be used to determine the characteristic degradation of the switching MOSFETs used in various power converters. An SSTDR technique was applied to determine the aging in power MOSFETs, while they remained energized in live circuits. In addition, SSTDR was applied to various test nodes of an H-bridge ac–ac converter, and multiple impedance matrices were created based on the measured reflections. An error minimization technique has been developed to locate and determine the origin and amount of aging in this circuit, and this technique provides key information about the level of aging associated to the components of interest. By conducting component level failure analysis, the overall reliability of an H-bridge ac–ac converter has been derived and incorporated in this paper.**

***Index Terms*—Aging, converter, degradation, failure rate, matrix, mean time to failure (MTTF), reflectometry, reliability, spread spectrum time domain reflectometry (SSTDR).**

I. Introduction

POWER converter circuits have a wide range of applications, and ceaseless operation of these converters is imperative in most cases. However, these converters may be exposed to stressful environments, i.e., over voltage, over current, high temperature, or switching impulses during regular operations and these external forces may result in severe degradation or complete failure of critical components inside a converter. Over longer periods, these conditions coupled with various environmental factors such as mechanical vibration, radiation, and thermal cycling may lead to catastrophic failure of converter components. A failure survey of various components in a power converter shown in Fig. 1 [1] clearly demonstrates that electrolytic capacitors and MOSFETs are the most age-affected components in power converter circuits. The photographs of some actual damaged MOSFET and electrolytic capacitor are given in Fig. 2.

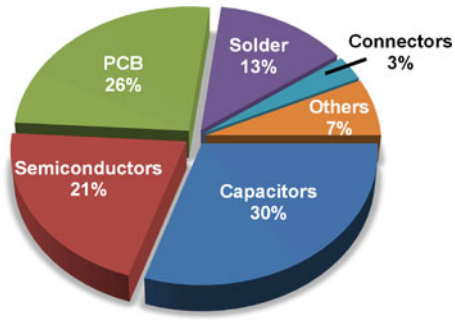

Fig. 1. Failure survey of different components responsible for converter failure [1].

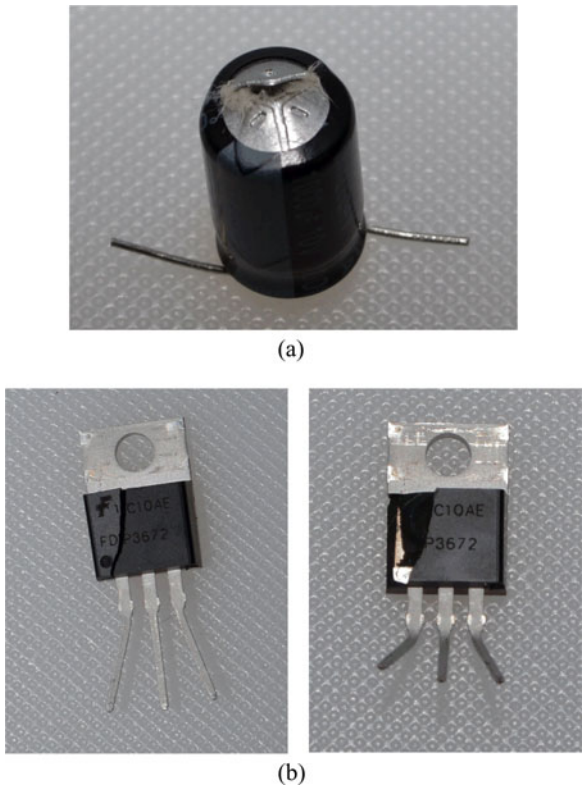

Fig. 2. (a) Damaged electrolytic capacitor (failed at high voltage) and (b) damaged MOSFET (failure caused by high voltage applied across drain and source).

Component parameters such as ON-resistance and switching characteristics of MOSFETs/IGBTs, and equivalent series resistance (ESR) of capacitors degrade with time, and the

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accumulated aging eventually leads to deterioration of several operating characteristics of a power converter such as output voltage ripple, switching loss, conduction loss, etc. [2]–[4]. Therefore, the aging profile, i.e., the state of health of the entire power converter could be obtained by studying the component level aging although the level of aging associated to any component is difficult to calculate because multiple components are interconnected in a converter circuit. Therefore, two hurdles need to be crossed—the component level aging needs to be identified with reasonable precision; and a converter specific model needs to be derived that could be used to predict the overall reliability of the converter based on component level aging.

This situation is even more challenging when components need to be characterized while they are energized in a live converter, and conventional measurement techniques could not be used with ease. Moreover, it is of paramount importance to identify which component parameters to look for. In this regard spread spectrum time domain reflectometry (SSTDR) can be used to measure impedance discontinuity in various current paths in a live converter circuit. As an added feature, several faults inside the circuit can be identified without interrupting the circuit's normal operation although the discussion on this capability of SSTDR (fault detection) is beyond the scope of this paper. Authors' previous work demonstrated how SSTDR can be applied to identify degradation in MOSFETs, IGBTs, and electrolytic capacitors [5]. Once the component level analysis was done, authors are particularly interested in the reliability estimation of a converter circuit using the SSTDR generated data.

This paper demonstrates that major parameters of power MOSFETs exhibit measurable changes over time in a real converter circuit, and SSTDR can be effectively used to measure these changes. These SSTDR generated data can be manipulated to calculate the ON resistance $(R_{\mathrm{DS(ON)}})$ of the switches which clearly reflects the adverse effect of aging. In addition, this paper also illustrates how SSTDR technique can be applied to: *1) detect the physical location of any aged MOSFET in a circuit; 2) measure the corresponding aging level of various MOSFETs inside an H-bridge ac–ac converter circuit; and 3) use these data for the reliability analysis of the H-bridge converter with a single-aged MOSFET.*

This paper is organized in the following manner. Section II describes the origin of power MOSFET failure and the existing state-of-the-art solutions to determine the measurable physical parameters quantifying the level of aging and the comparison of SSTDR with other existing real-time methods. Section III demonstrates the proposed approach which includes fundamentals of SSTDR operation and uniqueness of SSTDR compared to other techniques. Section IV presents the experimental results for estimating degradation in MOSFETs using SSTDR. Experimental SSTDR generated results for an H-bridge ac-ac converter has been included in Section V. Impedance matrix-based analysis applied to the H-bridge converter using the SSTDR generated data has been discussed in Section VI. Reliability analysis of the H-bridge converter has been presented in Section VII, and the summary has been presented in Section VIII.

II. Origin of Degradation in Power Semiconductor Devices

The prediction of converter's state of health as well as estimation of remaining life are extremely challenging tasks and involve extensive research in semiconductor device physics and circuit theory. Therefore, this ongoing research has identified four major layers of activities to conduct this prediction analysis. **Layer 1**: *identifying the origin of microscopic failures in components*; **layer 2**: *identifying the translated measurable quantities—how these microscopic changes are converted into changes in physical device parameters*; **layer 3**: *improving and ultimately customizing the SSTDR system to take these measurements and obtain three key aspects—impedance, location, and phase*; **layer 4**: *optimizing the mathematical model to estimate the state of health*. Research labs such as NREL and NASA, and commercial enterprise such as Siemens are working on layer 1 while this project aims to solve problems involved in the remaining layers.

One of the most failure prone components in a power converter is the power MOSFET. In order to conduct a failure study and predict the remaining life of the components as well as the entire power converter, the origin of component failure should be studied first. Therefore, the origin of these failures and previous work on the identification of the shifted measurable quantities induced by the degradation of power MOSFETs are described in the following section. In this regard, failure of semiconductor devices can be categorized into two groups: 1) chip-related failures and 2) packaging-related failures [6].

The reasons for chip-related failures are electrical overstress, electrostatic discharge, latch up, charge effects, and radiation effects [6]. The combined effect of high voltage and high current lead to electrical overstress, and under high-voltage conditions, overheating can be crucial and may cause secondary breakdown. The abrupt losses of gate oxide in MOS devices occur due to such breakdown. In this continuation, drain current decreases and gate leakage current increases after the breakdown [1]. The gate terminal of MOSFETs can also be affected by electrostatic discharge (ESD). The effect of electrical stress at the gate area was studied in [7] and [8] by applying a high voltage at the gate terminal. It was also found that the threshold voltage V_{th} increases with aging, and an increase in the threshold voltage directly results in an increase in switching time causing additional switching loss. Usually, the threshold voltage deviates from the standard value because any degradation in the gate oxide region and at the interface between the gate oxide and channel, and the rate of degradation depends on the thickness of the gate oxide. If a very high positive voltage is applied at the gate terminal or a very high negative voltage is applied at the drain terminal of an N-channel MOSFET, hot carriers are generated in the silicon substrate. However, the amount of shift in threshold voltage (ΔV_{th}) gradually decreases when an overvoltage stress is applied repeatedly [9]. Due to the very high kinetic energy of these carriers, they can move around or get trapped in the oxide region or at the Si–oxide interface. As a result of the repetitive application of positive-voltage stress, increased numbers of acceptor

ions move towards the surface and create a nonlinear energy distribution. This is the reason for nonlinearity in $\Delta V_{\rm th}$.

This shift in the threshold voltage is negative when a negative stress is applied at the gate terminal. In an N-channel MOSFET, when threshold voltage is increased over cumulative stress, the gate to source capacitance $C_{\rm gs}$ decreases, and the gate to drain capacitance $C_{\rm gd}$ increases [9]. Rapid increase in the applied drain-source voltage of a MOSFET may cause an undesirable triggering of the parasitic elements (the bipolar transistor in the MOSFET structure). In this regard, the authors [10] presented an accelerated aging procedure by applying both high power and constant thermal stress. In this paper [10], the drain current was allowed to increase with sufficient thermal stress, and the device failed to turn OFF at some point in spite of a zero gate voltage applied. Moreover, a sudden increase in package temperature indicates thermal runaway of the device. This phenomenon indicates the loss of gate control, and the ON-state resistance $(R_{\rm DS(ON)})$ exhibits a sudden drop due to elevated drain current. Therefore, higher $R_{\rm DS(ON)}$ is consistent with aging, and a sudden drop in the value of $R_{\rm DS(ON)}$ is an indicator of the loss of gate control.

In power MOSFETs, carrier injection and ionic contamination result in the change of threshold voltage, leakage current, and transconductance which eventually accelerate the breakdown process. The power semiconductor switches in space environments suffer from significant charge build up within the oxide and insulators due to the radiation effects, and this induced charge is responsible for any shift in the threshold voltage [11]. Oxide-trapped charge is positive for both P- and N- channel transistors. However, interface-trapped charge is negative for an N-channel transistor which causes positive shift in the threshold voltage; whereas interface-trapped charge is positive for a P-channel transistor which causes negative shift in the threshold voltage. Any shift in the threshold voltage increases the leakage current which leads to device failure.

The main reason for packaging-related failures is the dissimilarity between the coefficients of thermal expansion (CTE) of the chip and the package. These types of failures are bond failures and die solder layer failure. Bond failure is mainly caused by any crack growth at the bond wire/chip interface due to the difference of CTEs of Si and Al [12]. $R_{\rm DS(ON)}$ of a MOSFET increases due to the degradation at metallization and at the contact area of bonding wire metallization [13]. The authors in [14] also concluded that $R_{\rm DS(ON)}$ increases due to thermal aging, and intermetallic growth and Kirkendall voids formation at the bond–pad interface at higher temperature were studied in this paper. Fig. 3 provides the graphical presentation of crack and void formations inside a power MOSFET.

According to [15], $R_{\rm DS(ON)}$ is found to be the most significant aging factor in power MOSFETs. Die solder layer failures are related to the formation of initial solder microstructure, substrate metallization, intermetallic compounds, and cracks. These voids increase the thermal impedance, resulting in higher temperature fluctuations within the semiconductor device. The thermal impedance can be determined from the junction temperature of the device, and [16] described a technique which uses $R_{\rm DS(ON)}$ of the device to determine the junction temperature.

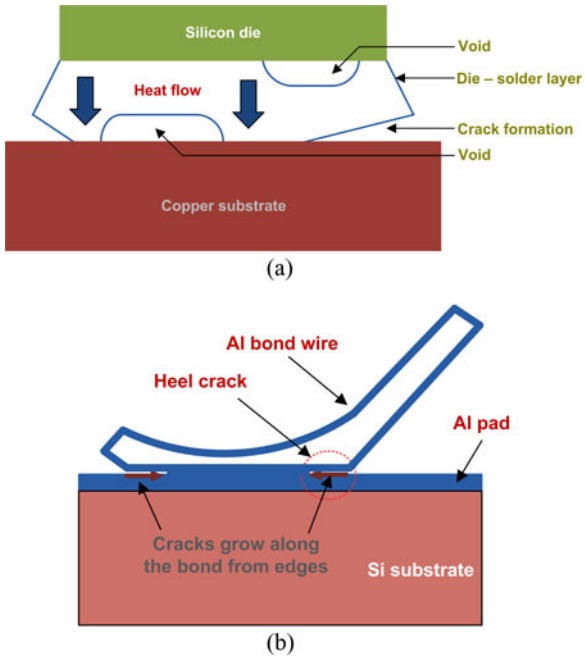

Fig. 3. (a) Origination of cracks and voids in a power MOSFET due to aging and (b) wire bonding failure.

Die solder degradation has been studied in [17] and [18] by applying thermal stress to the device, and $R_{\rm DS(ON)}$ increased due to the degradation. Therefore, the change in $R_{\rm DS(ON)}$ is considered a precursor to failure due to its strong correlation with junction temperature. Variation in $R_{\rm DS(ON)}$ can only be related to the formation of cracks and voids in the source metal layer according to [19]. Therefore, the aging factors associated with MOSFETs are 1) ON-resistance; 2) threshold voltage; and 3) various capacitors in the MOSFET equivalent circuit. However, from the existing literature study, it can be stated that the $R_{\rm DS(ON)}$ is the most significant aging factor in MOS devices and the novelty in any measurement technique lies in how accurately and conveniently this $R_{\rm DS(ON)}$ can be measured, especially when the device is energized. The proposed SSTDR method generates results depending on the impedance variation of the device under test, and it can be applied to differentiate new and aged MOSFETs based on the variation in $R_{\rm DS(ON)}$.

Multiple MOSFETs connected in parallel have become a prevalent trend in recent days. Nonuniform degradation among parallel MOSFETs is found in [20] due to high current stress, and variation in current distribution was observed in parallel MOSFETs as well. This imbalance is further aggravated with: 1) increased $R_{\rm DS(ON)}$ during thermal stress; 2) increased effect of conductance path mismatch during current stress; and 3) increased effect of thermal path difference during thermal stress.

Other than the MOSFET, the key measurable quantities to estimate the aging in individual components are—capacitor ESR and capacitance, V_{CE} of IGBTs, and gate characteristics of IGBTs [5]. The authors believe that there exist other measurable quantities that could be used to estimate aging in components, and the ongoing research and the collaboration with Sandia

National Lab should provide the necessary information to identify those quantities.

There exist several real-time methods to estimate the state of health of power converters. The following section presents the uniqueness of the proposed method with conventional device characterization techniques. The authors in [21] proposed a real-time monitoring of capacitor ESR based on the power dissipation across the capacitor and the capacitor current. The capacitor voltage and currents are continuously monitored to determine power dissipation. An online monitoring method was presented in [22] which measures the junction temperature of power devices in a voltage source inverter, and this temperature was found directly related to the operating states of the inverter. Online fault diagnosis methods in power electronic drives were described in [23] by measuring capacitor ESR, MOSFET $R_{\mathrm{DS(ON)}}$, and $V_{\mathrm{CE(sat)}}$ of IGBT. ESR was calculated from the capacitor voltage and current, and $R_{\mathrm{DS(ON)}}$ was calculated from the corresponding ripple voltage and ripple current of the MOSFET. The measurements of V_{CE} were taken to identify degradation of IGBTs, and it is imperative that all these measurement techniques require multiple sensors, and interrupting the circuit's normal operation may be necessary.

Monitoring solder joint fatigue in power modules using the case above ambient temperature (CAAT) was proposed in [24]. The CAAT was measured using a two-channel thermometer (FLUKE-1524), and the module power loss was calculated using this recorded temperature. Power loss is directly related to temperature, which depends on thermal resistance (R_{th}) and R_{th} is an indicator of aging. Another online fault diagnosis technique in dc—dc converters was proposed in [25] by calculating the ESR of the dc bus capacitor. ESR was calculated from the input current and output voltage ripple of the converter. In [18], $R_{\mathrm{DS(ON)}}$ of power MOSFETs was calculated as the ratio of the drain-source voltage (V_{DS}) and drain current I_D during on-state. The authors in [26] proposed an online diagnosis method considering the variation in parasitic/internal resistance of components in a dc–dc converter. However, this diagnosis method is applicable to diagnose the entire system, not individual components.

The authors in [46]–[49] presented several fault detection techniques which are primarily suitable to diagnose a specific component in the system. From the literature study presented in the previous section, it is apparent that some of the existing online methods are based on identification of individual component degradation, and the real-time techniques are based on identification of the overall system's performance. The techniques based on individual device degradation are particularly suitable to locate degradation in any specific type of component, i.e., electrolytic capacitors or MOSFETs or IGBTs, and at least two measurements are required to collect voltage and current. On the other hand, the methods intended for prediction of the overall circuit's degradation are unable to locate the aged components. Therefore, there is an imminent need to develop a real-time method which can identify the aged components as well as predict the overall system performance based on the aged devices. The aim of the proposed technique is to identify the origin of component-level degradation, level of aging, and thus predict the overall system's reliability using mathematical analysis based on obtained experimental data.

III. Proposed Methodology for Parameter Extrction

SSTDR has been used in this project to extract different component parameters in a live power converter. Most of the conventional techniques estimate converter's reliability by measuring individual components' characteristics while they are disconnected from the circuit. Even though they are characterized in real time, results obtained by characterizing individual components cannot be applied for the prediction of overall converter reliability. In order to overcome this limitation, SSTDR has been used to obtain several parameters of the individual components as well as the converter circuit. Reflectometry is conventionally used for locating wiring faults, and the authors in [27]–[33] presented several reflectometry techniques to identify aircraft wiring faults and aging.

A. Fundamentals of SSTDR

In reflectometry, a high-frequency electrical signal is sent down the wire, and it reflects from any impedance discontinuity. The reflection co-efficient gives a measure of how much signal is returned and is given by ρ

$$\rho = \frac{Z_t - Z_o}{Z_t + Z_o} \tag{1}$$

where Z_0 is the characteristic impedance of the transmission line and Z_t is the impedance connected at the terminating end of the transmission line. The time or phase delay between the incident and reflected signals provides the distance to the fault, and the observed magnitude of the reflection co-efficient provides the impedance at discontinuity. It has been discussed in the previous sections how the measurable electrical attributes of power MOSFETs used in a power converter can be determined to characterize the aging associated to that converter. As the aging of MOSFETs is directly related to the impedance variation, reflectometry can be used to identify the gradual changes in the impedance of a power MOSFET by comparing the results obtained from a reference unstressed MOSFET impedance values consistent with a new converter.

Time domain reflectometry (TDR) sends a step voltage from the source end, and this method was used in [34] to measure the parasitic parameters of printed circuit boards (PCB). Zhu *et al.* [35] presented the characterization of interconnect parasitics in the switching power converters using TDR. In addition, TDR was used in [36] and [37] to detect two interconnect failures: solder joint cracking and solder pad separation. The techniques for prognostic solder joint degradation using TDR has been discussed in [38]. The capacitance of a pad in CMOS process was estimated using an "on wafer" TDR measurement system in [39], and the method of extracting series resistance of capacitors using TDR was presented in [40]. The major limitation of TDR is the higher cost compared to other techniques and limited performance in live networks. In order to overcome the limitations of TDR, SSTDR has been used to estimate the state of health of power semiconductor switches and electrolytic

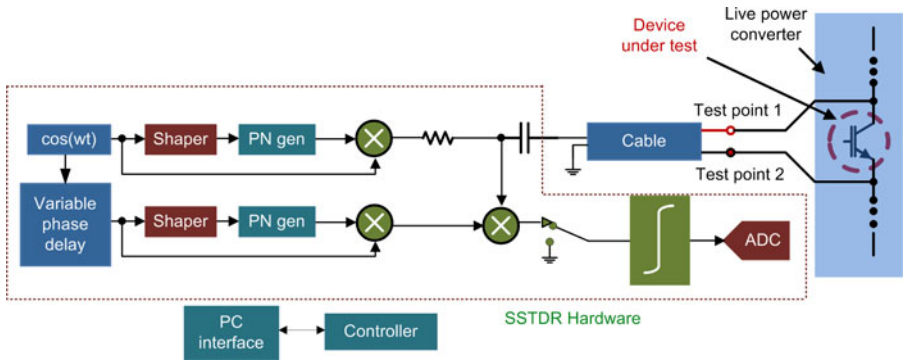

Fig. 4. Block diagram of the SSTDR test system [31].

capacitors. SSTDR uses a sine wave modulated pseudonoise (PN) code as the test signal. SSTDR has already been commercially used for locating faults in aircraft wires [31] as well.

B. SSTDR Operation

A block diagram of SSTDR setup is shown in Fig. 4. A sine wave generator (operating at 30–100 MHz) is used as master system clock, and this generator's output is converted to a square wave via a shaper, and the resulting square wave drives a pseudonoise digital sequence generator (PN gen). The sine wave is multiplied by the output of the PN generator in the SSTDR setup, and the test signal is injected into the cable. The other end of the cable is connected across the device under test. The reflected signal from the cable (including any digital data or ac signals in the cable, and any reflections observable at the receiver) are fed to a correlation circuit along with the reference signal. Inside the correlation, the received signal and the reference signal are multiplied, and the result is fed to an integrator. The output of the integrator is sampled with an analog-to-digital converter (ADC). A full correlation can be collected by repeatedly increasing the phase delay using the variable phase delay unit and acquiring the correlated output using the ADC. The location of the various peaks (either positive or negative) in the full correlation indicates the location of impedance discontinuities such as open circuits, short circuits, and arcs (intermittent shorts).

C. Test Setup Details

The schematic of the test setup to find the correlated output using SSTDR is shown in Fig. 5. Multiple MOSFETs were aged for different time durations and were characterized using the SSTDR system. An ADAM 5000 (data acquisition system) was used to continuously monitor and record the drain to source voltage V_{DS} of the MOSFETs under test and the voltage across the series resistance R_{Lim}. The voltage across R_{Lim} was measured to determine the drain current of the MOSFET, and the $R_{\mathrm{DS(ON)}}$ of the test MOSFETs were calculated from V_{DS} and I_{DS} (drain current). A dc–dc converter circuit shown in Fig. 5(a) was considered to test the MOSFETs using the SSTDR method. A commercial SSTDR hardware from Livewire Innovation was interfaced with a desktop computer to operate the hardware and monitor the correlated output [41].

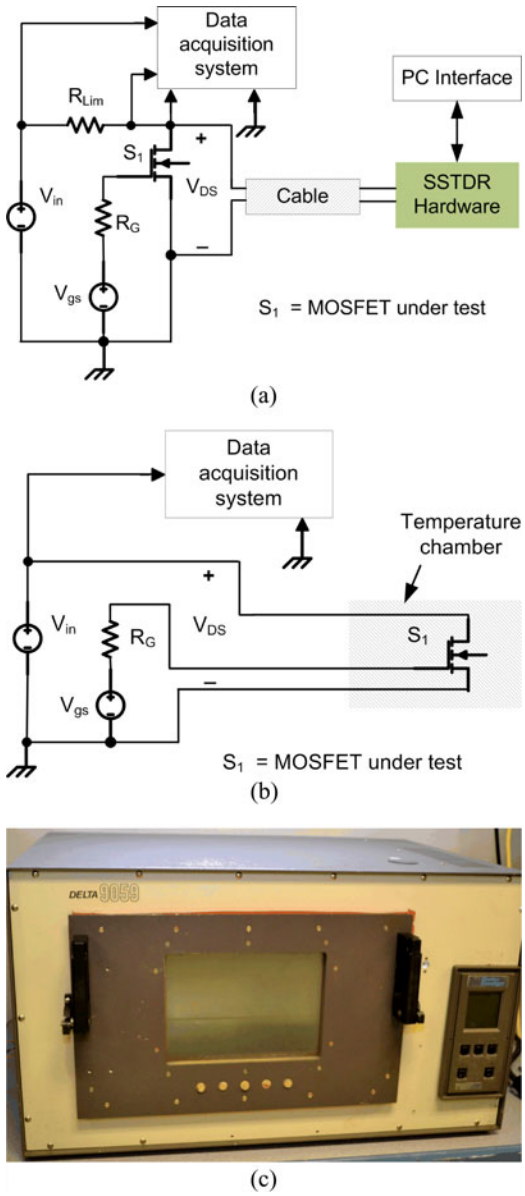

Fig. 5. (a) SSTDR test setup to characterize MOSFET's $R_{\mathrm{DS(ON)}}$—supported by the data acquisition system, (b) experimental setup used for quantifying the accelerated aging of the MOSFETs, and (c) temperature chamber used to stress the devices.

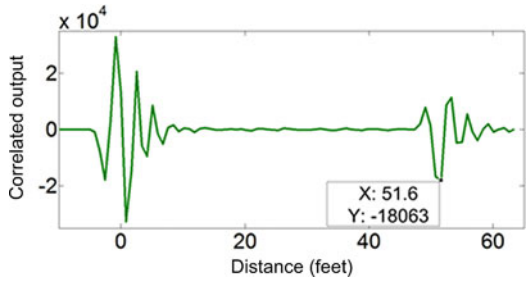

Fig. 6. Typical SSTDR generated plot across a 13-Ω carbon film resistor.

A typical SSTDR generated plot across a 13-Ω carbon film resistor is shown in Fig. 6. The SSTDR hardware generates autocorrelation plots for various frequencies (96, 48, 24, 12 MHz) sent from the PN signal generator, and the exact peak value of the correlated outputs varies with the frequency. The plot shown in Fig. 6 is generated for 96 MHz frequency. From the conducted tests, it was found that the SSTDR data generated at 24 and 48 MHz exhibit the best performance in determining $R_{\mathrm{DS(ON)}}$ of the MOSFETs under test.

A 54 ft 75-Ω (RG 59) coax cable was connected in between the dc–dc converter circuit and the SSTDR test system while SSTDR was applied across drain-source terminals of MOSFETs. Because of the uniform impedance of the coax cable over the entire length, a peak in correlated output was observed only at the starting point (due to the impedance mismatch between the SSTDR hardware and the coax cable) and at the end terminal of the cable (due to the impedance mismatch between the coax cable and the devices under test). The amplitude of the peak is dependent on the value of the ON-state resistance of the MOSFET under test. Once the individual characterization was performed, MOSFETs in an H-bridge ac–ac converter circuit were characterized.

The detailed experimental setup of the aging procedure and the application of SSTDR are described in the following sections.

IV. Experimental Results for Estimating MOSFET Degradation Using SSTDR

A. Characterizing the Aging of Power MOSFETs as a Function of Time

Multiple power MOSFETs were aged using power and temperature stress in a controlled environment. 1-V dc voltage V_{DS} was applied across the drain-source terminals of FDP 3672 N-channel power MOSFETs to apply power stress, and these MOSFETs were placed in a controlled temperature chamber at 110 °C using a Delta 9059 environment chamber [see Fig. 5(c)]. A constant current and constant temperature stress were applied to make the devices aged although temperature cycling is the most conventional method for device compared to aging with constant temperature. It was conducted in this way because the main purpose of this research was to verify if the recorded SSTDR data were consistent with the variation in device parameters such $R_{\mathrm{DS(ON)}}$. The gate-source voltage was 12 V, and R_{Lim} was removed ($R_{\mathrm{Lim}} = 0$) during the accelerated aging procedure. Due to the high power dissipation (∼8 W) in each MOSFET, the case temperature reached 170 °C within 10 min which was stabilized between 160 °C and 170 °C during the entire accelerated aging process. The aforementioned procedure was applied to four different MOSFETs M2, M3, M4, and M5, and their initial $R_{\mathrm{DS(ON)}}$ were approximately equal (33–34 mΩ). M1 was used as the reference MOSFET as zero stress was applied to it. These stressed MOSFETs were cooled down to room temperature after accelerated aging, and the $R_{\mathrm{DS(ON)}}$ were measured using the setup shown in Fig. 5(a). The gate voltage was set to 5 V, and the value R_{Lim} was selected as 5 Ω while taking the measurements of $R_{\mathrm{DS(ON)}}$ using the data acquisition system. A noticeable permanent increase in $R_{\mathrm{DS(ON)}}$ was obtained after aging which was 2–10 mΩ for these MOSFETs under test. Calculated $R_{\mathrm{DS(ON)}}$ from the data acquisition system and the peak amplitude of the correlated output at the far end of the cable found in SSTDR test system (see Fig. 7) for M1–M5 are shown in Table I.

SSTDR was applied to all five MOSFETs (M1 – M5) in order to compare the characteristics of M1 with the aged MOSFETs. Data from SSTDR test system were extracted into MATLAB, and the correlated outputs versus. distance characteristics are shown in Fig. 7. The correlated amplitude is the true measure of the reflected power, and the reflected power is a function of the impedance at the far end of the cable. If correlated waveform is normalized to the highest peak in the data, all amplitudes would be a fractional number between –1.0 to +1.0.

From the difference in correlated output (see Fig. 8) at the far end of the cable, it was found that the difference in $R_{\mathrm{DS(ON)}}$ values for M1 and M5 were the highest, and the corresponding difference in reflection co-efficient (SSTDR generated correlated output) were the highest as well. A similar phenomenon was observed for M3 and M4 where the difference in their $R_{\mathrm{DS(ON)}}$ was the lowest. The SSTDR hardware generates several sampled values of correlated outputs along the coax cable, and because the MOSFETs were connected at end terminals of the cable, the peak value of correlated amplitude at this point (∼ 54 feet) is different for various MOSFETs under test. These differences were calculated by subtracting the correlated amplitudes of one MOSFET from another MOSFET. The difference in correlated peak was 93 when difference in $R_{\mathrm{DS(ON)}}$ was 10.39 mΩ, and the difference in correlated peak was 6 when difference in $R_{\mathrm{DS(ON)}}$ was 0.01 mΩ. Therefore, if the values of $R_{\mathrm{DS(ON)}}$ are nearly equal, the SSTDR hardware generates similar or approximately equal values of correlated output. The best accuracy of the SSTDR hardware used in test was in the range of 1–2 mΩ, and this will be shown later.

Using the experimental results, the variation in $R_{\mathrm{DS(ON)}}$ can be predicted from the variation in the amplitude of the correlated outputs. Because the value of the $R_{\mathrm{DS(ON)}}$ is directly related to the state of health of power MOSFETs, the variation in correlated output is a true representation of the MOSFET aging. The calculations of $R_{\mathrm{DS(ON)}}$ from the SSTDR-generated peak correlated outputs are discussed in later sections.

B. Mapping Device Characteristics as a Function of Aging

The failure threshold can be considered as 25% increase in $R_{\mathrm{DS(ON)}}$ for power MOSFETs [17]. Failure threshold is

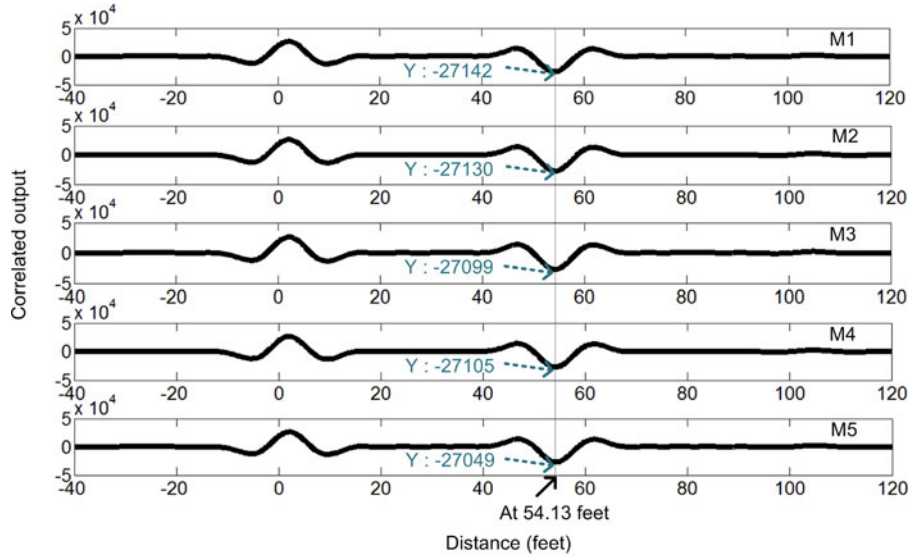

Fig. 7. Correlated output for five different MOSFETs (M1, M2, M3, M4 and M5) with respect to distance.

TABLE I
CORRELATED OUTPUT AND MEASURED $R_{DS(ON)}$ FOR MULTIPLE MOSFETS AGED BY POWER AND TEMPERATURE STRESS

MOSFETs	**M1 [New]**	**M2 [Aged]**	**M3 [Aged]**	**M4 [Aged]**	**M5 [Aged]**
Duration of aging (Minutes)	0	60	120	180	240
$R_{DS(ON)}$ (mΩ) after aging	33.26	35.34	39.57	39.58	43.65
Correlated amplitude	-27142	-27130	-27099	-27105	-27049

TABLE II
CALCULATED AGING LEVEL OF MOSFETS M1, M2, M3, M4 AND M5 USING REFERENCE [17]

MOSFETs	M1	M2	M3	M4	M5
Change in $R_{DS(ON)}$, $\Delta R_{DS(ON)}$ = MOSFET $R_{DS(ON)}$ − initial $R_{DS(ON)}$	0	2.08	6.31	6.32	10.34
Aging level = ($\Delta R_{DS(ON)}$ × 100%) / $\Delta R_{DS(ON)}$ of M5	0%	20%	60.7%	60.8%	100%

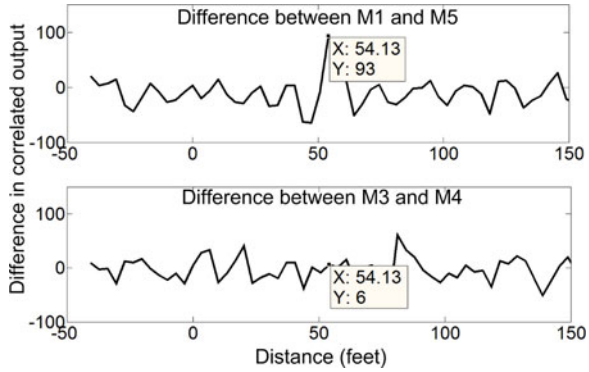

Fig. 8. Differential correlated output associated to various MOSFETs under test.

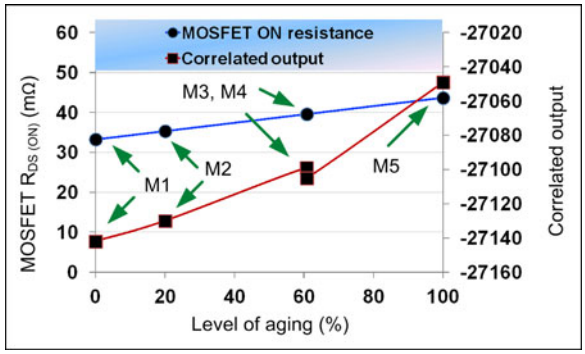

Fig. 9. Variation in MOSFET's $R_{DS(ON)}$ and correlated output as a function of aging.

calculated as the ratio of change in $R_{DS(ON)}$ ($\Delta R_{DS(ON)}$) to the initial $R_{DS(ON)}$. This ratio can be used to measure the approximate aging level of MOSFETs M1 to M5, although it is an arbitrary value. Calculated aging level of M1 to M5 are given in Table II. $\Delta R_{DS(ON)}/R_{DS(ON)}$ in case of M5 is 31.24% which is more than 25%. However, M5 is considered as 100% aged and all MOSFETs' initial $R_{DS(ON)}$ was considered as 33.26 mΩ for simplicity (this initial $R_{DS(ON)}$ value is consistent with the value obtained from the datasheet). Using M1 and M5 as the two extreme boundaries, the level of aging associated to M2, M3, and M4 were calculated. Variation in $R_{DS(ON)}$ and correlated output as a function of level of aging are shown in Fig. 9. This figure also shows that $R_{DS(ON)}$ as well as the correlated output becomes larger with the level of aging. From Table I, M3 and M4 have almost equal values of $R_{DS(ON)}$ which corresponds to ∼60% aging level. However, there is a small variation observed in the correlated output of these two MOSFETs because of the accuracy limit of the SSTDR hardware.

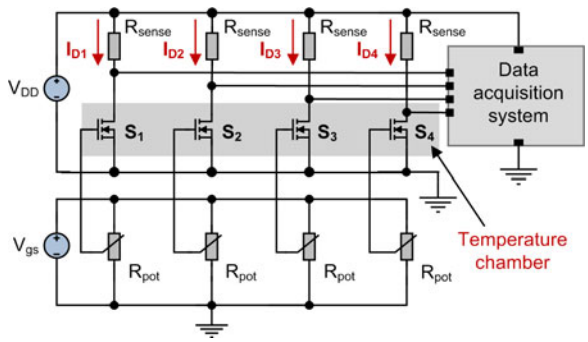

Fig. 10. Schematic of the test setup to conduct accelerated aging of MOSFETs in groups.

C. Identification of Aging and Damage in Power MOSFETs Using SSTDR

Multiple power MOSFETs were aged using both power and thermal overstress in a controlled environment. The main objective of this test was to identify the sample variation from device to device by applying similar stress to a group of MOSFETs. Three groups of MOSFETs were selected with four devices in each group with similar characteristics ($R_{\mathrm{DS(ON)}}$). No stress was applied to one group, one group was aged by moderate power stress, and the third group was aged by extreme power stress. The schematics of the test setup of this group test are shown in Fig. 10.

The value of the current sense resistor R_{sense} was 0.05 Ω, and the power dissipation across each device was calculated, and R_{pot} was initially adjusted to ensure equal power stress across each of these four MOSFETs. 1.46-V dc voltage was applied for moderately accelerated aging of one group of FDP 3672 N-channel power MOSFETs. The power dissipation across each MOSFET was ∼9.417 W, and the surface temperature was stabilized at 200 °C during the period of aging. These devices were aged at 110 °C ambient temperature inside the thermal chamber for 150 min and were cooled down to the room temperature after accelerated aging, and $R_{\mathrm{DS(ON)}}$ were calculated while the MOSFET was connected in a dc–dc converter circuit [test set up of Fig. 5(a)]. It was found that all four MOSFETs in a group had similar rise (∼25%) in $R_{\mathrm{DS(ON)}}$ as a result of this aging. These values of $R_{\mathrm{DS(ON)}}$ before and after aging are given in Table III.

A 1.66-V dc voltage was applied for extremely accelerated aging of one group of MOSFETs and the power dissipation was ∼12.35 W across each of the devices in the group. The surface temperature was ∼245 °C during this extremely accelerated aging procedure, while the ambient temperature was 110 °C. The drain current of the devices dropped to zero after 90 min of aging because of the complete failure of one MOSFET in the group. The failure related to a single MOSFET caused a sudden imbalance in current through the remaining MOSFETs. Therefore, thermal impedance of the devices increased significantly which lead the devices to act like an open circuit and finally drain current of all MOSFET's reached to zero. $R_{\mathrm{DS(ON)}}$ of these devices were calculated after gradually bringing the devices to room temperature and a large increment in $R_{\mathrm{DS(ON)}}$ of one MOSFET (M16) was observed. $R_{\mathrm{DS(ON)}}$ of M15 increased only by 2 mΩ, and this may happen because of a shorter time duration of the test (90 min). The variations in $R_{\mathrm{DS(ON)}}$ before and after this aging are given in Table III.

TABLE III
MEASURED $R_{\mathrm{DS(ON)}}$ AND CORRESPONDING PEAK SSTDR OUTPUTS FOR THREE GROUPS OF MOSFETS BEFORE AND AFTER ACCELERATED AGING

MOSFETs		$R_{\mathrm{DS(ON)}}$ (mΩ) before aging	$R_{\mathrm{DS(ON)}}$ (mΩ) after aging	Peak SSTDR output
Group 1 (not aged)	M6	34.823	----	-27151
	M7	34.751	----	-27160
	M8	34.751	----	-27161
	M9	35.050	----	-27142
Group 2 (moderately aged)	M10	34.275	42.968	-27108
	M11	34.161	42.622	-27110
	M12	34.123	42.613	-27102
	M13	34.303	41.410	-27106
Group 3 (extremely aged)	M14	33.884	41.231	-27110
	M15	34.021	35.862	-27133
	M16	34.206	**6899**	**-24566**
	M17	34.188	46.718	-27045

From the peak values generated by the SSTDR hardware, it is apparent that SSTDR can generate consistent output depending on the impedance of the devices. However, the existing SSTDR hardware cannot faithfully detect a very small change in impedance (1–3 mΩ). For this reason, the SSTDR hardware generated almost equal peak values in the case of M10, M11, and M13 although the $R_{\mathrm{DS(ON)}}$ of M13 was smaller than that of M10 and M11. Due to the drastic increment in $R_{\mathrm{DS(ON)}}$ of M16, the peak SSTDR is significantly smaller than the other MOSFETs. Therefore, this MOSFET can be considered as damaged.

D. Estimation of $R_{\mathrm{DS(ON)}}$ from Correlated Peak Amplitude

This section describes how $R_{\mathrm{DS(ON)}}$ values can be calculated from the correlated outputs generated by the SSTDR system. Once the initial $R_{\mathrm{DS(ON)}}$ and corresponding SSTDR generated correlated outputs are known, the new $R_{\mathrm{DS(ON)}}$ after accelerated aging can be easily determined from the SSTDR data. Using the data summarized in Table I, Fig. 11(a) was drawn which shows the relationship between the $R_{\mathrm{DS(ON)}}$ values and correlated outputs. This relationship can be quantified as shown in (2) using the basic fitting tool in MATLAB. Here "x" and "y" represent

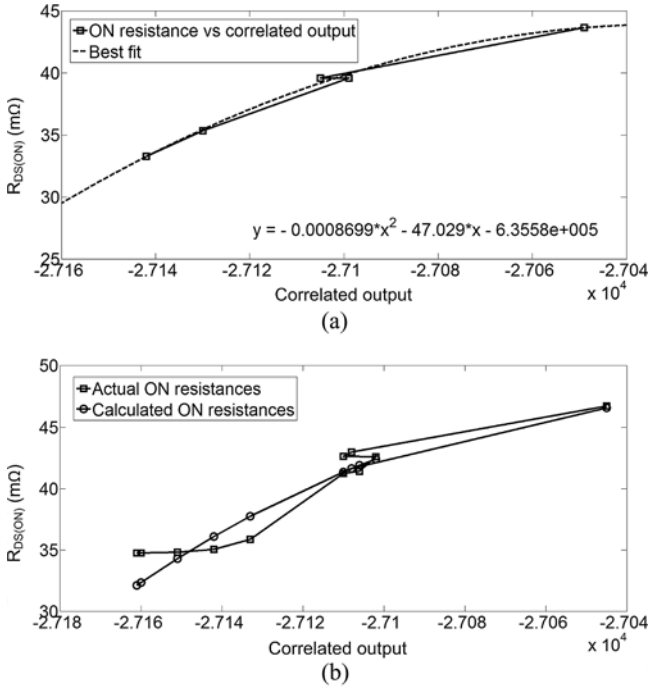

Fig. 11. (a) Relationship between $R_{DS(ON)}$ and correlated output and (b) graphical comparison between actual and calculated $R_{DS(ON)}$.

correlated output and $R_{\mathrm{DS(ON)}}$, respectively

$$y = -6.3558 \times 10^5 - 47.029x - 0.0008699x^2. \qquad (2)$$

Using (2), it is possible to calculate the $R_{\mathrm{DS(ON)}}$ of MOSFETs M6 to M17 by using the SSTDR data given in Table III. The actual $R_{\mathrm{DS(ON)}}$ values, SSTDR outputs and $R_{\mathrm{DSON)}}$ values calculated using (2) are given in Table IV. A graphical comparison between actual and calculated $R_{\mathrm{DS(ON)}}$ is given in Fig. 11(b).

The calculated $R_{\mathrm{DS(ON)}}$ of all MOSFETs except M16 are nearly equal to the actual $R_{\mathrm{DS(ON)}}$ values while SSTDR generated those output depending on the equivalent impedance across the test nodes. According to Fig. 5(a), SSTDR is applied across the drain and source nodes of MOSFET which is in parallel with $(R_{\mathrm{Lim}}+R_S)$, where R_S is the source's internal resistance. Therefore, SSTDR generates output depending on the impedance of $(R_{\mathrm{DS(ON)}} \parallel (R_{\mathrm{Lim}}+R_S)$. $R_{\mathrm{DS(ON)}}$ values of all MOSFETs except M16 are very small (in the range of 34–47 mΩ) compared to R_{Lim} (=5 Ω) + R_S. Therefore, the SSTDR generated outputs can be considered as true reflections of actual $R_{\mathrm{DS(ON)}}$ values. However, this statement is not correct in the case of M16 because of its very high $R_{\mathrm{DS(ON)}}$ value. The best fit curve of Fig. 11(a) and the function given in (2) were derived for very low $R_{\mathrm{DS(ON)}}$ values compared to $R_{\mathrm{DS(ON)}}$ of M16, and this might not be suitable for calculating the exact impedance of M16. Considering a normal aging process, the proposed SSTDR system can detect aging associated to the devices as well as any faults or damages (M16). The test setup for applying stress to the devices and characterizing the devices using SSTDR are shown in Fig. 12.

TABLE IV
CALCULATED $R_{\mathrm{DS(ON)}}$ USING FUNCTION (2) AND CORRESPONDING SSTDR DATA

MOSFETs		Actual $R_{DS(ON)}$ (mΩ)	Calculated $R_{DS(ON)}$ (mΩ)	SSTDR peak at the load end
Group 1 (not aged)	M6	34.823	34.2798	-27151
	M7	34.751	32.3346	-27160
	M8	34.751	32.1097	-27161
	M9	35.050	36.0841	-27142
Group 2 (moderately aged)	M10	42.968	41.6287	-27108
	M11	42.622	41.3582	-27110
	M12	42.613	42.3984	-27102
	M13	41.410	41.8922	-27106
Group 3 (extremely aged)	M14	41.231	41.3582	-27110
	M15	35.862	37.7475	-27133
	M16	6899	-5240.1	-24566
	M17	46.718	46.5865	-27045

V. SSTDR APPLIED TO AN H-BRIDGE AC–AC CONVERTER

A. Test Setup

SSTDR was applied to a power converter circuit while the converter was operational. This test was performed to verify if the proposed technique can identify an aged component in a live converter. The arrangement is shown in Fig. 13, and the schematic of the converter circuit is shown in Fig. 14. As there is no external trigger in the SSTDR hardware, it could be synchronized with the switching states of the MOSFET under test, and the converter was operated at a very low switching frequency to make sure the measured SSTDR data were generated during the ON/OFF states of the switches. SSTDR data were recorded across each test pairs during the following two states: 1) S1 and S2 are turned ON, S3 and S4 are turned OFF and 2) S3 and S4 are turned ON, S1 and S2 are turned OFF. The key objective of this test was to observe the peak SSTDR output across various components in this converter. There are four test points in this circuit (see Fig. 14), and SSTDR was applied in different combinations to map these four test points. A 5 V (RMS) 60 Hz AC input voltage was applied to the circuit, and the load resistance R_L was set to 5 Ω. The equivalent circuits of the H-bridge converter are shown in Fig. 15 for both switching states, and the internal resistances R_D of diodes D1, D2, D3, and D4 were considered equal for simplicity. Here, R_S is the source's internal resistance, ESR is the equivalent series resistance of the dc bus capacitor, and R_{S1}, R_{S2}, R_{S3}, and R_{S4} are the ON-state resistances of MOSFETs S1, S2, S3, and S4 respectively.

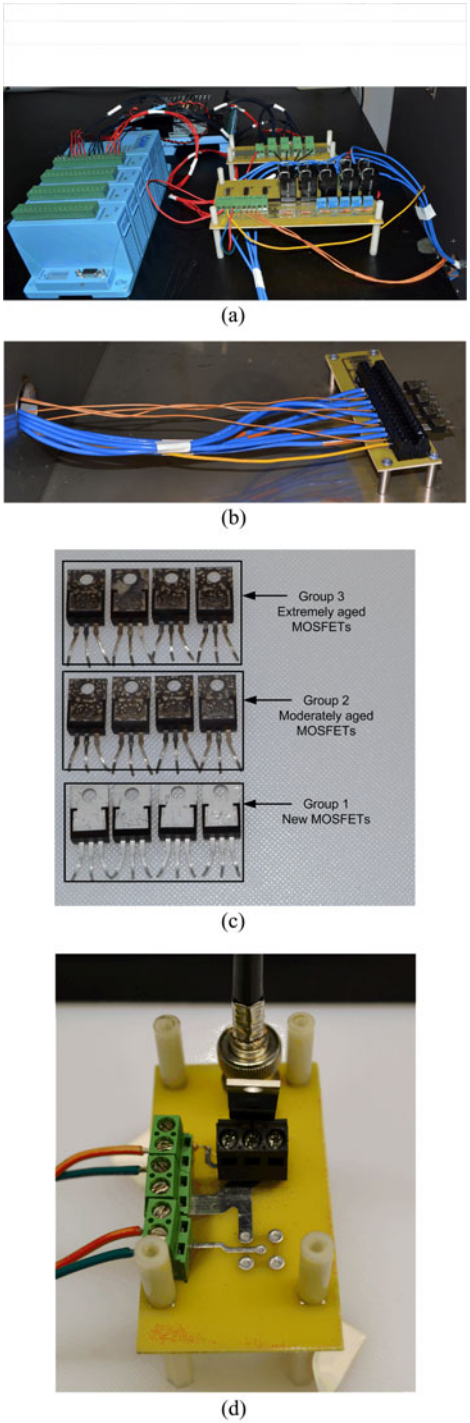

Fig. 12. Test setup showing the (a) data acquisition system connected to devices under test during accelerated aging procedure, (b) MOSFETs in the temperature chamber, (c) aged MOSFETs, and (d) dc–dc converter circuit to characterize MOSFETs.

The details of equivalent path impedance calculation of each node pair has been conducted by the authors and described in [42]. The equivalent path impedances of each node pair for both switching states are given in Table V, and the parallel combination of ESR and $(R_D+R_S+R_D)$ has been labeled as R_{eq}.

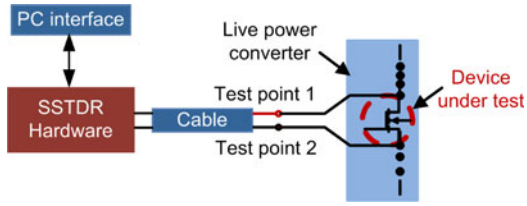

Fig. 13. Schematic of the test set up of showing the applied SSTDR to the device under test while the device is connected in a converter circuit.

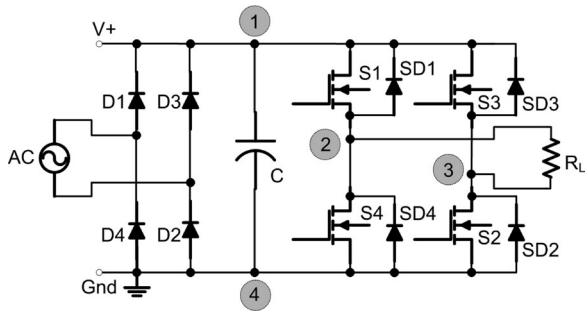

Fig. 14. Schematic of the H-bridge ac–ac converter showing the SSTDR test points.

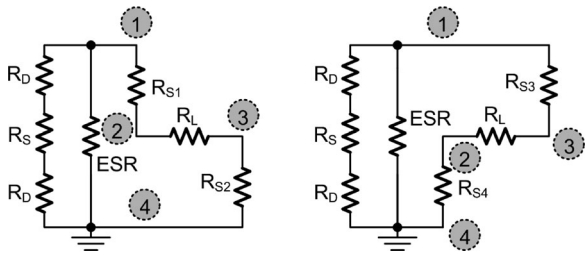

Fig. 15. Equivalent circuit in diagram of the H-bridge ac–ac converter (shown in Fig. 14) during both switching states. (a) S1 and S2 are activated and (b) S3 and S4 are activated.

TABLE V
EQUIVALENT PATH IMPEDANCES ACROSS NODE PAIRS IN AN H-BRIDGE AC–AC CONVERTER CIRCUIT DURING BOTH SWITCHING STATES

Test point	1 and 2	1 and 3	1 and 4	2 and 3	2 and 4	3 and 4
S1 and S2 are "ON"	R_{S1}	$R_{eq}+R_{S2}$	R_{eq}	$R_{S1}+R_{eq}+R_{S2}$	$R_{eq}+R_{S1}$	R_{S2}
S3 and S4 are "ON"	$R_{eq}+R_{S4}$	R_{S3}	R_{eq}	$R_{S3}+R_{eq}+R_{S4}$	R_{S4}	$R_{eq}+R_{S3}$

$$A=\begin{pmatrix} A_{11} & A_{12} & A_{13} & A_{14} \\ A_{21} & A_{22} & A_{23} & A_{24} \\ A_{31} & A_{32} & A_{33} & A_{34} \\ A_{41} & A_{42} & A_{43} & A_{44} \end{pmatrix}$$

Fig. 16. Generic form of the impedance matrix created using the SSTDR technique applied to the H-bridge ac–ac converter.

B. Formulating the Reflection-Based Impedance Matrix for the H-bridge AC–AC Converter

A reflection matrix has been constructed from the single-phase H-bridge ac–ac converter shown in Fig. 16. For $i = 1$–4

When S1, S2 are "ON" and S3, S4 are "OFF"

$$\text{Reference,A} = \begin{pmatrix} -24672 & -23793 & -21560 & -24083 \\ -23793 & -24672 & -21234 & -21366 \\ -21560 & -21234 & -24672 & -23538 \\ -24083 & -21366 & -23538 & -24672 \end{pmatrix}$$

When S1, S2 are "OFF" and S3, S4 are "ON"

$$\text{Reference,A} = \begin{pmatrix} -24672 & -21444 & -23711 & -23849 \\ -21444 & -24672 & -21202 & -23779 \\ -23711 & -21202 & -24672 & -21390 \\ -23849 & -23779 & -21390 & -24672 \end{pmatrix}$$

Fig. 17. Impedance matrix created from SSTDR generated outputs with all new MOSFETs (M6, M7, M8, and M9), dc bus capacitor, and diodes in an H-bridge ac–ac converter circuit during both switching conditions.

$$\text{A} = \begin{pmatrix} -24672 & \mathbf{-23683} & -21415 & -24044 \\ \mathbf{-23683} & -24672 & \mathbf{-21041} & \mathbf{-21209} \\ -21415 & \mathbf{-21041} & -24672 & -23506 \\ -24044 & \mathbf{-21209} & -23506 & -24672 \end{pmatrix}$$

Fig. 18. Matrix built from SSTDR generated outputs of the H-bridge ac–ac converter while S1 was replaced by an aged MOSFET during state I.

and $j = 1$–4, A_{ij} represents peak SSTDR output across any two test points among these four nodes. As explained earlier, the SSTDR generated output is the true reflection of the equivalent path impedances of different test pairs given in Table V. SSTDR generates negative output in short circuit conditions or in situations with extremely low impedances [$< z_o$ in (1)], and it generates positive output in open circuit conditions or in cases of higher impedances [$> z_o$ in (1)]. From the equivalent path impedances given in Table V, it is apparent that A_{12} and A_{34} will be the lowest during state I (when S1 and S2 are activated). Similarly, A_{13} and A_{24} will be the lowest during state II (when S3 and S4 are activated), whereas, A_{14} and A_{23} should be unaffected in both switching states. The SSTDR generated output in both switching conditions with all new components (zero aging) are given in Fig. 17, and these two matrices will be used as reference matrices.

It is of paramount importance to study how the impedance matrix changes when one or multiple components are aged in this ac–ac converter circuit. According to the impedance matrix analysis in [42], only the elements of the second row and the second column will be affected due to any aging in switch S1 during state I. However, no change is expected to be observed in matrix elements during state II due to the aging in S1. For analysis purpose, it is assumed that S1 has been aged and the corresponding modified matrix has been formed during state I, and it is given in Fig. 18. This figure shows that the matrix element A_{12} increases due to any aging in MOSFET S1, and A_{13} should not be affected due to this aging. However, there may be some capacitive effect in the real circuit and A_{13} may change due to the any aging with S1. The experimental setup to characterize the ac–ac converter using SSTDR is shown in Fig. 19.

Fig. 19. Experimental SSTDR setup to generate the impedance matrix for the H-bridge ac–ac converter.

C. Analysis of the Experimental Data: Reverse Synthesis Method

In order to derive a reliability model of the converter under test, we need the aging information consistent to every affected component such as the switching MOSFETs or IGBTs and capacitors in the core converter circuit. All these impedance information could be grouped in the impedance vector where the dimension of the vector will be equal to the number of components under test. For example, in the ac–ac converter test, six components will be studied using STTDR, and these components are S1–S4, C, and R_L. The SSTDR hardware is a two-terminal device that needs to be connected across the device under test. The proposed solution applies SSTDR signal across various components in a power converter in order to detect the impedance degradation associated with those components, and an impedance matrix is formed based on the recorded reflection data. While doing so, the results associated with any component is influenced by all other components such as free-wheeling diodes, parasitic, and source/load impedance connected in parallel to that aged component of interest. Therefore, we need a new algorithm that can deembed the correlated output corresponding to only that affected component, and obtain the impedance vector from the impedance matrix. This impedance vector will have the reflection data corresponding to individual components. Therefore, we need an additional step to transform this reflection- based impedance vector to actual impedance vector in ohms.

This paragraph explains how to create the actual impedance vector from the reflection-based impedance vector. Section V.A and B have shown how to create the impedance matrix based on the SSTDR data. These impedances are simply the $R_{\mathrm{DS(ON)}}$ of the corresponding MOSFETs while other components were connected across them during taking measurements. Therefore, we need to derive a new function to correlate the actual $R_{\mathrm{DS(ON)}}$ and SSTDR data, and Fig. 20 shows the relationship between measured $R_{\mathrm{DS(ON)}}$ and the corresponding correlated output. The actual $R_{\mathrm{DS(ON)}}$ of these MOSFETs was calculated by simply measuring the voltage and current through the MOSFET while SSTDR was applied. The SSTDR frequency was 48 MHz which is different from the SSTDR measurement done for characterizing isolated components. A curve-fitting method

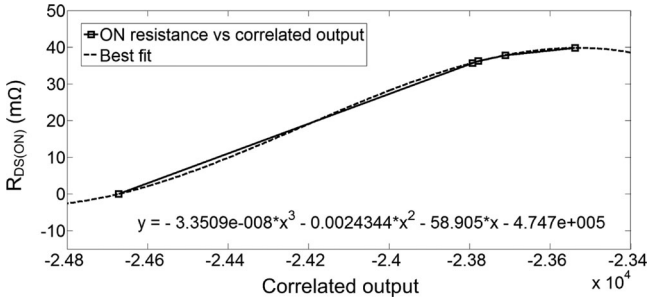

Fig. 20. Relationship between the correlated outputs and $\mathrm{R_{DS(ON)}}$ on MOSFETs used in the H-bridge ac–ac converter.

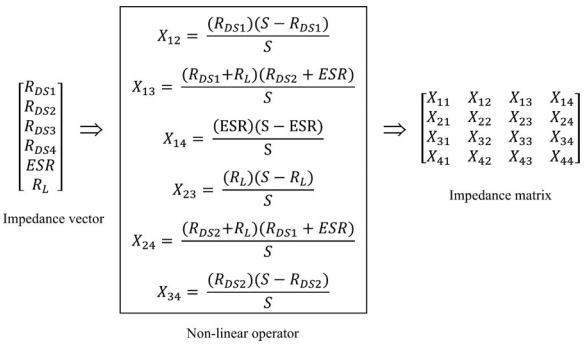

Fig. 21. System transform model to obtain the impedance matrix from the impedance vector. Here, [$\mathrm{S = R_{DS1} + R_{DS2} + ESR + R}_L$].

was used to find the relationship between the SSTDR data and the corresponding $R_{\mathrm{DS(ON)}}$, and this nonlinear function is given in (3). In this equation "x" and "y" represent correlated output and $R_{\mathrm{DS(ON)}}$, respectively

$$y = -4.747\times10^{5} - 58.905x - 0.0024344x^{2} - 3.3509x^{3}\times10^{-8}. \tag{3}$$

Using (3), the $R_{\mathrm{DS(ON)}}$ corresponding to an aged S1 can be calculated while other components were connected across it. The correlated output x is –23683 from Fig. 17. Using this value, the $R_{\mathrm{DS(ON)}}$ "y" can be calculated as 44.2821 mΩ. The actual $R_{\mathrm{DSON)}}$ from the voltage and current measurement was found as 45.567 mΩ. Therefore, the values of $R_{\mathrm{DS(ON)}}$ calculated from SSTDR data and from the conventional voltage and current measurement are in good agreement.

As mentioned earlier, an impedance vector consistent with components under test needs to be derived from the impedance matrix. The number of elements in this vector should be the same as the number of aging affected components. In forward transform, an impedance matrix could be created from impedance vector, and this project thus needed the reverse transform. The forward transformation has been shown in Fig. 21 for i = 1–4 and j = 1–4, X*ij* represents the equivalent impedance between any two test points among the four different nodes. X*ij* = 0 for i=j because it would be a short circuit. Therefore, all the diagonal elements of this matrix are "0." In fact, there exist two impedance matrices for two different operating states of the converter, and these two matrices are shown in Fig. 22. For simplification, it was assumed that impedance between nodes 1

$$\mathrm{A_{State\ I}} = \begin{pmatrix} 0 & 0.03377 & 0.05048 & 0.01694 \\ 0.03377 & 0 & 0.08357 & 0.05048 \\ 0.05048 & 0.08357 & 0 & 0.03377 \\ 0.01694 & 0.05048 & 0.03377 & 0 \end{pmatrix}$$

(a)

$$\mathrm{A_{State\ II}} = \begin{pmatrix} 0 & 0.05048 & 0.03377 & 0.01694 \\ 0.05048 & 0 & 0.08357 & 0.03377 \\ 0.03377 & 0.08357 & 0 & 0.05048 \\ 0.01694 & 0.03377 & 0.05048 & 0 \end{pmatrix}$$

(b)

Fig. 22. Impedance matrices for the power converter created from the original impedance vector shown in (6) during (a) state I and (b) state II.

$$\mathrm{A} = \begin{bmatrix} 0 & 0.04165 & 0.05929 & 0.01992 \\ 0.04165 & 0 & 0.09996 & 0.06125 \\ 0.05929 & 0.09996 & 0 & 0.03968 \\ 0.01992 & 0.06125 & 0.03968 & 0 \end{bmatrix}$$

Fig. 23. Modified impedance matrix during state I due to aging with $\mathrm{R_{DS1}}$, $\mathrm{R_{DS2}}$, and ESR.

and 4 would be

$$R_{\mathrm{eq}} = \mathrm{ESR} \parallel (R_D + R_S + R_D) \approx \mathrm{ESR}. \tag{4}$$

Because of the nonlinearity and over deterministic nature of the system, it is not possible to inverse the operator and to determine the impedance vector from the impedance matrix. In order to identify the variation in impedances across node pairs, the new impedance vector needs to be consistently determined with the aged converter, and a comparison with the initial vector can be used to identify the level of aging associated with any particular component. Even if the impedance matrix and the operator are known, the process is not reversible because of its nonlinear nature. Therefore, an error function was defined in MATLAB with the expression

$$F = (X_{13} - X_{e\_13})^2 + (X_{24} - X_{e\_24})^2. \tag{5}$$

In order to verify whether the reverse synthesis method could reproduce the impedance vector with reasonable accuracy, a test case was created, where both the impedance vector and the corresponding impedance matrix are known. The impedance vector was the following:

$$\begin{bmatrix} R_{\mathrm{DS1}} \\ R_{\mathrm{DS2}} \\ R_{\mathrm{DS3}} \\ R_{\mathrm{DS4}} \\ \mathrm{ESR} \\ R_L \end{bmatrix} = \begin{bmatrix} 0.042 \\ 0.040 \\ 0.034 \\ 0.034 \\ 0.020 \\ 5 \end{bmatrix}. \tag{6}$$

The affected components were R_{DS1}, R_{DS2}, and ESR. Due to the aging associated with these three components, the actual impedance matrix in state I looks like the matrix shown in Fig. 23. Using the error function, an iterative program was executed in MATLAB, and R_{DS1} was varied from 0.034 to 0.050 Ω with a 0.0005 Ω interval. The corresponding simulation results

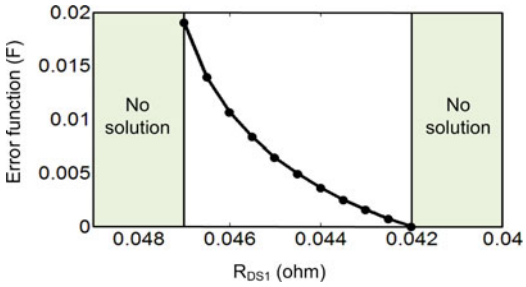

Fig. 24. Variation in error function as a function of R_{DS1}. The solution produces imaginary results for $0.042 > R_{DS1} > 0.047$.

TABLE VI
SIMULATION RESULTS OF THE CONVERGING STEPS USED TO IDENTIFY THE NEW R_{DS1}

R_{DS1} (Ω)	R_{DS2} (Ω)	R_L (Ω)	ESR (Ω)
0.04700	0.04447	0.24379	0.02099
0.04650	0.04403	0.29503	0.02090
0.04600	0.04359	0.34641	0.02081
0.04550	0.04314	0.40568	0.02072
0.04500	0.04270	0.47892	0.02062
0.04450	0.04225	0.57486	0.02053
0.04400	0.04180	0.70895	0.02043
0.04350	0.04135	0.91294	0.02032
0.04300	0.04090	1.26542	0.02022
0.04250	0.04045	2.03055	0.02011
0.04200	0.04000	5.00000	0.02000

have been summarized in Fig. 24 and Table VI. The error function becomes the smallest when R_{DS1} is equal to 42 mΩ; which is the correct solution, and this iterative solution can accurately reconstruct the impedance vector from the impedance matrix. In real life, the SSTDR hardware will measure reflections at various node pairs and therefore, construct a matrix equivalent to the impedance matrix. By knowing the nonlinear operator, the change in individual components could be identified using this process.

VI. RELIABILITY ANALYSIS OF AN H-BRIDGE AC–AC CONVERTER

Once the impedance vector for a specific converter is obtained, the overall reliability of the converter can be performed by using the individual aging associated to those components. This section presents the reliability analysis of the H-bridge converter (shown in Fig. 14) based on the component parameters, and those parameters used in this experiment are given in Table VII. It was assumed that the $R_{DS(ON)}$ of the MOSFET S1 changed from 34 to 44 mΩ due to natural aging (which is consistent with the experimental results summarized in Tables I and III). Although in real converters all the components will age naturally with time, only one of the MOSFET's aging has been considered to simplify the analysis. The circuit was simulated in Powersim (PSIM) using the parameters given in Table VII, and it was assumed that the circuit is operating in an open-loop condition.

TABLE VII
CIRCUIT PARAMETERS OF THE H-BRIDGE AC–AC CONVERTER

Symbol	Description	Value
V_{in}	AC Input voltage	80 V (RMS)
V_{out}	Output voltage	100 V
r_{sw}	MOSFET $R_{DS(ON)}$	0.034 - 0.044 Ω
r_D	Diode on resistance	0.03 Ω
V_f	Diode forward voltage	0.7 V
C	Output capacitance	4700 μF
$V_{RATED\text{-}CAP}$	Rated voltage of capacitor	200 V
r_C	ESR of the capacitor	0.017Ω
R_L	Load resistance	35 Ω

Considering a constant failure rate, the reliability of the system can be calculated as

$$R_S(t) = e^{(-\lambda_{\mathrm{SYSTEM}} \times t)} \ [43]. \tag{7}$$

Here, $R_S(t)$ is the probability that the system will not fail within time t and $\lambda_{\mathrm{SYSTEM}}$ is the failure rate of the system. The mean-time-to-failure (MTTF) can be calculated from the reliability of the system using the following equation:

$$\mathrm{MTTF} = \int_0^\infty R_S(t)\,dt = \frac{1}{\lambda_{\mathrm{SYSTEM}}}. \tag{8}$$

The failure rate of an N-channel MOSFET can be written as

$$\lambda_{\mathrm{sw}} = \lambda_B \pi_T \pi_A \pi_E \pi_Q \ \ [44], [45]. \tag{9}$$

The base failure rate λ_B is constant and equal to 0.012. The application and quality factors π_A and π_Q are 8 (for switches rated at 135 W). The environment factor π_E is considered as 9 for an equipment installed on wheeled or tracked vehicles. Temperature factor and junction temperature can be calculated as

$$\begin{aligned}\pi_T &= \text{temperature factor} \\ &= \exp\left[-1925\left\{\left(\frac{1}{T_j + 273}\right) - \frac{1}{298}\right\}\right] \end{aligned} \tag{10}$$

$$T_j = T_a + (\theta_{ja})\, P_{\mathrm{sw}}. \tag{11}$$

Ambient temperature T_a is 25° C and junction to ambient thermal resistance θ_{ja} is 62 °C/W (based on the datasheet of different TO-220 package MOSFETS). The total power dissipation (conduction loss + switching loss) of the switching device is P_{sw}. Therefore, considering the values stated previously in (9)

$$\lambda_{\mathrm{sw}} = \lambda_B \pi_T \pi_A \pi_E \pi_Q = 0.012 \times \pi_T \times 8 \times 9 \times 8 = 6.912 \times \pi_T. \tag{12}$$

The power loss (conduction loss + switching loss) was calculated to be 0.2972 W in a power MOSFET from simulation when the $R_{DS(ON)}$ is 0.034 Ω

$$T_j = T_a + (\theta_{\mathrm{ja}})\, P_{\mathrm{sw}} = 25 + (62 \times 0.2972) = 43.4264 \tag{13}$$

$$\pi_T = \exp\left[-1925\left\{\left(\frac{1}{T_j + 273}\right) - \frac{1}{298}\right\}\right] = 1.4567 \tag{14}$$

$$\lambda_{\mathrm{sw}} = 6.912 \times 1.4567 = 10.068 \text{ failures/million} - \text{h}. \tag{15}$$

The failure rate of a diode can be written as

$$\lambda_{\mathrm{DIODE}} = \lambda_B \pi_T \pi_S \pi_C \pi_E \pi_Q \ [44], [45]. \tag{16}$$

The base failure rate λ_B is 0.003 for schottky devices. The stress factor π_S accounts for the operational reverse-voltage stress of the diode relative to the rated voltage. Considering $V_{\mathrm{OUT}}/V_{\mathrm{RATED-DIODE}} \leq 0.3$, stress factor π_S is 0.054. The effect of the diode's physical contact with the PCB is denoted by the contact construction factor π_C, and this is unity for metallurgical bonded contacts. Quality and environment factors (for equipment installed on wheeled or tracked vehicles) π_Q and π_E are 8 and 9, respectively. The temperature factor can be calculated as follows:

$$\begin{aligned}\pi_T &= \text{temperaturefactor} \\ &= \exp\left[-3091\left\{\left(\frac{1}{T_j+273}\right)-\frac{1}{298}\right\}\right]. \end{aligned}\tag{17}$$

T_j is the junction temperature and it is computed in the same manner it was done for MOSFET. Power loss in a diode is considered to be 2.3935 W from simulation

$$T_j = T_a + (\theta_{\mathrm{ja}})\, P_{\mathrm{diode}} = 25 + (50 \times 2.3935) = 144.675 \tag{18}$$

$$\pi_T = \exp\left[-3091\left\{\left(\frac{1}{T_j+273}\right)-\frac{1}{298}\right\}\right] = 19.5308. \tag{19}$$

Therefore, considering the values stated previously

$$\begin{aligned}\lambda_{\mathrm{DIODE}} &= \lambda_B \pi_T \pi_S \pi_C \pi_E \pi_Q \\ &= 0.003 \times 19.5308 \times 0.054 \times 1 \times 9 \times 8 \\ &= 0.2278 \text{ failures/million} - \text{h}. \end{aligned}\tag{20}$$

The failure rate of dc aluminum or dry electrolyte polarized capacitor can be expressed as

$$\lambda_{\mathrm{CAP}} = \lambda_B \pi_{CV} \pi_E \pi_Q \ [44], [45] \tag{21}$$

$$\lambda_B = \text{base failure rate} = 0.0028 \times \left[\left(\frac{S_{\mathrm{CAP}}}{0.55}\right)^3 + 1\right] \times \exp\left[4.09 \times \left(\frac{T+273}{358}\right)^{5.9}\right] \tag{22}$$

$$S_{\mathrm{CAP}} = \frac{V_{\mathrm{OUT}} + (\Delta V_{\mathrm{OUT}}/2)}{V_{\mathrm{RATED-CAP}}} \tag{23}$$

$$\pi_{\mathrm{CV}} = 0.32\,(C\mu\mathrm{F})^{0.19}. \tag{24}$$

The operational voltage stress S_{CAP} is defined as the ratio of the peak-to-rated capacitor voltage. The capacitance factor π_{CV} denotes the failure rate based on the value of capacitance in μF. Finally, π_E and π_Q are 2 and 10, respectively, for equipment installed on wheeled or tracked vehicles. If a capacitor with 4700 μF capacitance is used for 100 V output, the rated voltage is 200 V and p-p ripple voltage is 5.11926 V.

Considering the values stated previously

$$\begin{aligned}S_{\mathrm{CAP}} &= \frac{V_{\mathrm{OUT}} + (\Delta V_{\mathrm{OUT}}/2)}{V_{\mathrm{RATED-CAP}}} = \frac{100 + (5.11926/2)}{200} \\ &= 0.512798 \end{aligned}\tag{25}$$

$$\begin{aligned}\lambda_B &= 0.0028 \times \left[\left(\frac{S_{\mathrm{CAP}}}{0.55}\right)^3 + 1\right] \\ &\quad \times \exp\left[4.09 \times \left(\frac{T+273}{358}\right)^{5.9}\right] \\ &= 0.0028 \times 1.8105 \times 3.9978 = 0.020266 \end{aligned}\tag{26}$$

$$\pi_{\mathrm{CV}} = 0.32\,(C\mu\mathrm{F})^{0.19} = 0.32\,(4700)^{0.19} = 1.5953 \tag{27}$$

$$\begin{aligned}\lambda_{\mathrm{CAP}} &= \lambda_B \pi_{\mathrm{CV}} \pi_E \pi_Q = 0.020266 \times 1.5953 \times 12 \times 10 \\ &= 3.8797 \text{ failures/million} - \text{h}. \end{aligned}\tag{28}$$

The H-bridge converter circuit shown in Fig. 14 does not have any redundant components and requires zero failures for proper operation. Therefore, the failure rate of the converter can be calculated as

$$\lambda_{\mathrm{SYSTEM}} = 4 \times \lambda_{\mathrm{sw}} + \lambda_{\mathrm{CAP}} + 4 \times \lambda_{\mathrm{DIODE}}. \tag{29}$$

Using the calculated failure rates of active switches, diodes, and capacitors

$$\begin{aligned}\lambda_{\mathrm{SYSTEM}} &= 4 \times \lambda_{\mathrm{sw}} + \lambda_{\mathrm{CAP}} + 4 \times \lambda_{\mathrm{DIODE}} \\ &= 4 \times 10.068 + 3.8797 + 4 \times 0.2278 \\ &= 45.0629 \text{ failures/million} - \text{h}. \end{aligned}\tag{30}$$

Therefore

$$\begin{aligned}\mathrm{MTTF} &= \frac{1}{\lambda_{\mathrm{SYSTEM}}} = \frac{10^6}{45.0629} = 22191.2\mathrm{h/failure} \\ &= 2.533 \text{ years/failure}. \end{aligned}\tag{31}$$

A MATLAB script based on the analysis presented previously was executed to estimate the converter's failure rate and MTTF as a function of aging in the MOSFET, and the obtained results have been summarized in Fig. 25. The power loss associated with the MOSFET will eventually increase due to aging in MOSFET S1, and that has been demonstrated in Fig. 25(a). Fig. 25(b) shows that the MOSFET failure rate will significantly increase if $R_{\mathrm{DS(ON)}}$ continues to increase, and Fig. 25(c) demonstrates that converter reliability can be expressed as a function of MOSFET $R_{\mathrm{DS(ON)}}$. The MTTF can vary from 2.541 to 2.473 for a variation in $R_{\mathrm{DS(ON)}}$ from 0.034–0.044 Ω. The MTTF of the converter would be even lower if aging in other components in the circuit are considered. For simplicity, only the aging associated with one MOSFET has been considered in the MATLAB script.

$R_{\mathrm{DS(ON)}}$ of S1 prior to accelerated aging was measured to be 35.64 mΩ from the voltage and current through the MOSFET, and the calculated $R_{\mathrm{DS(ON)}}$ (=45.567 mΩ) obtained from the SSTDR data was nearly in very good agreement (= 44.2821 mΩ). Therefore, the actual MTTF of the H-bridge

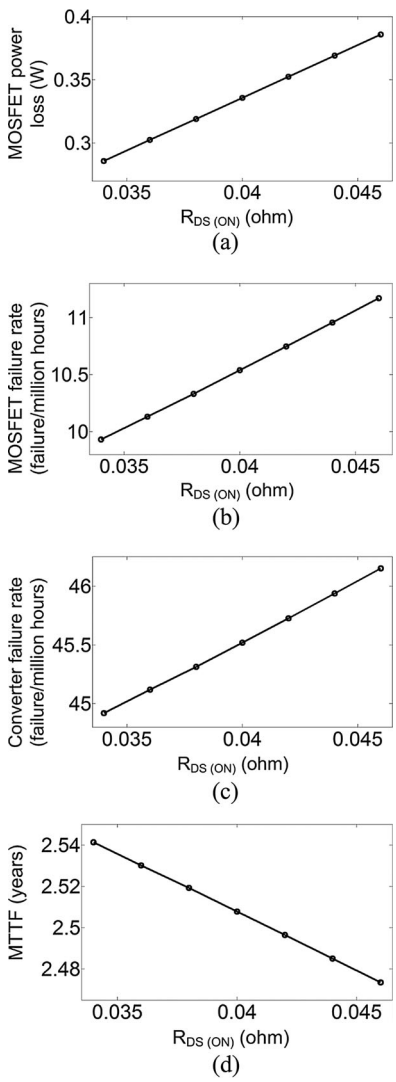

Fig. 25. Analytically computed reliability and failure analysis results for the H-bridge ac–ac converter: (a) variation in MOSFET power loss, (b) MOSFET failure rate, (c) converter failure rate, and (d) MTTF of the entire converter as a function of $R_{DS(ON)}$.

ac–ac converter can be approximated from the calculated $R_{\mathrm{DS(ON)}}$ using the SSTDR generated data.

VII. Conclusion

A nonintrusive measurement technique to estimate the state of health of power converters has been described in this paper. MOSFETs were aged using both power and thermal stress in a controlled environment, and SSTDR was applied to identify the aged and damaged devices and determine the level of aging while the devices were connected in an operational circuit. It was found that SSTDR can detect degradation in terms of $R_{\mathrm{DS(ON)}}$ variation in MOSFETs. SSTDR was applied in a single phase ac–ac converter across different test point pairs and corresponding peak SSTDR responses were recorded. A reverse mapping method has been used to recover the impedance vector from this impedance matrix in order to isolate the aging affected devices. By comparing these two vectors (one was generated using all new MOSFETs, while another one was generated using all but one aged MOSFET), it is possible to identify the degraded MOSFET and its corresponding $R_{\mathrm{DS(ON)}}$ variation. This paper also presented a failure analysis for the H-bridge ac–ac converter studied using the SSTDR hardware. Because the SSTDR technique could be applied to a live converter, it is possible to detect the gradual degradation in various components in the converter, and it was applied to MOSFETs within the scope of this project. By combining the SSTDR data and the reverse mapping technique, the real-time reliability and time to failure can be calculated. This approach is truly novel, and this paper has presented a sample case with a single-aged MOSFET. However, it is possible to use this technique for converters having multiple aged components, and this is already included in our future research portfolio.

References

[1] E. Wolfgang, "Examples for failures in power electronics systems," presented at the ECPE Tutorial 'Reliable Power Electronics System, Nuremberg, Germany, Apr. 2007.

[2] J. R. Celaya, N. Patil, S. Saha, P. Wysocki, and K. Goebel, "Towards accelerated aging methodologies and health management of power MOSFETs (technical brief)," presented at the Annu. Conf. Prognostics Health Management Society, San Diego, CA, USA, 2009.

[3] N. Patil, D. Das, K. Goebel, and M. Pecht, "Identification of failure precursor parameters for insulated gate bipolar transistors (IGBTs)," in *Proc. Int. Conf. Prognostics Health Manage.*, 2008, pp. 1–5.

[4] J. R. Celaya, C. Kulkarni, S. Saha, G. Biswas, and K. Goebel, "Accelerated aging in electrolytic capacitors for prognostics," in *Proc. Annu. Proc. Rel. Maintainability Symp.*, 2012, pp. 1–6.

[5] M. S. Nasrin and F. H. Khan, "Characterization of aging process in power converters using spread spectrum time domain reflectometry," in *Proc. IEEE Energy Convers. Congr. Expo*, Sep. 15–20, 2012, pp. 2142–2148.

[6] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.

[7] S. Saha, J. R. Celaya, V. Vashchenko, S. Mahiuddin, and K. F. Goebel, "Accelerated aging with electrical overstress and prognostics for power MOSFETs," in *Proc. Energytech*, 2011, pp. 1–6.

[8] J. Celaya, P. Wysocki, V. Vashchenko, S. Saha, and K. Goebel, "Accelerated aging system for prognostics of power semiconductor devices," in *Proc. IEEE AUTOTESTCON*, 2010, pp. 1–6.

[9] S. S. Mahiuddin, "Modeling of the impact of electrical stressors on the degradation process of Power MOSFETs," M.S. thesis, Dept. Elec. Eng. San Jose State univ., San Jose, CA, USA, 2011, Paper 3943.

[10] J. R. Celaya, N. Patil, S. Saha, P. Wysocki, and K. Goebel, "Towards accelerated aging methodologies and health management of power MOSFETs (technical brief)," in *Proc. Annu. Conf. Prognostics Health Manage. Soc.*, San Diego, CA, USA, 2009.

[11] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in MOS oxides," *IEEE Trans. Nuclear Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008.

[12] Y. L. Seng, "Characterization of intermetallic growth for gold bonding and copper bonding on aluminum metallization in power transistors," in *Proc. Electron. Packag. Technol. Conf.*, 2007, pp. 731–736.

[13] T. Azoui, P. Tounsi, Ph. Dupuy, J. M. Dorkel, and D. Martineau, "Numerical and experimental results correlation during power MOSFET ageing," in *Proc. 13th Int. Conf. Therm., Mech. Multi-Phys. Simul. Experiments Microelectron. Microsyst.*, 2012, pp. 1/4–4/4.

[14] Y. L. Seng, "Characterization of intermetallic growth for gold bonding and copper bonding on aluminum metallization in power transistors," in *Proc. Electron. Packag. Technol. Conf.*, 2007, pp. 731–736.

[15] L. Dupont, S. Lefebvre, M. Bouaroudj, Z. Khatir, J. C. Faugieres, and F. Emorine, "Ageing test results of low voltage MOSFET modules for electrical vehicles," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.

[16] D. C. Katsis and J. D. van Wyk, "Void-induced thermal impedance in power semiconductor modules: Some transient temperature effects," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1905–1911, Sep./Oct. 2003.

[17] J. R. Celaya, A. Saxena, V. Vashchenko, S. Saha, and K. Goebel, "Prognostics of power MOSFET," in *Proc. 23rd Int. Symp. Power Semicond. Devices ICs*, 2011, pp. 160–163.

[18] J. R. Celaya, A. Saxena, C. S. Kulkarni, S. Saha, and K. Goebel, "Prognostics approach for power MOSFET under thermal-stress aging," in *Proc. Annu. Proc. Rel. Maintainability Symp.*, 2012, pp. 1–6.
[19] A. Testa, S. De Caro, and S. Russo, "A reliability model for power MOSFETs working in avalanche mode based on an experimental temperature distribution analysis," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3093–3100, Jun. 2012.
[20] G. H. Sarma, G. Nitin, M. Ramanan, K. Mehta, and A. Bhattacharjee, "Reliability studies on high current power modules with parallel mosfets," in *Proc. Eur. Microelectron. Packag. Conf.*, 2009, pp. 1–70.
[21] T. Wiesinger and H. Ertl, "A novel real time monitoring unit for PWM converter electrolytic capacitors," in *Proc. Power Electron. Spec. Conf.*, 2008, pp. 523–528.
[22] U. Franke, R. Kruemmer, and J. Petzoldt, "Online diagnostics and condition monitoring in voltage source inverters," in *Eur. Conf. Power Electron. Appl.*, 2005, p. 6.
[23] J. M. Anderson, R. W. Cox, and J. Noppakunkajorn, "An Online fault diagnosis method for power electronic drives," in *Proc. IEEE Electric Ship Technol. Symp.*, 2011, pp. 492–497.
[24] X. Dawei, R. Li, P. Tavner, Y. Shaoyong, A. Bryant, and P. Mawby, "Monitoring solder fatigue in a power module using the rise of case-above-ambient temperature," in *Proc. Energy Convers. Congr. Expo.*, 2010, pp. 955–962.
[25] A. M. R. Amaral and A. J. M. Cardoso, "Using input current and output voltage ripple to estimate the output filter condition of switch mode DC/DC converters," in *Proc. IEEE Int. Symp. Diagnostics Elect. Mach., Power Electron. Drives*, 2009, pp. 1–6.
[26] T.-J. Kim, J.-P. Lee, B.-D. Min, and D.-W. Yoo, "A diagnosis method of DC/DC converter aging based on the variation of parasitic resister," in *Proc. 31st Int. Telecommun. Energy Conf.*, 2009, pp. 1–5.
[27] L. Chet and C. Furse, "Noise domain reflectometry for locating wiring faults," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 1, pp. 97–104, Feb. 2005.
[28] P. Tsai, L. Chet, C. C. You, and C. Furse, "Mixed-signal reflectometer for location of faults on aging wiring," *IEEE Sens. J.*, vol. 5, no. 6, pp. 1479–1482, Dec. 2005.
[29] C. R. Sharma, F. C. Reid, and R. Harrison, "Low power STDR sensor for locationg faults in aging aircraft wiring," *IEEE Sens. J.*, vol. 7, no. 1, pp. 43–50, Jan. 2007.
[30] P. Amini, C. Furse, and B. Farhang-Boroujeny, "Filterbank multicarrier reflectometry for cognitive live wire testing," *IEEE Sens. J.*, vol. 9, no. 12, pp. 1831–1837, Dec. 2009.
[31] P. Smith, C. Furse, and J. Gunther, "Analysis of spread spectrum time domain reflectometry for wire fault location," *IEEE Sens. J.*, vol. 5, no. 6, pp. 1469–1478, Dec. 2005.
[32] P. K. Kuhn, C. Furse, and P. Smith, "Locating hidden hazards in electrical wiring," presented at the Aged Electrical Systems research applied symp., Chicago, IL, USA, 2006.
[33] C. Furse, C. C. You, L. Chet, and P. Pendayala, "A critical comparison of reflectometry methods for location of wiring faults," *Smart Struct. Syst.*, vol. 2, no. 1, pp. 25–46, 2006.
[34] S. Hashino and T. Shimizu, "Characterization of parasitic impedance in a power electronics circuit board using TDR," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 900–905.
[35] H. Zhu, A. R. Hefner, and J.-S. Lai, "Characterization of power electronics system interconnect parasitic using time domain reflectometry," *IEEE Trans. Power Electron*, vol. 14, no. 4, pp. 622–628, Jul. 1999.
[36] D. Kwon, M. H. Azarian, and M. Pecht, "Non-destructive sensing of interconnect failure mechanisms using time domain reflectometry," *IEEE Sensors J.*, vol. 11, no. 6, pp. 1236–1241, May 2011.
[37] D. Kwon, M. H. Azarian, and M. Pecht, "Identification of interconnect failure mechanisms using RF impedance analysis," *IEEE workshop Signal Propag. Interconnects*, 2009, pp. 1–4.
[38] Y. Lu, Y. Bin, W. Ming, and F. Jingdong, "Time domain reflectometry technique for detecting the degradation of solder joints," in *Proc. 9th Int. Conf. Rel., Maintainability Safety*, 2011, pp. 395–397.
[39] C. S. Chiu, W. L. Chen, K. H. Liao, B. Y. Chen, Y. M. Teng, G. W. Huang, and L. K. Wu, "Pad characterization for CMOS technology using time domain reflectometry," in *Proc. IEEE Int. RF Microw. Conf.*, 2008, pp. 215–217.
[40] Y. Wang, K. P. Cheung, R. Choi, G. A. Brown, and B.-H. Lee, "Accurate series-resistance extraction from capacitor using time domain reflectometry," *IEEE Electron. Device Lett*, vol. 28, no. 4, pp. 279–281, Apr. 2007.
[41] (2012). [Online].Available: http://livewireinnovation.com/
[42] M. Sultana Nasrin and F. H. Khan, "Use of spread spectrum time domain reflectometry to estimate state of health of power converters," in *Proc. IEEE 13th Workshop Control Model. Power Electron. (COMPEL)*, Jun. 10–13, 2012, pp. 1–6.
[43] *Military Handbook Electronic Reliability Design Handbook, MIL-HDBK-338B*, Department of Defense, Washington, DC, USA, Oct. 12, 1998.
[44] *Military Handbook Reliability Prediction of Electronic Equipment, MIL-HDBK-217 F*, Department of Defense, Washington, DC, USA, Dec. 2, 1991.
[45] S. V. Dhople, A. Davoudi, A. D. Dominguez-Garcia, and P. L. Chapman, "A unified approach to reliability assessment of multiphase DC–DC converters in photovoltaic energy conversion systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 739–751, Feb. 2012.
[46] S. B. Lee, J. Yang, J. Hong, J.-Y. Yoo, B. Kim, K. Lee, Y. Jangho, M. Kim, K.-W. Lee, E. J. Wiedenbrug, and S. Nandi, "A new strategy for condition monitoring of adjustable speed induction machine drive systems," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 389–398, Feb. 2011.
[47] D. Xiang, L. Ran, P. Tavner, S. Yang, A. Bryant, and P. Mawby, "Condition monitoring power module solder fatigue using inverter harmonic identification," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 235–247, Jan. 2012.
[48] H. Sheng, F. Wang, and C. W. Tipton IV, "A fault detection and protection scheme for three-level DC–DC converters based on monitoring flying capacitor voltage," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 685–697, Feb. 2012.
[49] S. Zhou, L. Zhou, and P. Sun, "Monitoring potential defects in an IGBT module based on dynamic changes of the gate current," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1479–1487, Mar. 2013.

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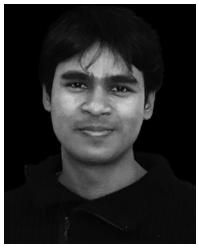

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