

FLOATING GATE CURRENT MIRROR FOR GAIN CORRECTION IN CMOS TRANSLINEAR CIRCUITS

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ABSTRACT

The exponential behavior of MOSFETs in subthreshold operation has recently been exploited to build CMOS translinear circuits such as multipliers and log-domain filters. A major obstacle in developing a practical CMOS implementation is the variation in threshold voltage between devices. In translinear circuits, these voltage offsets manifest themselves as gain errors in the current-mode outputs. We have designed a floating-gate CMOS current mirror that can adapt its gain to compensate for these errors. The adaptation process uses only hot-electron injection, so the high voltages typically associated with tunneling are not needed. A small array of these circuits were fabricated in a standard 1.2 μm double-poly CMOS process. We demonstrate gain adaptation and discuss the non-linearity introduced by the adaptive mirror.

1. INTRODUCTION

Translinear circuits use devices whose transconductance is linear with current (*i.e.*, the current through the device is an exponential function of the input voltage). A recent resurgence of interest in log-domain filtering [1] has led to the development of translinear, current-mode circuits in modern technologies. Standard CMOS processes are well-suited for building translinear circuitry if the transistors are operated in the weak inversion, or *subthreshold* region, where the drain current exhibits an exponential dependence on gate voltage. Recent work with translinear CMOS circuits has yielded practical log-domain filters, multipliers, and more general power-law circuits [2], [3], [4], [5].

The device-to-device variation in threshold voltage associated with MOS transistors [6], [7] is a major obstacle in building arrays of matching translinear circuits across a die. In translinear circuits, these voltage offsets are transformed into gain errors in current-mode signals. This is easily seen by considering the simplest current-mode circuit: the current mirror (see Figure 1).

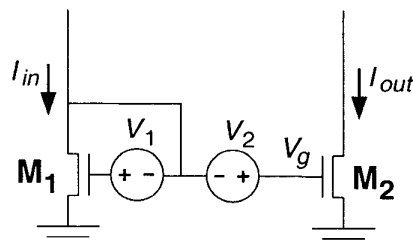


Figure 1. Current Mirror with Transistor Mismatch. Stochastic cross-chip variations in the threshold voltages of M_1 and M_2 , modeled here as voltage sources V_1 and V_2 , introduce gain errors into translinear, current-mode CMOS circuits.

The voltage sources V_1 and V_2 represent offsets in the threshold voltages due to impurities in the silicon, surface states, and defect traps. The equation for subthreshold transistor operation in saturation is given by

$$I = I_0 \exp\left(\frac{\kappa}{U_T} V_g\right) \quad (1)$$

where U_T is the thermal voltage kT/q , κ is the exponential slope (typically around 0.65), I_0 is a process dependent constant, and V_g is the gate voltage. Thus if we force a current I_{in} into M_1 , then the gate voltage of M_2 is given by

$$V_g = \frac{U_T}{\kappa} \ln \frac{I_{in}}{I_0} - V_1 + V_2 \quad (2)$$

Solving for I_{out} , we get

$$I_{out} = K I_{in} \quad (3)$$

where

$$K = \exp\left[\frac{\kappa}{U_T}(V_2 - V_1)\right] \quad (4)$$

If $V_1 \neq V_2$, then $K \neq 1$. A second source of mismatch in CMOS transistors is variation in the length L and

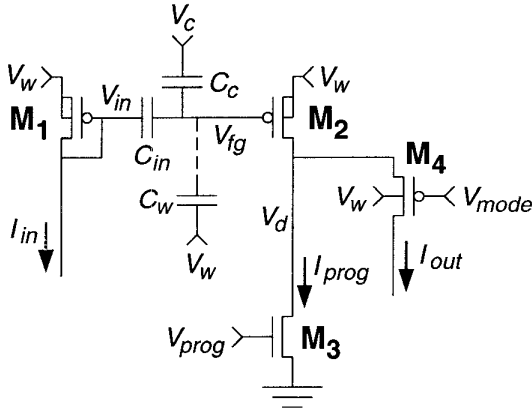


Figure 2. Schematic of the Programmable-Gain Current Mirror (PGCM). The diode-connected transistor M_1 is capacitively couple to the floating gate through C_{in} . This floating gate voltage controls the current through M_2 . If V_d is sufficiently low, hot-electron injection will add charge to the floating node, decreasing V_{fg} . In programming mode, the floating-gate charge is increased until the current through M_2 equals I_{prog} . After programming, I_{prog} is set to zero, and M_4 is opened.

width W of devices. Since current is proportional to W/L , this also introduces gain errors.

We have developed a novel circuit to compensate for current-mode gain errors. The *Programmable-Gain Current Mirror* (PGCM) uses a floating-gate transistor to store a compensation gain factor locally in a non-volatile fashion. Here we describe the theory and operation of the PGCM, which was fabricated in a standard $1.2\ \mu\text{m}$ double-poly CMOS process.

2. CIRCUIT ANALYSIS

The PGCM is shown in Figure 2. We assume that transistors M_1 and M_2 are operating in the subthreshold region of operation, where the drain current is an exponential function of gate voltage. The current through a pFET whose source and well are connected to V_w is given by

$$I = I_0 \exp \left[\frac{\kappa}{U_T} (V_w - V_g) \right] \quad (5)$$

The input current I_{in} sets the voltage V_{in} to

$$V_{in} = V_w - \frac{U_T}{\kappa} \ln \frac{I_{in}}{I_0} \quad (6)$$

The floating gate voltage V_{fg} is given by

$$V_{fg} = \frac{C_{in}}{C_T} V_{in} + \frac{C_c}{C_T} V_c + \frac{C_w}{C_T} V_w + \frac{Q_{fg}}{C_T} \quad (7)$$

where Q_{fg} is the charge trapped on the floating gate, and C_T is the total capacitance seen by the floating node, including the parasitic capacitance between the node and the well, C_w . Formally,

$$C_T = C_{in} + C_c + C_w \quad (8)$$

If we assume for now that V_{prog} is at ground so that $I_{prog} = 0$, and $V_{mode} = 0$ so that this transistor is turned completely on, then we can express I_{out} as

$$I_{out} = I_0 \exp \left[\frac{\kappa}{U_T} (V_w - V_{fg}) \right] \quad (9)$$

Substituting Equations 6 and 7, we derive an expression for I_{out} as a function of I_{in} :

$$I_{out} = (I_0)^{1-\alpha} AB (I_{in})^\alpha \quad (10)$$

where

$$\alpha = \frac{C_{in}}{C_T} \quad (11)$$

$$A = \exp \left[\frac{\kappa}{U_T} \left[\left(1 - \frac{C_{in} + C_w}{C_T} \right) V_w - \frac{C_c}{C_T} V_c \right] \right] \quad (12)$$

$$B = \exp \left[-\frac{\kappa}{U_T} \frac{Q_{fg}}{C_T} \right] \quad (13)$$

The circuit mirrors a power α of the input current multiplied by two gain terms: A , a constant set by the biases V_c and V_w ; and B , a term set by the charge on the floating gate.

We can add charge to the floating gate (thus changing the gain B) through hot-electron injection [8]. If the drain-to-source voltage V_{ds} of a pFET is made sufficiently large (8-10 V in a typical process), the strong electric field between the drain and the channel will induce hot-hole impact ionization. This produces electrons which begin to travel back toward the source, accelerated by the field. Some of these electrons may acquire enough energy to surpass the oxide energy barrier and move into the gate. If the gate is floating (*i.e.*, surrounded by oxide and having only capacitive inputs) then the charge will remain indefinitely until removed by tunneling or by exposing the chip to ultraviolet light. Injection current increases approximately exponentially with V_{ds} , increasing by a factor of ten every 580 mV [8].

To equalize the gains in an array of PGCMs, we apply an input current I_{in} to each PGCM. These input currents could be the outputs of an array of nominally identical translinear circuits that exhibit gain errors. we set $V_{mode} = V_w$ and V_{prog} to a reasonable subthreshold bias, which forces the current I_{prog} through M_2 .

The drain voltage V_w is raised to 10 V, and V_c is adjusted to bias M_2 so that the p FET current is less than I_{prog} . This lowers V_d to near ground, and the large source-to-drain voltage induces hot-electron injection. As the floating gate becomes more negative, the drain current of M_2 will decrease. As the drain current approaches I_{prog} , V_d will begin to rise. As V_{ds} decreases, injection decreases exponentially.

Eventually, all PGCMs will exhibit the same drain current, regardless of the input current. Of course, the M_3 transistors have to match well between circuits, but this is the only device where matching is critical. The exponential slowing of the injection process allows initially disparate floating gate voltages to approach each other asymptotically. Once programming is complete, I_{prog} is set to zero, and V_{mode} is tied to ground for normal operation. The drain voltage V_w is lowered to 3 V to prevent further injection, and V_c is adjusted to compensate for this shift.

3. EXPERIMENTS

We fabricated an array of four PGCMs in a standard 1.2 μm double-poly CMOS process. Our circuits had capacitance value of $C_{in} = 14$ fF and $C_c = 37$ fF. The absolute value of the capacitance was kept to a minimum to maximize bandwidth, but capacitors were made large enough to ensure good matching between circuits. Generally, even small capacitors such as these match very well across a chip [9].

The transfer function I_{out}/I_{in} was measured for each PGCM. Due to random initial charges on the floating gates, the four current mirrors operate with different gains (see Figure 3).

We applied four input currents to the PGCM array: I_{in} , $2I_{in}$, $3I_{in}$, and $4I_{in}$, where $I_{in} = 570$ pA. This simulated the output of four circuits with large gain errors. We set $I_{prog} = 570$ pA, raised V_w to 10 V, and set V_c to 16 V. After ten minutes, we lowered V_w to 3 V, V_c to 7.25 V, and I_{prog} to zero. As we see in Figure 4, the gain errors have been corrected. As predicted in the analysis, the current mirror obeys a power law of $\alpha = C_{in}/C_T$, which was 0.22 for our circuit.

We then left the circuit powered up for 70 hours while current was flowing through the mirrors. Figure 5 shows the long-term stability of the PGCM array. There is a small gain shift, but that could have been caused by a change in room temperature. However, the mirrors remain well matched.

4. DISCUSSION

We have demonstrated a floating-gate circuit that greatly reduces gain errors in current-mode circuits. The circuit uses hot-electron injection to adapt a gain

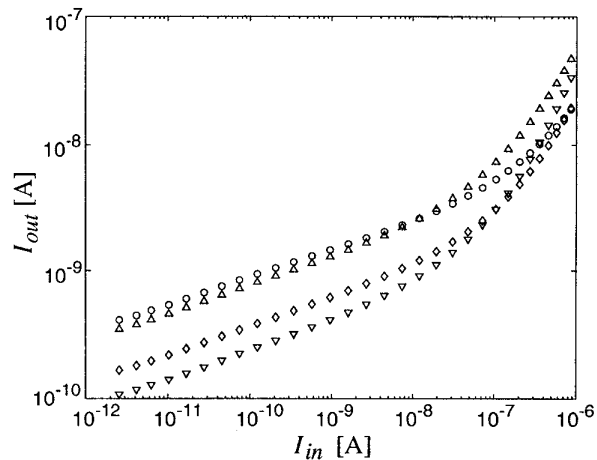


Figure 3. Four PGCMs Before Gain Correction. Due to random initial charges on the floating gates, the four current mirrors operate with different gains.

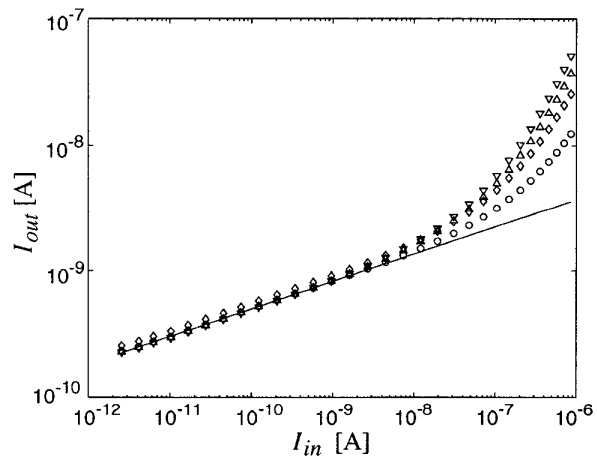


Figure 4. Four PGCMs After Gain Correction. The gains are well matched for subthreshold input currents, and exhibit the behavior $I_{out} \sim (I_{in})^\alpha$, where $\alpha = 0.22$.

to a reference determined by a well-matched n FET. The major limitation of this circuit is its power-law behavior, where the output current is proportional to the input current raised to a power less than one. This behavior could be counteracted by an expansive non-linearity, or it could be exploited a useful computation.

This circuit should work well for audio frequencies. The bandwidth of a PGCM operating around an input current I_{dc} is given by

$$f_c = \frac{g_{in}}{2\pi C} = \frac{\kappa I_{dc}}{2\pi U_T C} \quad (14)$$

where the effective input capacitance C is

$$C = C_{in} \parallel (C_T - C_{in}) = (1 - \alpha)C_{in} \quad (15)$$

which is 11 fF in our implementation. If we modulate a small-signal input around an operating current $I_{dc} = 5$ nA then we have a bandwidth of 1.8 MHz.

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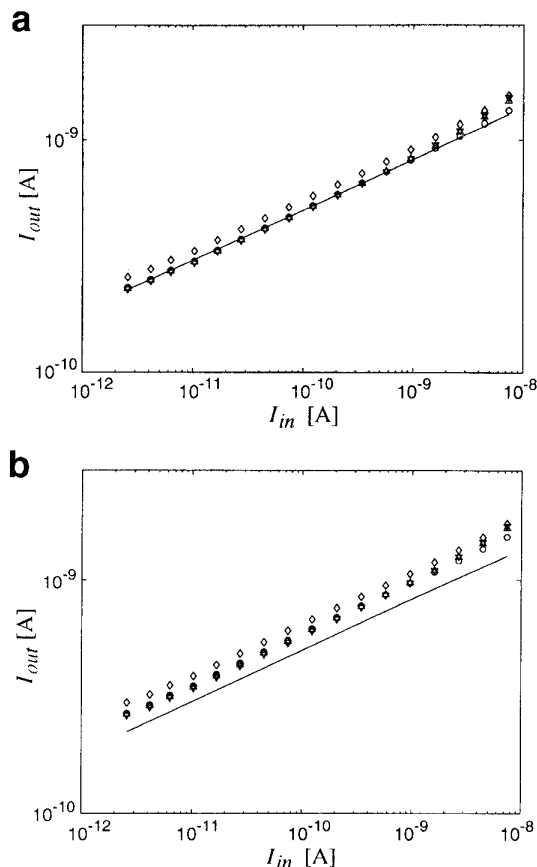


Figure 5. Long-term Stability of PGCMs. (a) Close-up of data from Figure 4. (b) Same characterization performed after 70 hours of circuit operation. The reference line is identical to the line in (a). The gains have shifted slightly (which may be due to drifting biases), but the ensemble remains well matched.

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