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A FLOATING-GATE PFET BASED CMOS PROGRAMMABLE ANALOG MEMORY CELL ARRAY

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ABSTRACT

The complexity of analog VLSI systems is often limited by the number of pins on a chip rather than by the die area. Currently, many analog parameters and biases are stored off chip. Moving parameter storage on chip could save pins and allow us to create complex programmable analog systems. In this paper, we present a design for an on-chip non-volatile analog memory cell that can be configured in addressable arrays and programmed easily. We use floating-gate MOS transistors to store charge, and we use the processes of tunneling and pFET hot-electron injection to program values. With these designs, we achieve greater than 13-bit output precision with a 39dB power supply rejection ratio and no crosstalk between memory cells.

Recent advances in floating-gate CMOS circuits open up the possibility for building on-chip non-volatile parameter storage [1]. Using on-chip parameter storage has many advantages over the conventional use of off-chip potentiometers to supply biases to analog or mixed-mode VLSI chips, as seen in Fig. 1. Setting bias parameters off chip requires one pin per variable (Fig. 1a); moving the analog parameters and circuit biases onto the chip saves more pins for input, output, and diagnostics (Fig. 1b). Such a parameter storage system can be thought of as a series of easily modifiable, on-chip, electronic potentiometers, or **e-pots**. We have presented previously an e-pot design with an nFET-injector structure, which cannot be fabricated in many submicron processes[2, 3].

We have built and tested an array of non-volatile analog VLSI memory cells capable of greater than 13 bits of precision. The analog values, which are stored as charge on a floating gate, are modified through Fowler-Nordheim tunneling and hot-electron injection using a pFET-injector structure. The cells are individually addressable and are capable of sourcing precisely controlled voltages for long periods of time with very little noise or drift and a high degree of power supply noise rejection.

We have demonstrated the ability of this structure to provide bias voltages and bias currents, and intend to use it to allow the construction of complex analog and mixed-mode circuits without sacrificing an excessive number of pins for setting circuit biases. It will also greatly simplify board layout, as a large number of potentiometers can be replaced by a simple digital control system. This array has been laid out in a standard frame and fabricated in a commercially available 1.2μm CMOS process.

1. CIRCUIT DESCRIPTION

The circuit schematic is shown in Figure 2. We configured the e-pot circuits in a 1-D array along the edge of each 2.2mm × 2.2mm chip. Addressing circuitry was included in the arrays(see Fig. 2b). In the 1.2μm process, each e-pot measured 41.4μm × 231.6μm, allowing us to place 39 elements in the array. An e-pot array of

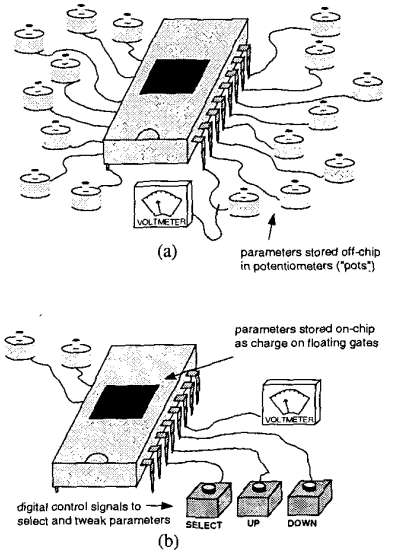

Figure 1: Using electronic potentiometers (e-pots). (a) On typical analog VLSI chips, many of the pins are consumed by bias voltages set with off-chip potentiometers. (b) By storing these voltages on chip, many pins are freed for I/O.

arbitrary length consumes 11 pins for control signals and other biases. Once programming is completed, the array needs only three off-chip biases.

In order to make the e-pots non-volatile, we use floating-gate MOS transistors[1]. A floating gate is a polysilicon node surrounded by SiO_2, trapping charge on the gate indefinitely. The floating gate is connected to the negative input of a high-gain amplifier with a feedback capacitor C_f, pinning the floating gate voltage at V_{ref}, the positive input to the amplifier.

1.1. Controlling the Array

The e-pot elements are arranged in a 1-D array, with only one of those elements being "active" at a given time. It is important to note that e-pots are still sourcing voltage into the chip when they are not active. The first control signal is a clock that advances the shift register depicted in Figure 2b, causing the next E-pot in the array to become active. The vOut pin presents the output voltage of the active e-pot, while the sync output presents a logic high signal

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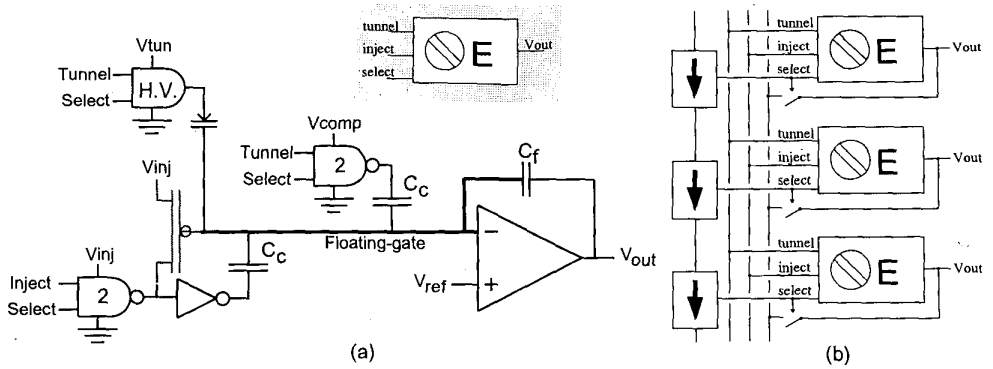

Figure 2: E-pot circuit schematic. (a) Single e-pot cell. The floating gate is connected to the negative input of an amplifier with feedback capacitor C_f. This pins the floating gate voltage to V_{ref}, and allows V_{out} to be moved from rail to rail by changing the charge of the floating gate. Charge is removed from the floating gate through tunneling. The tunneling voltage is switched with a high-voltage differential amplifier built with lightly-doped-drain nFETs. The capacitive coupling of the tunneling voltage to the floating gate is counterbalanced by switching a lower voltage V_{comp} on a larger capacitor. Charge is added to the floating gate through pFET hot-electron injection. An inverter is used in the injection compensation circuitry to offset the capacitive coupling into the floating gate through the drain-to-channel capacitor. Gate 2 is a pseudo-pMOS NAND gate; we use these symbols for clarity. The high-voltage amplifier is shown in Fig. 3. The amplifier is a ten transistor, nFET input, wide output range transconductance amplifier [5]. (b) Array of e-pots with shift register used for addressing. The tunnel, inject, and select lines carry digital signals.

when, after stepping through the entire array, the shift register rolls over and the first e-pot becomes active again.

The tunnel and inject input signals control charge flow onto and off of the floating node, which in turn controls the output voltage of the amplifier. Tunneling, by removing electrons from the floating gate, increases the floating gate voltage and reduces the output voltage. Injection, by placing electrons onto the floating gate, reduces the floating gate voltage and increases the output voltage. The array can be operated either in a "tweakable" mode, where the tunneling and injection signals are controlled directly by the user, or in a "targeted" mode, where external circuitry is used to drive the e-pot output to match the output of a user-controlled analog value.

While tunneling or injecting individual e-pots, we measured no crosstalk to other elements in the array. Figure 4a illustrates the independent control available over the individual e-pots; in this example, the pots have been programmed in a cosine pattern.

We have set e-pots to voltages within 150mV of the ground and power supply rails. When operating within 300mV of the rails, however, the gain of the output amplifier begins to drop off, leading to a dramatic reduction in programming speed. Programming accuracy is actually improved by this phenomenon, as this reduction in gain reduces the effect of the DC offsets generated during tunneling and injection.

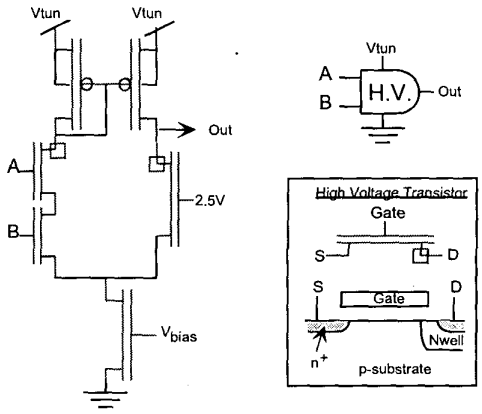

Figure 3: High-voltage AND gate for connecting and disconnecting high voltages to tunneling junctions. Because the required tunneling voltages are often higher than the breakdown voltage of the source-drain regions to the substrate, we need to use high-voltage transistors. A high-voltage transistor is formed by using a drain region made from a lightly doped n-well. These transistors should be made sufficiently long to eliminate punchthrough effects.

1.2. Electron Tunneling and Capacitive Compensation

To decrease an e-pot's output voltage, we remove electrons from its floating gate by the process of Fowler–Nordheim tunneling [4]. This process uses a high voltage source to create an energy barrier thin enough that electrons can tunnel through the gate oxide; typical tunneling voltages used are 27V–30V in 1.2μm processes. Based on other measurements, we expect tunneling voltages in the range of 10V-12V in 0.5μm processes.

We switch these high voltages on chip with a high-voltage differential amplifier built with lightly-doped-drain nFETs, which use well diffusion as their drain regions(see Fig. 3), giving them breakdown voltages greater than 45V. The pFETs in the diffamp are allowed to break down. The diffamp output varies between around 30V in the "on" mode to around 12V in the "off" mode; since the tunneling current depends exponentially on the reciprocal of the oxide voltage, at $V_{\text{tun}} = 12$V there is no observable tunneling current. By switching the tunneling and injection voltages locally, we achieve individually programmable memory cells, with no need for a global erase.

A major limitation of floating-gate memory cells that are programmed by tunneling results from parasitic capacitances between

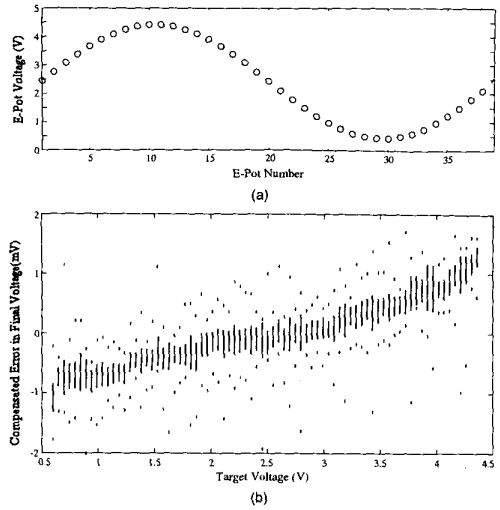

Figure 4: E-pot Programming. (a) Output voltages from all 39 E-pots, after each element in the array had been programmed to a voltage proportional to the cosine of the E-pot position number. No crosstalk was observed between e-pot elements during programming. (b) Deviation of the e-pot programming voltages from their target voltages. We clearly see the 0.05 gain error in this plot. There is a systematic increase in the error as the target voltage increases, due to finite common-mode rejection in our amplifier circuit, We observed a 19.3mV DC offset between the target voltage and the actual output, which can be attributed to imperfect compensation for the output voltage offset that takes place during injection. The vertical bars show the standard deviation of the error over 64 trials, while the points show the minimum and maximum observed errors. This deviation comes from noise in both the floating-gate amplifier and in the instrumentation circuitry.

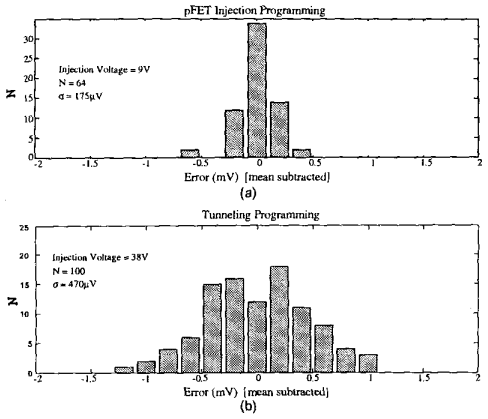

Figure 5: (a) Histogram for programming with pFET hot-electron injection- 64 trials. (b) Histogram for programming with tunneling- 100 trials. In both cases, the target voltage was 3.0V. Both processes give a precision (V_{dd} range divided by σ) of greater than 13 bits; pFET injection gives the higher precision, with nearly 15 bits.

the tunneling node and the floating gate. The switching of the tunneling voltage couples into the floating gate, causing a large voltage offset in the e-pot output. Since capacitors connected to floating gates are DC elements, this voltage offset does not decay away, but rather is present for the duration of tunneling, making for indirect and awkward programming.

In order to make our memory cells "tweakable," we compensate for this effect by switching a lower voltage on a larger capacitor in the opposite direction. When we switch the tunneling junction to a high voltage, we simultaneously switch another node from a positive "compensation voltage" to ground. This node is coupled to the floating gate with a capacitance that is many times larger than the tunneling junction capacitance. The compensation voltage $V_{\rm comp}$ is set by an off-chip bias, so the capacitive coupling can be precisely nulled by the user.

1.3. Hot-Electron Injection

To increase the e-pot output voltage, we can add electrons to the floating gate by the process of pFET hot-electron injection. We use pFET hot-electron injection, because this effect is usable across most submicron processes [1]. To perform pFET injection, we place a large voltage($>$ 7V) across the source and drain of a normal pFET, while holding the gate voltage below that of the source. Switching this large voltage to activate the hot-electron injection process causes a step change in channel voltage which, by capacitive coupling, causes an offset in the floating gate voltage. To counteract these effects, we tie the switching node to the input of an inverter, the output of which is also capacitively coupled to the floating gate. By adjusting the size of this coupling capacitor prior to fabrication, we can tune the system to reject injection offset for a specific combination of power supply and injection voltages. The resulting compensation system works well within that narrowly defined voltage range, but as either voltage is changed the offset voltage becomes significant. In principle, we could compensate for this offset in the same way that we deal with tunneling offset, but to do so would require another off-chip bias.

2. CIRCUIT PERFORMANCE

2.1. Programming Accuracy and Precision

In order to program voltages precisely, we used a comparator in a feedback loop with the e-pot output voltage, so that the tunneling or injection controls were triggered by the comparator output. In order to measure the accuracy of the memory cell, we programmed the same voltage multiple times and measured the error between the resulting voltage and the target voltage. To quantify precision, we computed the standard deviation of the resulting voltages.

To measure the accuracy and precision of the e-pot output over a wide range of target voltages, we programmed a single pFET-injector e-pot to produce a series of 79 voltages, uniformly spaced between 0.6V and 4.4V. At each step, we recorded both the target voltage and actual output, finding remarkably little deviation from ideal performance across the tested range. Figure 4 shows how the observed output error varies as a function of the target voltage once the previously mentioned DC offset has been removed. The vertical bars show the standard deviation of the error over 64 trials, while the points show the minimum and maximum observed errors. There is a systematic increase in the error as the target voltage increases, due to the finite CMRR of the output amplifier; as the output voltage shifts in response to injection switching, the gain applied to that shift is, to some degree, a function of the output voltage. Figure 5 shows the distribution of output errors after multiple attempts to program a given target voltage (3.0V). The standard deviation when tunneling to the target was 470μV, corresponding to

greater than 13-bit precision over the 4.7V operating range of the e-pot. When approaching the target by pFET injection, the e-pot demonstrated a standard deviation of 175μV over its 4.7V operating range, giving an effective precision of 14.5 bits. This precision may improve when the e-pot is operated in a low-noise environment.

2.2. E-pot Output Noise

The total RMS noise present on the e-pot-supplied output voltage was on the order of 1-2 mV. In order to determine the noise components present in the e-pot voltage, we measured the frequency spectrum of a pFET-injector e-pot output. The resulting spectrum, shown in Figure 6, shows conventional 1/f noise, as well as thermal device noise at higher frequencies. This noise could be reduced by using larger transistors in the output transconductance amplifier, at the cost of increasing the e-pot element size and thereby reducing the number of e-pots that could be placed on a single chip. These noise properties are similar to other floating-gate amplifiers [6]. We showed elsewhere that the tunneling and injection processes do not contribute significantly to the noise levels [6].

The e-pot output noise comes directly from the generated noise of the wide-output range transconducance amplifier [5]. We use the result that effective current noise of this transconductance amplifier is roughly 5.3 times that of the bias current transistor [8]. We calculate elsewhere that the total output-noise power is [3]

$$\hat{V}_{out}^2 = \frac{10.6q(I/g_m)}{C_L + C_f}. \quad (1)$$

The total output-noise power is inversely proportional to $C_L + C_f$; therefore, a larger capacitor can be used to decrease the total noise. The lowest total output-noise power occurs at subthreshold current biases. We define dynamic range, DR, of this e-pot as the ratio of the maximum possible linear output swing to the total output-noise power. For a 5V supply, we can assume conservatively that we have a 4V linear range (V_{max}). With this definition, and assuming that the e-pot is biased in subthreshold $I/g_m = U_T/\kappa$, we can express the e-pot dynamic range as

$$DR = \frac{V_{max}^2}{2\hat{V}_{out}^2} = \frac{1.51V^2\kappa(C_L + C_f)}{qU_T} \quad (2)$$

which is similar to the form for dynamic range for the wide-linear-range amplifier. Using typical C_f capacitors of 2pF at room temperature (T = 300K), we calculate the dynamic range as approximately equal to 84dB (14 bits).

2.3. Power Supply Rejection

The inset of Figure 6 shows how the e-pot output voltage changes in response to variation in the power supply voltage. As the supply voltage decreases, the output voltage increases linearly, with a Power Supply Rejection Ratio of 39dB. This is another advantage the e-pot structure has over a conventional bank of potentiometers, each of which has an average PSRR of 6dB. Since the output transconductance amplifier is the only e-pot component with a direct connection to the supply voltage, we believe that these variations are due entirely to this amplifier. By optimizing device lengths, and thereby increasing the output amplifier's open-loop gain, the PSRR could be further increased, at the cost of increasing the size of each e-pot element.

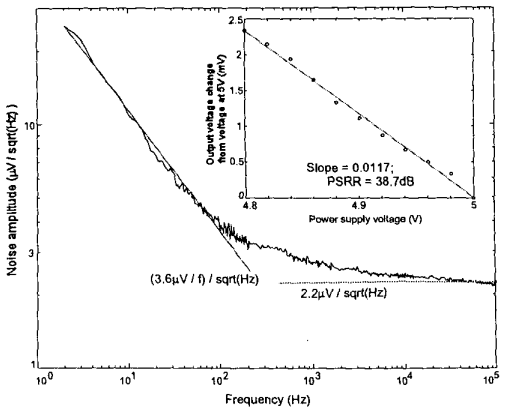

Figure 6: Noise spectrum from an on-chip e-pot cell. We see two types of noise, conventional $1/f$ noise at low frequencies, and the $1/f^{(1/2)}$ thermal noise characteristic of pFETs operating in weak or moderate inversion. We also plot lines showing curve fits to these regions of noise. **Inset:** Deviations from ideal output voltage due to changes in the power supply voltage. All e-pot bias voltages, which are ground referenced, were fixed for these measurements.

2.4. Long-term Drift of the Output Voltage

Once a voltage has been programmed, it is important that it remain stable for long periods of time. To test the e-pots stability, we monitored the output voltage of a single e-pot over a 70 hour period. The output voltage increased almost 20mV in the first 36-40 hours, after which it settled to a stable value. This initial increase appears to be due to electron detrapping, as electrons that had become trapped in the gate oxide during injection slowly worked their way out of the oxide and into the floating gate itself. After 40 hours, the population of trapped electrons had been significantly reduced, and the output voltage stabilized. Additionally, we observed no significant change in an e-pot array's stored values after one month of disuse.

3. REFERENCES

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