A Multilevel Modular Capacitor Clamped DC-DC Converter

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***Abstract*—A novel topology of multilevel modular capacitor clamped dc-dc converter (MMCCC) will be presented in this paper. In contrast to the conventional flying capacitor multilevel dc-dc converter (FCMDC), this new topology is completely modular and requires a simpler gate drive circuit. Moreover, the new topology has many advantageous features such as high frequency operation capability, low input/output current ripple, lower on-state voltage drop, and bi-directional power flow management. This paper discusses the construction and operation of the new converter along with a comparison with a conventional converter. Finally, the simulation and experimental results validate the concept of this new topology.**

I. INTRODUCTION

Multilevel dc-dc converter is becoming more popular for its high efficiency power conversion. There are several different types of multilevel dc-dc converters that have been previously developed [1-7][9-10]. The flying capacitor multilevel converter shown in [1][3] has some potential features to be used in automotive applications such as hybrid electric vehicles to manage power transfer between different voltage level buses.

There are several inherent limitations of any FCMDC. The major drawback is the voltage balancing among the capacitors used in the circuit. This phenomenon is profoundly observed in [1][4-5] where all the capacitors are connected in series during the charging period. The number of capacitors used in the circuit depends on the number of levels used, and it is governed by the up/down conversion ratio requirement. Thus for a 5-level converter, there will be 5 capacitors connected in series during the charging period which may introduce a capacitor charge unbalance situation. Moreover, the stress voltages across the switches are not equal. The top-level transistors experience more voltage stress than the bottom-level transistors, and for a 5-level application the maximum ratio of voltage stress of the transistors from top level to the bottom level is four. For these two main flaws, the circuit cannot be considered as a modular circuit, and modifications need to be introduced for capacitor charge balancing.

The second contender of an FCMDC considered in this paper is the converter [3] shown in Fig. 1. This conventional circuit suffers from several limitations. First, this conventional circuit does not have a modular structure. For this reason, the circuit cannot be easily extended to increase/decrease the number of levels, hence changing the conversion ratio. The other major limitation is the complicated switching schemes for the different transistors shown in Fig. 2. For the convenience of explaining the operation of the circuit, it is considered that power is transferred from the high voltage battery to the low voltage battery and associated loads.

During one operating cycle, only one sub-interval is associated with the energy extraction from the high voltage side battery in this converter. During the other sub-intervals, energy stored in capacitor C_5 is transferred to the other capacitors through the output circuit. Thus, when the conventional converter is designed with a high conversion ratio, one capacitor takes energy from the high voltage battery for a period of one over the conversion ratio. This is not a serious issue when the conversion ratio is low. However, when the conversion ratio is high such as 5, only a small timeframe is allowed to transfer the energy from the voltage source to the capacitor, and from the capacitor to the next level capacitors as well. Sometimes it is desirable to operate the circuit at high frequency to reduce the capacitor sizes [3]. However, when the transition time (rise time and fall time) of a transistor is comparable to the ON time (t_{on}) of it, the circuit becomes inefficient. For an N-level converter, the ON time for any transistor shrinks to $(1/N)^{th}$ of the total time period, and the effective switching frequency is N times of the original switching frequency. This increased effective switching will introduce high frequency ripple at the output dc voltage. While charging a battery, this high frequency ripple causes additional heating inside the battery and this effect is bad for the health of the battery. For these reasons this circuit cannot be operated

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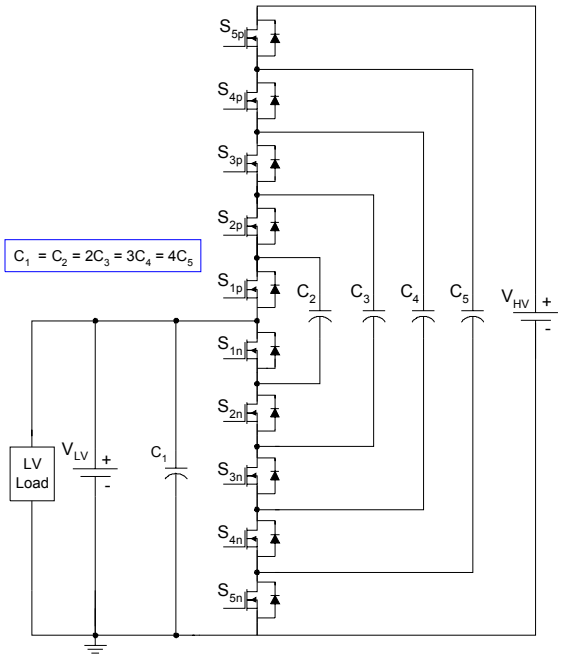


Fig. 1. A conventional 5-level FCMDC.

at high frequency.

The excessive voltage drop across the active switches or diodes inside the converter is another flaw of the conventional FCMDC. This can be seen from Fig. 1. During any subinterval, 5 transistors/diodes are turned on, and the input/output current flows through these five transistors/diodes. In fact, for an N-level converter, a total number of N transistors/diodes are intended to flow the current, which could add a severe voltage drop across them during high power applications. As this operation takes place N times in a complete cycle, the dynamic loss can also be excessive [4][8]. Thus, the remedy to this flaw would be to obtain a circuit such that the number of devices in a series path is significantly less. By obtaining a new circuit, the voltage regulation of the converter can be substantially enhanced and dynamic loss can be reduced.

The incapability to withstand any fault in the converter is another major drawback. To form a 5-level converter, 10 transistors are required and if any one of these transistors fails, there is no way to continue the operation of the circuit. Hence, the circuit configuration is non-modular, so no redundancy can be incorporated in the circuit.

In the proposed application where the converter is responsible to transfer power from a high voltage battery to a low voltage battery or vice-versa, the direction of power flow depends on the voltages at the two ends. For a 5-level converter, if the voltage at the high voltage side battery is more than five times of the low voltage battery, then the power is transferred from high voltage side to the low voltage side. In the same token, if the high voltage side battery voltage is less

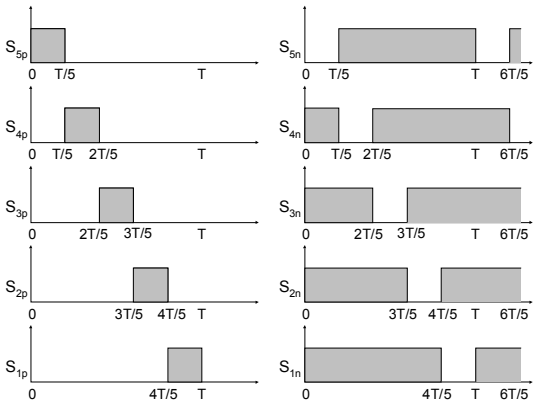


Fig. 2. The switching scheme of the conventional FCMDC.

than five times of the low voltage battery, then power is transferred from low to high voltage side battery. This property of power flow indicates the incapability of having a true bi-directional power flow where the direction will not depend on the battery voltages. Table 1 summarizes the possible cases where the converter fails to establish bi-directional power management. In automotive applications, the battery voltage at the two ends can vary within a wide range, though power transfer may be required in either direction irrespective of the two end battery voltages.

Thus, the limitations of the conventional flying capacitor converter can be summarized as: 1) Non-modular structure, 2) complicated switching scheme, 3) difficulty in high frequency operation, 4) excessive voltage drop across the switches/diodes, 5) higher dynamic switching loss, 6) lack of bi-directional power management, and 7) No fault bypass capability.

TABLE 1. DIRECTION OF POWER FLOW AT DIFFERENT BATTERY VOLTAGES.

Case	Ratio of battery voltages	Power flow direction	Power flow from high side to low side	Power flow from low side to high side
1	>5	High to Low	Possible	Not possible
2	<5	Low to High	Not possible	Possible

II. THE NEW TOPOLOGY

The proposed 5-level MMCCC shown in Fig. 3 has an inherent modular structure and can be designed to achieve any conversion ratio. Each modular block has one capacitor and three transistors leading to three terminal points. A modular block is shown in Fig. 4. The terminal V_{in} is connected to either the high voltage battery or to the output of the previous stage. One of the output terminals V_{next} is connected to the input of the next stage. The other output terminal V_{LB} is connected to the low voltage side + battery terminal.

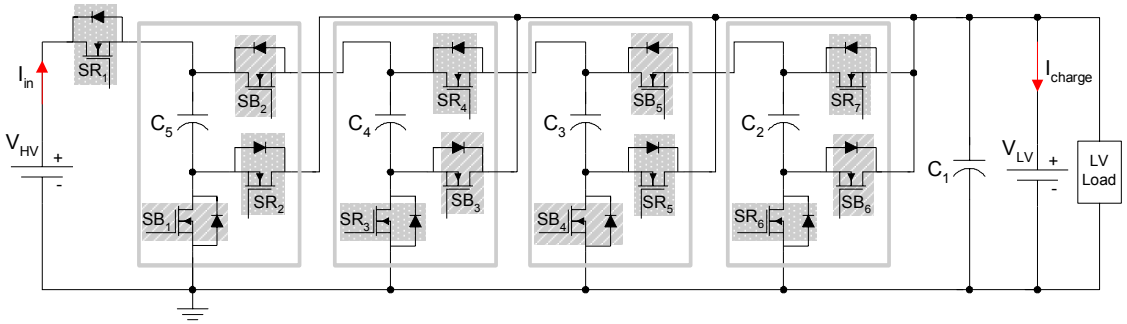


Fig. 3. The proposed 5-level MMCCC with four modular blocks.

In a conventional converter with conversion ratio of 5, the total operation takes 5 sub-intervals, which is shown in Fig. 2 and Table 2. It is seen that only one charge-discharge operation is performed in one sub interval. Thus, the component utilization is poor in this circuit. For an N-level converter, any capacitor except C_1 is utilized during only two sub-intervals for a complete cycle (one sub interval for charging, one for discharging) and for the remaining three sub-intervals in one period, the component is not used. The new converter introduced here can increase the component utilization by performing multiple operations at the same time, which is shown in Table 2 also.

In Fig. 5, the simplified operational circuit of the MMCCC is shown. To get the new switching scheme, it is initially assumed that the new converter will perform the entire operation in 5 sub-intervals and later on it will be shown how these five operations can be done in two sub-intervals. Fig. 5(a) shows the first sub-interval where C_5 is being charged from V_{HV} through the output circuit. In the second sub-interval, C_5 will transfer the charge to C_4 through the output circuit, and this operation is shown in Fig. 5(b). During the third sub-interval, C_4 releases energy to C_3 through the output circuit as shown in Fig. 5(c). So far, these operations are the same as the conventional FCMDC. Interestingly,

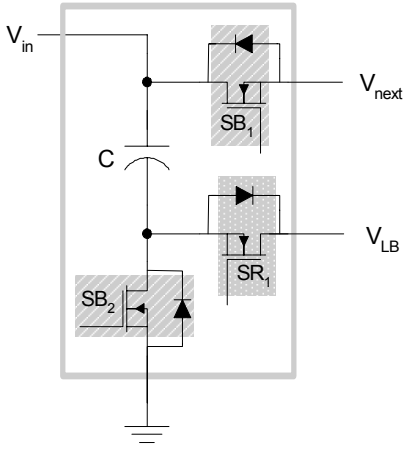


Fig. 4. The unique modular block.

TABLE 2. SWITCHING SCHEMES OF CONVENTIONAL CONVERTER AND THE NEW CONVERTER. ↑ = CHARGING, ↓= DISCHARGING

Conventional Converter		New Converter	
Sub interval No.	Operations	Sub interval No.	Operations
1	$V_{HV\rightarrow} C_5\uparrow_+ C_1\uparrow$	1	$V_{HV\rightarrow} C_5\uparrow_+ C_1\uparrow$
2	$C5\downarrow_\rightarrow C4\uparrow_+ C1\uparrow$		$C4\downarrow_\rightarrow C3\uparrow_+ C1\uparrow$
3	$C4\downarrow_\rightarrow C3\uparrow_+ C1\uparrow$		$C2\downarrow_\rightarrow C1\uparrow$
4	$C3\downarrow_\rightarrow C2\uparrow_+ C1\uparrow$	2	$C5\downarrow_\rightarrow C4\uparrow_+ C1\uparrow$
5	$C2\downarrow_\rightarrow C1\uparrow$		$C3\downarrow_\rightarrow C2\uparrow_+ C1\uparrow$

during this third sub-interval, the charging operation of the first sub interval (C_5 gets charged from V_{HV} through the output circuit) can be performed without perturbing the operation of the entire circuit, which is shown in Fig. 5(c) also. Thus in this stage, two operations are performed at the same time, and C_5 gets energy for the second time through the output circuit.

During the 4th sub-interval, the same operation of Fig. 5(b) can be performed. In addition to that, C_3 can transfer energy to C_2 through the output circuit without perturbing the entire operation. Thus, two operations can take place at the same time. These operations are shown in Fig. 5(d). In this way, all the steps shown in Fig. 5(a) to (d) are the initialization steps where all the capacitors are being charged and ready to get into the steady state operating conditions.

In the fifth stage shown in Fig. 5(e), C_5 is again energized from V_{HV}, and C_4 transfers energy to C_3. C_2 was charged in the previous stage, and now it transfers the energy to the output circuit. Thus three operations take place at the same time, which are independent of each other. The operations that took place in Fig. 5(d) are repeated again in the sixth step, which is shown in Fig. 5(f). Thus these two steps shown in Fig. 5(e) and (f) are the steady state operations of the converter where the 4th step and the 6th step are the same. The simplified diagram shown in Fig. 5(e) is defined as state 1 during steady state, and the diagram in Fig. 5(f) is the state 2 during steady state operation. Once all the capacitors are

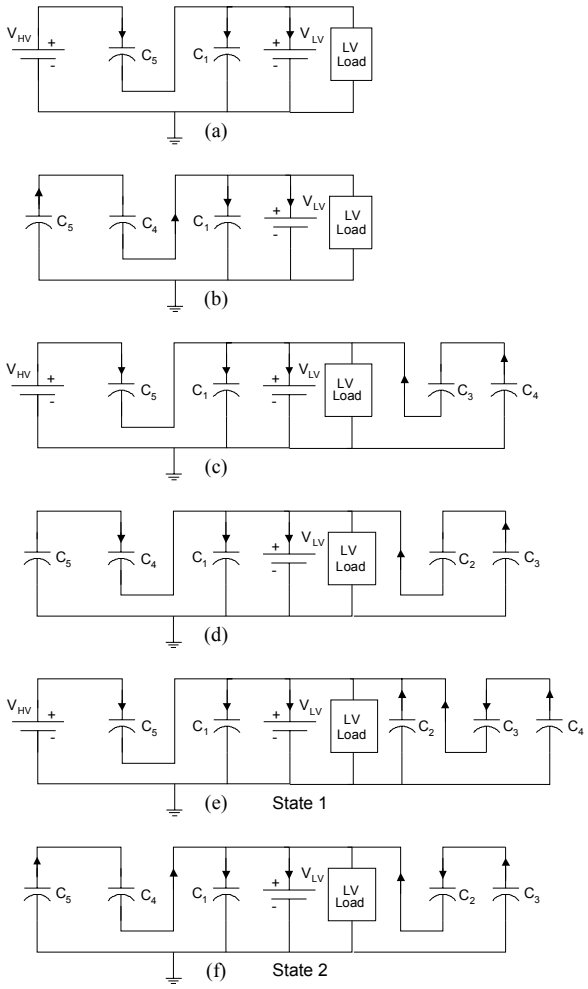


Fig. 5. The simplified diagram of the new converter using the switching scheme of the conventional converter.

charged after the initialization stage, the circuit enters into the steady state and state 1 and state 2 will be repeated in every clock cycle.

The switching sequence in the new converter works in a simpler way than the conventional converter. As there are only two sub-intervals, two switching states are present in the circuit. Following this fact, switches SR_1 to SR_7 in Fig. 3 are operated at the same time to achieve state 1; the equivalent circuit is shown in Fig. 5(e). In the same way switches SB_1 to SB_6 are operated simultaneously to make the steady state equivalent circuit shown in Fig. 5(f). This new switching pattern is shown in Fig. 6.

The simpler switching scheme enables high-speed operation for the new MMCCC circuit. In a conventional FCMDC, the permitted time for charging/discharging of any capacitor depends on the conversion ratio. Thus for a 5-level converter running at frequency f_s, the allowable charging/discharging time is

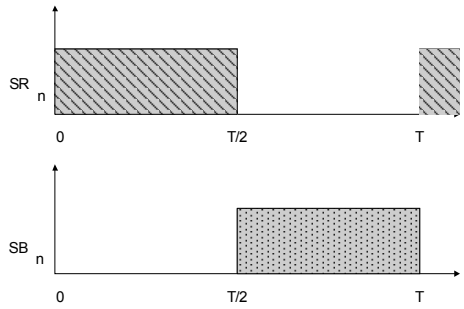


Fig. 6. The gating signal of the switches in the new circuit, i.e. there are only two switching states present in the circuit.

$T_s/5$ ($T_s = 1/f_s$). If this time is the minimum for a complete charging/discharging operation, the switching frequency of the circuit must be less than or equal to f_s. However, this problem is eliminated in the new converter by virtue of the new switching scheme. As there are only two switching states, the switching frequency can be made $2.5f_s$ by keeping the same charging/discharging time $T_s/5$.

Table 1 shows that a conventional FCMDC suffers from true bi-directional power management. To eliminate this problem, the new converter uses one additional level to achieve more voltage at the output side during the up conversion operation. During the down conversion, more power can be transferred from the high voltage side to the low voltage side by reducing the number of levels to four. As long the circuit is modular, it is possible to change the number of levels by adding or bypassing any redundant levels in the circuit. The duty ratio is changed also when the conversion ratio is deviated from 5. This method can be simultaneously used to bypass a faulty module with uninterrupted operation.

III. Simulation Results

To compare the performance of the new converter, a 6-level converter was simulated in PSIM along with the conventional converter. Both of them were simulated in three modes listed in Table 3. Fig. 7(a) shows the output voltage of an FCMDC in down conversion mode. With a 75 V input voltage and a conversion ratio of 6, the output voltage of this converter should be close to 12 V. Fig. 7(b) shows the output voltage of the MMCCC, and clearly it produced an output voltage close to 12 V, which could not be obtained from the conventional FCMDC.

Fig. 7(c) shows the input current of the conventional converter, and Fig. 7(d) shows the same for the new converter. This shows that the peak current stress for the new converter is 2.5 times smaller than that of the conventional converter. This feature will ensure higher reliability and the freedom of using smaller size transistors.

Fig. 8 shows the simulation results in the up conversion mode. When the low voltage side is energized by a 12 V source and the high voltage side is loaded by a 30 Ω load, the conventional converter produces an average output of only 37 V and the new MMCCC produces very close to 60 V. They are shown in Fig. 8(a) and (b) respectively. Fig. 8(c) and (d) shows the input currents taken from the 12 V source and the ripple present in the MMCCC is substantially less than the conventional converter. Moreover, it takes more power from the 12 V source and transfers it to the high voltage side. By virtue of the higher component utilization, the MMCCC can deliver more power than

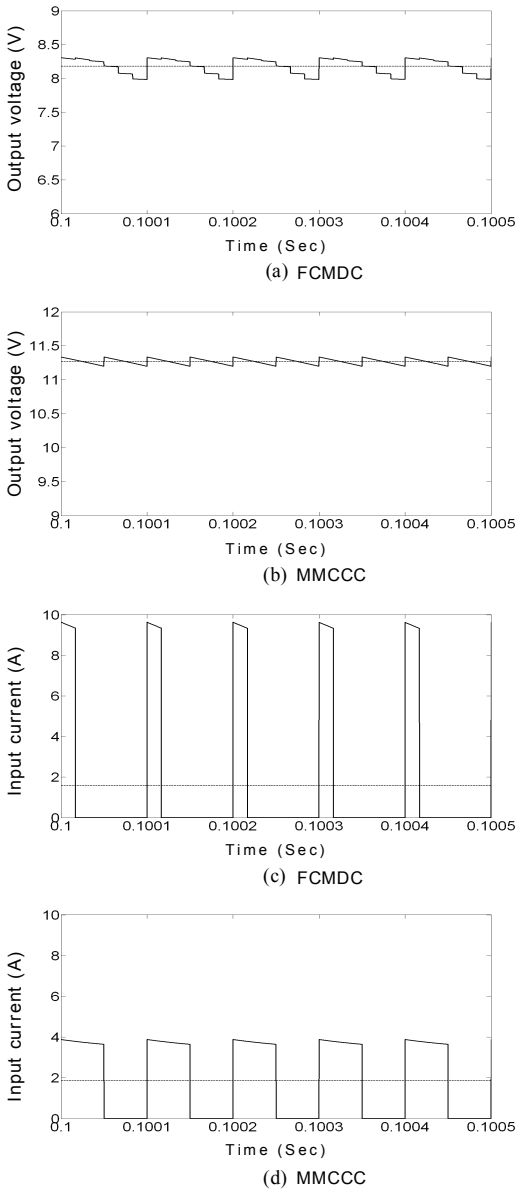


Fig. 7. The converters' simulation results in down-conversion mode, (V_{in} = 75 V, R_{load} = 1 Ω).

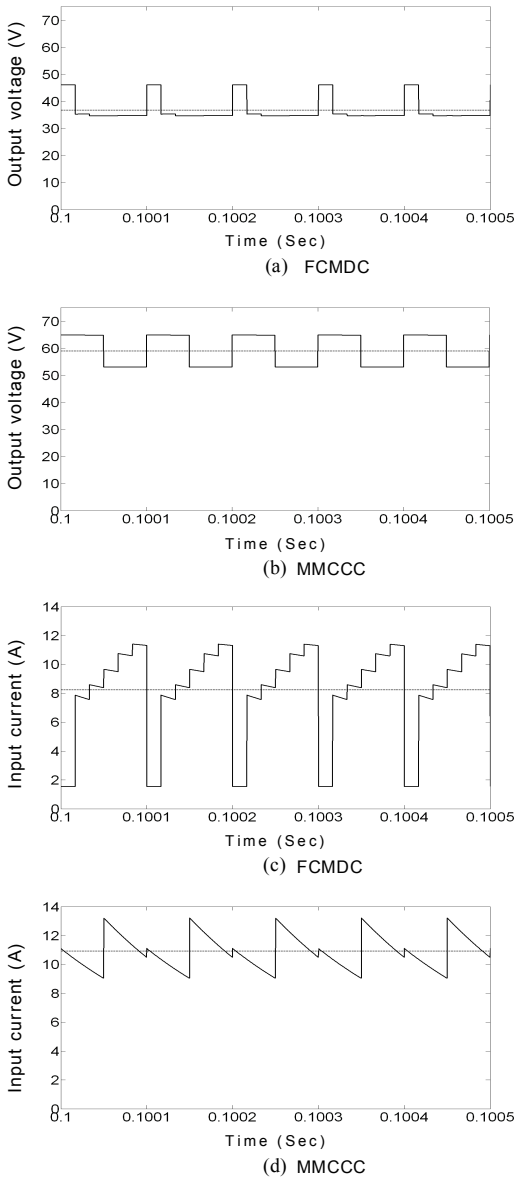


Fig. 8. The converters' simulation results in up-conversion mode, (V_{in} = 12 V, R_{load} = 30 Ω).

the conventional converter using the same components.

Fig. 9(a) to (d) shows the simulation results in the battery-charging (down conversion) mode. They clearly show that the average output charging current of the MMCCC is substantially higher than the conventional circuit although the input (high voltage side) peak current is almost the same for both the cases.

IV. Features of the New Proposed Topology

A. Advantages

The simulation results and the schematic of the new design explain many of its potential features. The new circuit is modular and requires a simple gate drive circuit. As there are only two switching states present in the circuit, the switching ripple present at the output is

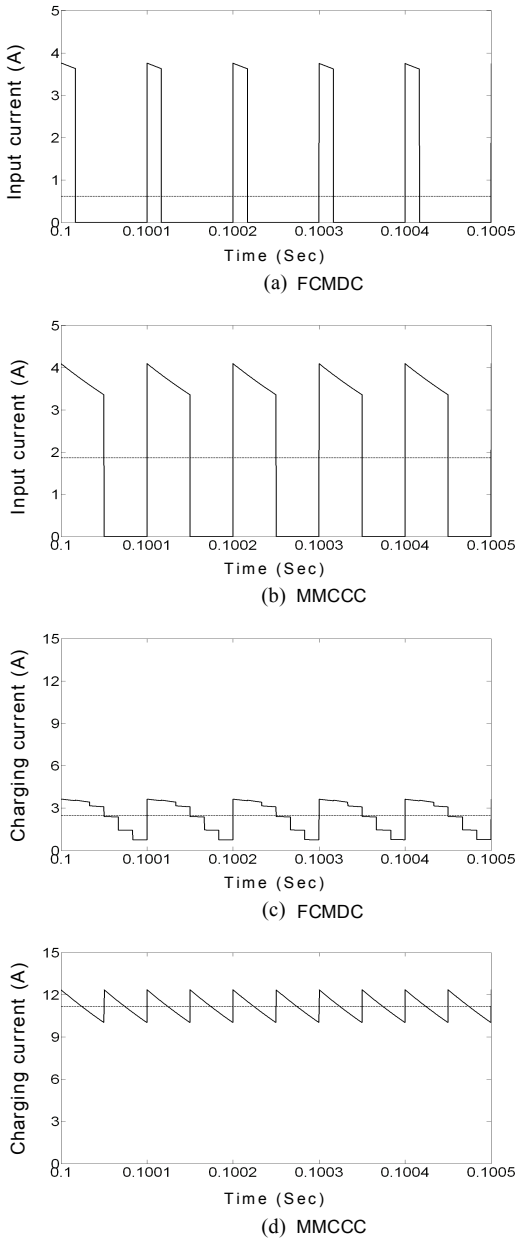


Fig. 9. Simulation results of the converters' battery charging performance in down-conversion mode (V_{in} = 80 V).

always two times of the frequency of the gate drive signal, whereas the effective switching frequency is N times of the gate drive signal for an N-level conventional converter. The new converter can be operated at a clock frequency N/2 times higher than the FCMDC where N is the conversion ratio. This feature permits the designer to use small size capacitors to attain the same output current capability.

The new converter has much better voltage regulation compared to the conventional converter. In up conversion mode, the FCMDC's input current flows though (N-1) series connected transistors and 1 diode.

TABLE 3. DIFFERENT MODES OF THE SIMULATION

Mode	V_{in} (V)	Output load	Battery Voltage
Down conversion	75	1 Ω	NA
Up Conversion	12	30 Ω	NA
Down conversion with battery charging	80	NA	12 V

The situation will be worse when the conventional converter attempts to deliver current from the high voltage side to low voltage side. During this time the current flows through (N-1) diodes and only one transistor. Usually the voltage drop across the diode is higher than the voltage drop across any transistor and thereby the regulation is very poor during this time. In contrast, the current flows through at most three transistors or diodes in the new converter irrespective of the conversion ratio. The reduced number of series connected devices in the new converter is responsible for less voltage drop and better regulation.

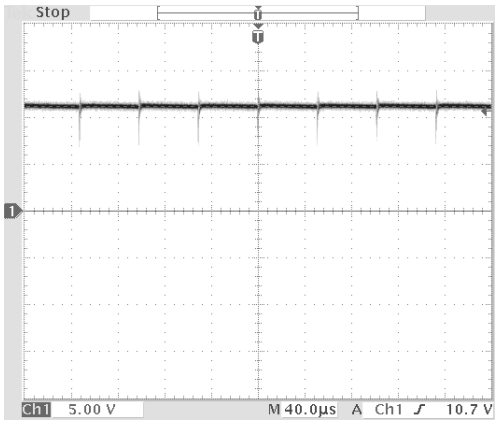
B. Disadvantages

The new circuit suffers from one limitation. The MMCCC uses more transistors than what is required for the conventional FCMDC with the same conversion ratio. For an N-level design, the conventional converter requires 2N transistors whereas the new converter needs (3N-2) transistors. Thus for a five level design, the conventional converter needs 10 transistors; 13 transistors are needed for the new converter. However, the use of more transistors is truly compensated by obtaining all the desirable features from the new converter.

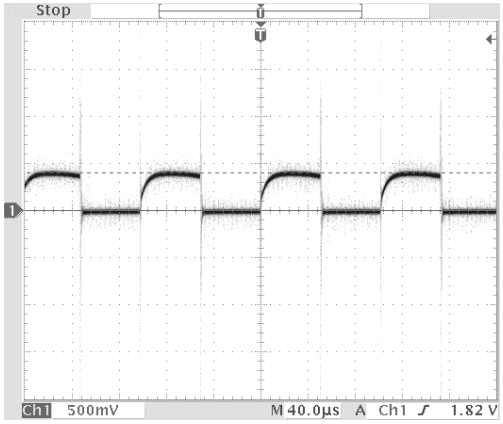
V. EXPERIMENTAL RESULTS

A 6-level prototype of the proposed design has been constructed on the printed circuit board shown in Fig. 14. For a 6-level design, 5 modules are used and each module will have its own gate drive circuit on board. Inside one module, two bootstrap gate drive circuits (IR2011) have been used to drive three IRFI540N MOSFETs. These MOSFETs have an on state resistance of 52 mΩ and they are rated at 20 A. An onboard dc-dc converter has been used to drive the top transistor in each module (Transistor S_{B1} in Fig. 4). General-purpose 1000 μF 100 V electrolytic capacitors having 0.1 Ω ESR have been used in the circuit. A main board has been built in such a way that each module is connected to the main board through a 10-pin header. Thus if there is any fault in any one of the modules, either it can be bypassed by the onboard fault clearing circuit or it can be physically disconnected from the main board and can be replaced by another good module.

A Fluke 87 III multimeter has been used to measure all the voltages and currents. Like the simulation, this 6-level converter was tested in three steps. In the first step,



(a)



(b)

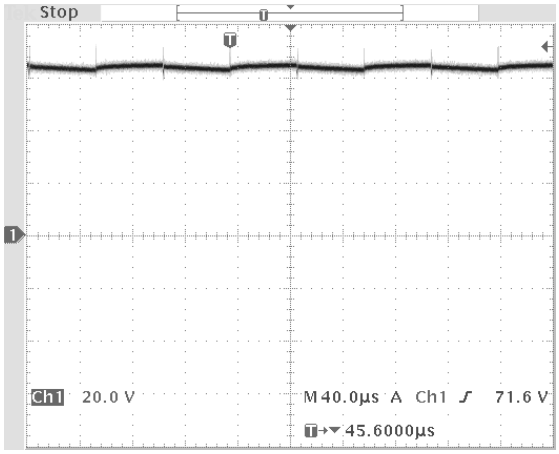
Fig. 10. The experimental results for the down conversion mode, a) output voltage, b) input current (1 V = 10 A).

the down-conversion operation was tested by connecting a 75 V source to the high voltage side of the converter. A 1 Ω resistive load from a 3711A programmable load bank was connected across the output, and the voltage wave shape was recorded. Because of the resistive nature of the load, the current will have the same wave shape like the voltage wave. Fig. 10(a) shows the output voltage of the MMCCC, and Fig. 10(b) shows the input current wave shape. Thus the peak input current was found to be 4 A (400 mV drop across a 0.1 Ω resistor), which is the same as found in the simulations (Fig. 7(d)).

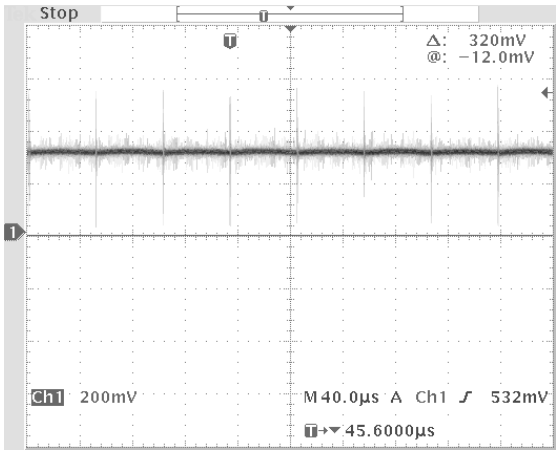
Fig. 11 summarizes the experimental results in the up conversion mode. In this up conversion mode, a 65.3 V output is produced from a 12 V input with 30 Ω loading at the high voltage side. The output voltage is shown in Fig. 11(a). The input current is shown in Fig. 11(b).

In the battery-charging mode, an 80 V source was connected at the high voltage side, and the low voltage side of the converter was connected to the battery. Fig. 12(a) shows the input current and (b) shows the output or charging current. For this setup, the maximum charging current to the 12 V battery was only 1.2 A which is much less than the simulation result. The reason for this low current was the increased battery voltage, which was eventually 13.2 V while taking the measurement. In the simulation, the battery voltage was considered constant at 12 V.

The converter was tested to measure the efficiency at different operating conditions. Fig. 13 shows the efficiency of the converter at different loading conditions for both up and down conversion mode, and Fig. 14 shows the actual prototype. A maximum efficiency of 99.1% was achieved at 20 W power output (in up-conversion mode). The relatively higher on-state resistance (52 mΩ) of the transistors causes the efficiency to drop at higher loading conditions. However, when the converter will be designed for higher power rating, larger MOSFETs will ensure low on-state loss and better efficiency at higher output power.

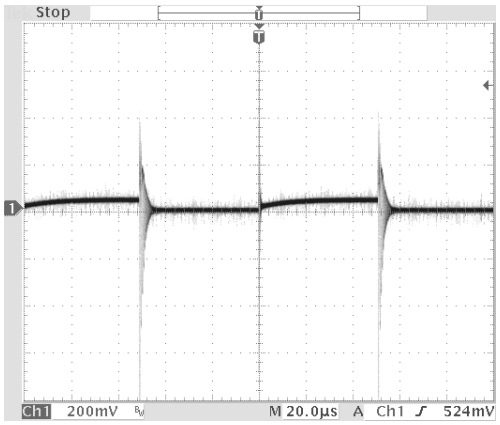


(a)

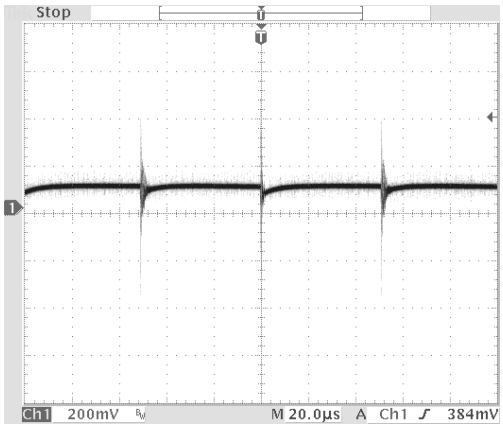


(b)

Fig. 11. The experimental results for the up conversion mode, a) output voltage, b) input current (100 mV = 4 A),



(a)



(b)

Fig. 12. The experimental results for the battery charging mode, a) input current (100 mV = 1 A), b) charging current (100 mV = 1 A).

VI. CONCLUSIONS

A new topology of modular multilevel dc-dc converter has been proposed and validated by both simulation and experimental results. The new converter outperforms the conventional converters by having complete modular construction, high power transfer capability, simpler gate drive circuit requirement, high frequency operation capability, onboard fault bypassing, and bi-directional power management capability. By virtue of the modular topology, the circuit obtains redundancy and the reliability can be increased significantly. The modular nature also introduces the use of one additional level to establish the fault bypassing and bi-directional power flow management. Thus this converter could be a suitable choice in various applications to establish a bi-directional power management between buses having different voltages.

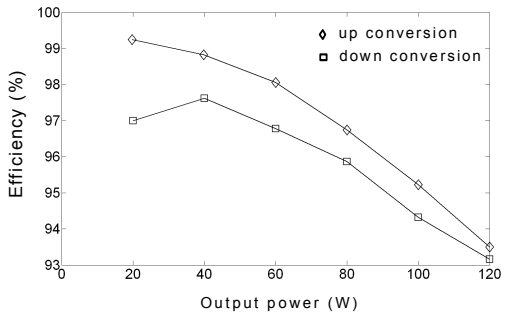


Fig. 13. The efficiency of the MMCCC at different power output.

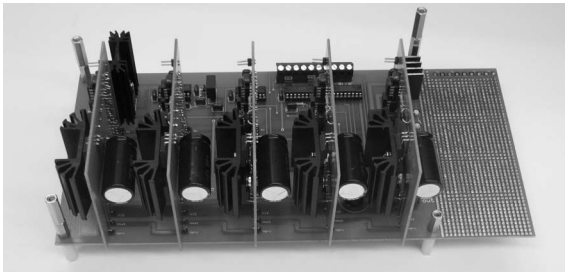


Fig. 14. The actual 6-level prototype.

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