LATERAL DOPANT PROFILING IN MOS STRUCTURES ON A 100 nm SCALE USING SCANNING CAPACITANCE MICROSCOPY

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ABSTRACT

Scanning capacitance microscopy and atomic force microscopy have been used to image the extent of lateral dopant diffusion in MOS structures. The data are capacitance vs. voltage measurements made on a submicron scale. The technique is non-destructive when imaging uncleaved samples. New experimental data are presented here on actual, cleaved device structures which clearly indicate the two-dimensional dopant profile in terms of a spatially varying modulated capacitance signal. First-order deconvolution indicates the technique has much promise for the quantitative characterization of dopant profiles. The potential of the technique to illuminate important device-related phenomena on a local scale is also discussed.

INTRODUCTION

Present-day VLSI device technology demands accurate knowledge of the spatial extent in three dimensions (3-D) of active impurity dopants which have been incorporated into the discrete device elements. The active region of a MOSFET device is engineered by incorporating dopants, such as, As, B, or P, in a concentration range of 10^{15} to $10^{20} cm^{-3}$. In the (2-D) junction regions of a submicron MOSFET device, it is necessary to quantify the variation (or "profile") of these impurity dopants to resolution of 100 nm or less over four orders of magnitude in concentration. Achieving such high precision in the characterization of dopant profiles is a nontrivial task in both the design and manufacturing phases.

Thus, it is desirable to have a method capable of measuring dopant profiles in 2-D (or even 3-D) in a straightforward, reliable, and repeatable (nondestructive) fashion. Lateral dopant profiles have been inferred from device capacitance measurements and simulation [1], or from junction-staining [2]. A "tomographic" technique based on a matrix of SIMS measurements has been explored [3]. We have developed a technique, using scanning capacitance microscopy (SCM) and its cousin, atomic force microscopy (AFM), which satisfies many of the desired criteria for 2-D and in some sense 3-D, dopant imaging [4,5]. It is noted that other workers have used scanning tunneling microscopy (STM) for potentiometry on p-n junctions [6,7].

CAPACITANCE MICROSCOPE

We describe here mainly the SCM; the AFM implementation is discussed briefly. As depicted in Figure 1, a small metallic probe, with a radius of curvature at its tip of typically 50 nm, is scanned over a nonuniformly doped sample. A bias voltage (dc or ac) is placed on the tip, and the local capacitance, C, or its derivative, $\partial C/\partial V$, are then measured as a function of lateral position (x). The measured capacitance or capacitive gradient, as a function of bias voltage, provides a direct measurement of the activated dopant density with high spatial resolution. The inset to Figure 1 respresents the simplest equivalent circuit model for the SCM-semiconductor system. This is a series capacitance stack wherein the dopant affects the detected capacitance by virtue of dictating what the local depletion capacitance, C_d, is at lateral scan position, x. C_{air} and C_{ox} are the capacitances due to the air

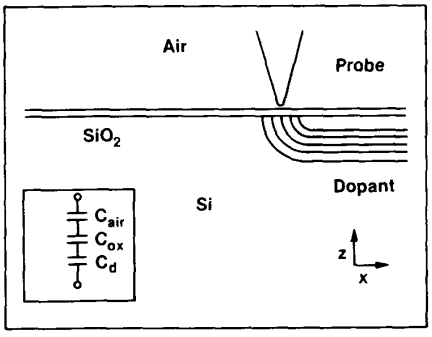

Figure 1. Illustration of the basic concept of scanning capacitance microscopy.

gap and oxide film, respectively. Figure 2 is a high-level block diagram of the SCM. The central feature of the detection system is the capacitance sensor [8]. This sensor is basically a microwave inductance strip in a resonant circuit. It can measure capacitance variations between the tip and sample on the order of $10^{-22} F/\sqrt{Hz}$. The tip scan is controlled by a feedback loop which maintains the capacitive signal constant. The piezo-scanners have a 6-mm lateral and 3-mm vertical range. To avoid low-frequency drifts caused by stray capacitances, a vertical dither is placed on the

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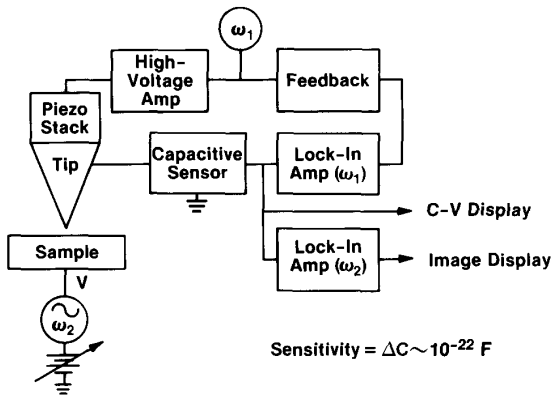

Figure 2. Block diagram of the SCM apparatus with sample at bias voltage, V.

tip/sample spacing typically at 30 kHz. This also provides a means to measure the capacitive gradient. The ac signal is filtered and rectified by the lock-in (ω_1). The lock-in output is sent to an integrating feedback loop to maintain the constant ac signal by adjusting the average tip height above the sample. Such a system has achieved 25-nm resolution in topographic mode [9].

In the AFM implementation [5], a laser heterodyne detection system is used to measure excursions of a cantilever-style tip which is mechanically oscillated near its resonsance. These deviations are directly proportional to tip-to-sample forces, including the coulomb force due to mutual capacitance.

A signal generator provides an ac and/or dc signal between tip and sample at the desired frequency (ω_2). Thus, a C-V curve can be taken at any given lateral position, or $\partial C/\partial V$ curves at constant dc bias can be acquired as the tip is scanned. Both the tip scan and data acquisition are controlled by a laboratory computer. In either SCM or AFM mode, a separate laser (0.633 nm) is used as an optical carrier pump to obtain transport data, described below.

SAMPLE PREPARATION

Measurements have been made on a variety of VLSI structures: diffusion gratings, submicron MOSFET structures, and even DRAM devices. In this work, we describe data taken on uncleaved gratings and on cleaved MOSFETs.

The gratings were prepared to emulate typical FET source/drain diffusion pockets. N-type silicon substrates were thermally oxidized to grow 24 nm of SiO_2. The wafers were masked with 500-nm photoresist with an 8-μm period. A 50 keV BF_2 implant at $10^{-15} cm^{-3}$ dose was performed, producing a peak concentration of roughly $10^{20} cm^{-3}$ near the surface of the unmasked regions. The photoresist was stripped, leaving a topographically flat, nonuniformly implanted silicon surface. A 900 C, 10-min anneal was performed to activate (and diffuse) the dopant. The 8-μm period was chosen in this case to minimize the effects of possibly large lateral depletion at some tip biasses. Small area sections containing the gratings (typically a few mm^2) were cut from the wafer and mounted on the SCM stage with the sectioned wafer surface up. The MOSFET samples were actual production devices from IBM's 1-Mb DRAM. A small section of the wafer was cleaved to expose an FET cross section. The section was mounted with the cleaved face up on the stage. For both the grating and the MOSFET samples, measurements were made in ambient air.

MEASURED CAPACITANCE DATA

For the grating structure, Figure 3 shows $\partial C/\partial V$ data vs. lateral scan position, x, for three typical tip-to-sample dc biasses. The line traces clearly indicate the dopant variation in the sample on a scale less than 1 μm. The periodic variation is 8 μm. The signal varies strongly with bias voltage as expected from the simple model, based on depletion capacitance in the semiconductor. The largest signal is apparent in the lightly-doped (n-type) region, due to the fact that depletion capacitance varies more rapidly with bias at lower dopant densities. Note that there is some defect or nonuniformity in the fourth period of the data which has apparently shifted the depletion voltage. Since the sample surface was measured in topographic mode to be nearly atomically flat, this defect is evidently some fixed charge, perhaps in the oxide.

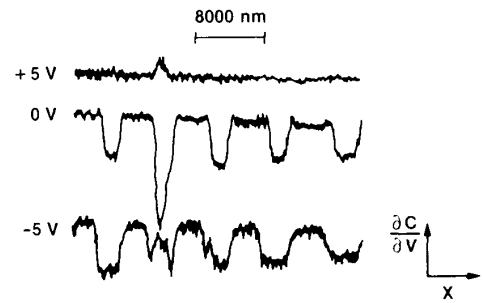

Figure 3. Three line scans of the grating structure showing the $\partial C/\partial V$ signal at different bias voltages.

Figure 4 shows a set of C-V curves taken with the SCM tip held fixed while positioned over several points along the grating structure. When the tip is centered over the low-doped region (position D), the C-V curve looks very much like a "textbook" high-frequency C-V curve. As the tip is moved closer to the junction near the more highly doped p-type region, the C-V curves are altered from the usual 1-D form. A gradual transition is evident as the junction is approached, due to the mixing of lateral depletion effects in this region of highly inhomogeneous doping. Note that, at positions A, B, and C, the signature of both p- and n-type dopant are evident (positive and negative C-V slope, respectively). When the tip is well inside the highly-doped region (i.e., to the left of position A), a signal is measured but cannot be displayed on the scale of Figure 4.

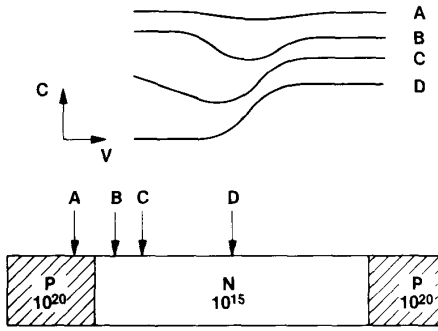

Figure 4. Local C-V measurements acquired on grating structure with tip stationary at various points.

Figure 5 shows a raster scan of the tip over a region close to a junction on the grating structure at fixed dc bias. The 2-D image of the $\partial C/\partial V$ output resolves the transition from the p-side to the n-side of junction (high doping to low doping) to about 100 nm. Note the signal variations on the low-doped side (left) over a similar scale. This image is repeatable. It is intriguing that the doping in this region ($10^{15} cm^{-3}$) implies an average spacing between fixed dopant ions on the order of 100 nm.

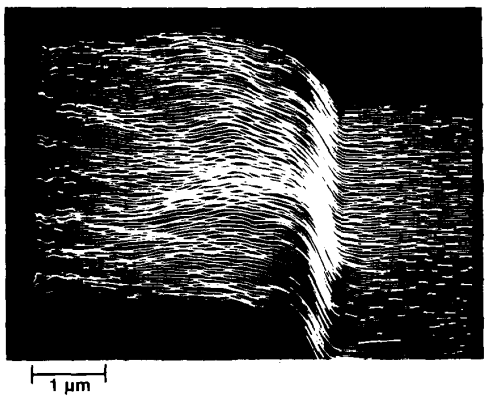

Figure 5. An image of a 2-μm-square area of the grating structure. Note 100-nm "defects" to the left (10^{15} cm^{-3}); the p-n junction "falls" to right.

Figure 6 shows a raster scan of the tip over two adjacent active regions exposed on the cleaved face of the MOSFET sample. The cross-sectioned FET appears inverted from the usual perspective so that signal strength (again, $\partial C/\partial V$) can be plotted increasing towards the top of the figure. The arrows indicate the the appearance of low-doped channel regions and the substrate appears as the constant background. The metallurgical channel length was designed at less than 1 μm.

Figure 7 shows the effects of optically pumping on the $\partial C/\partial V$ signal near a junction on the grating structure. A 0.1-mW laser (0.633 nm) is focused on the tip and sample. Both the amplitude of the signal and apparent location of the lateral depletion edge are significantly modified by the light. The upper (lower) trace was taken with the pump off (on). Note that the optical pump reduces the capacitive signal over the low-doped region (as well as shifting the apparent depletion edge). We believe that these effects are attributable to the creation of electron-hole pairs, which reduce depletion by providing carriers to short out the field in the space-charge regions both vertically and laterally.

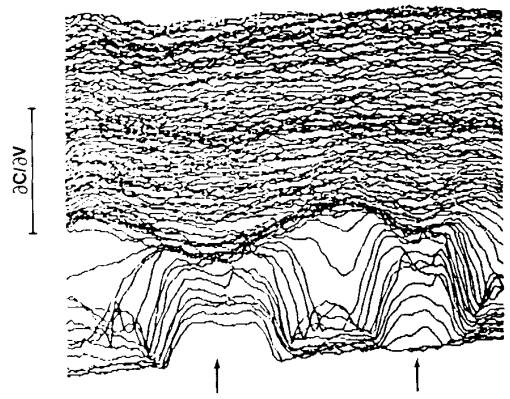

Figure 6. An image of a cleaved MOSFET. The substrate increases toward the top of the figure. Two channel regions with high ∂C/∂V signal are visible (indicated by arrows).

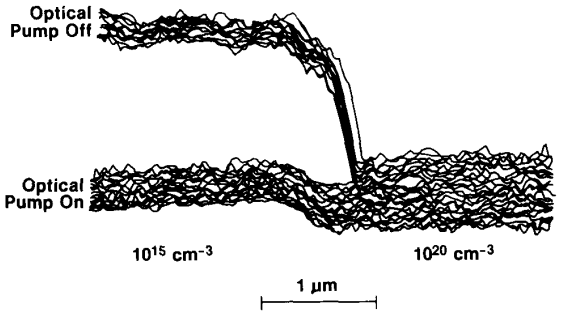

Figure 7. Line scan of the ∂C/∂V signal as the tip is is scanned across a junction in the grating structure.

DATA DECONVOLUTION

A first-order deconvolution of the the $\partial C/\partial V$ vs. x data to obtain crude contours of activated dopant density in 2-D is possible by a simple extension of the standard C-V analysis [10]. One integrates the $\partial C/\partial V$ vs. data (e.g. the data of Figure 3) to obtain C(V) at x to within a constant. (A less efficient procedure requires measuring both $\partial C/\partial V$ vs. x and C(V) vs. x, as in Figure 4, to avoid the integration procedure.) The modified standard model yields an expression for local activated dopant density, $N_D(x, z)$, where z is the vertical dimension (in the bulk):

$$N_D(x,z(x)) = -(C^{-3}(a;V)/(\partial C/\partial V)/(q\varepsilon_s))^{-1},$$

where q is the electronic charge, ε_s is the dielectric coefficent for silicon. It is important to note that z is interpreted the local depletion depth:

$$z(x) = \varepsilon_s \times (1/C(a;V) - 1/C_{ox} - 1/C_{air})$$

The parameter *a*, which appears in C(a;V), is necessary to scale the integrated, measured $\partial C/\partial V$ signal. *a* is unitless and of order unity (0.3 in this case); it is interpreted as dependent on the effective spot size which the tip presents to the sample.

Figure 8 shows the results of such a deconvolution for data taken on the grating structure near one of the junction regions. The contours of dopant density (cm^{-3}) in the upper plot are the result of a process simulation of the steps required to create the sample structure. The contours in the lower plot are the deconvolution of data such as shown in Figure 3. The agreement is admittedly gross, but is encouraging since it indicates that

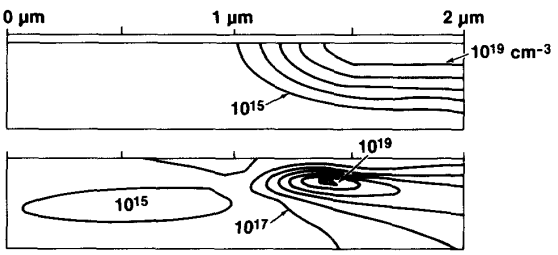

Figure 8. 2-D dopant profile of grating structure. Upper profile is simulated; lower profile is deconvolved from SCM data.

the data have some quantitative value. Much of the error in the deconvolution is attributed to the neglect of junction capacitance and to the assumption of a homogeneous depletion front near the the tip. However, evidence of the basic physical model's validity can be seen by the following comparison. Figure 9 shows the

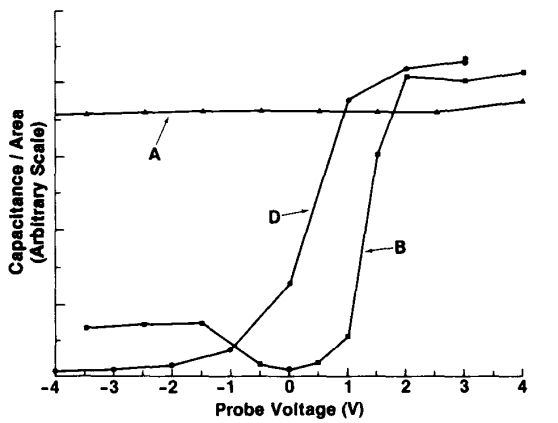

Figure 9. Results of 2-D simulation of C-V data of Figure 4.

results of a 2-D electrical simulation of the tip-sample system for the grating structure; Figure 4 shows the measured data corresponding to the same bias conditions. The qualitative agreement is apparent. (The simulator FIELDAY [11] was used for this purpose.)

SUMMARY

Lateral dopant profiling has been demonstrated on a 100-nm scale by a straightforward, basically nondestructive technique. With increased sensitivity, imaging on a 10-nm scale is believed feasible. Other important measurements can evidently be made, including trapped-charge, surface-defects, direct measurement of a variety of device-scale capacitances and, perhaps, carrier transport. It is anticipated that, with moderate enhancement, characterization of VLSI devices using SCM or AFM will have much value in future device development and manufacture.

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